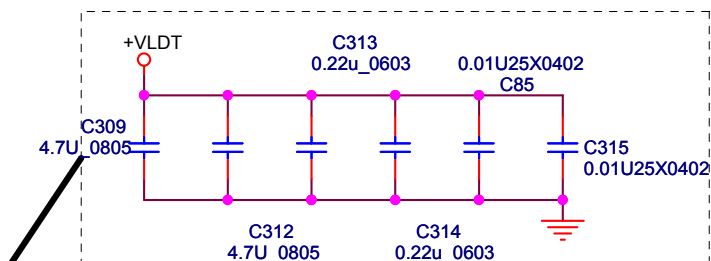
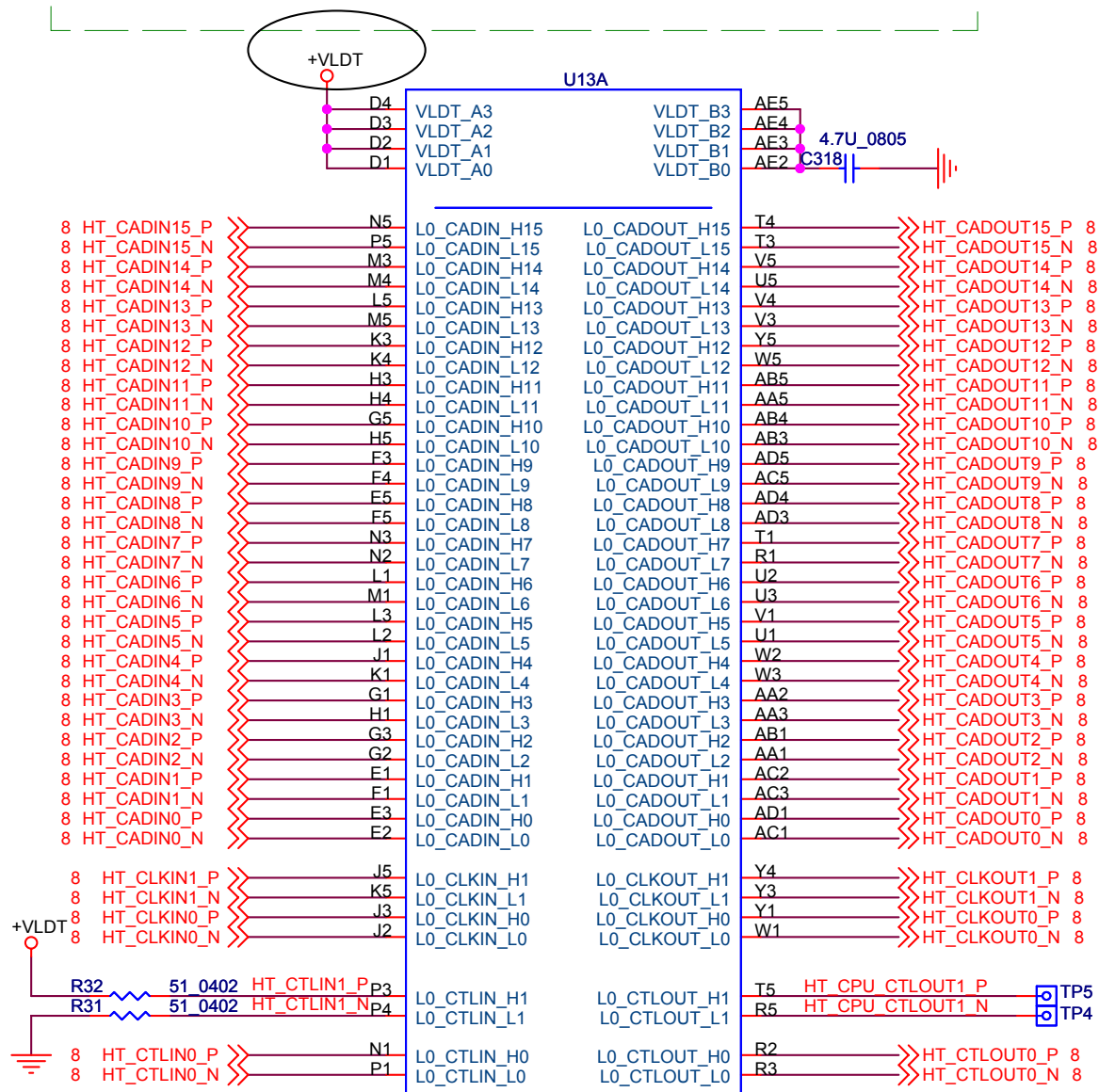




## PROCESSOR HYPERTRANSPORT INTERFACE


VLDT\_Ax AND VLDT\_Bx ARE CONNECTED TO THE LDT\_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



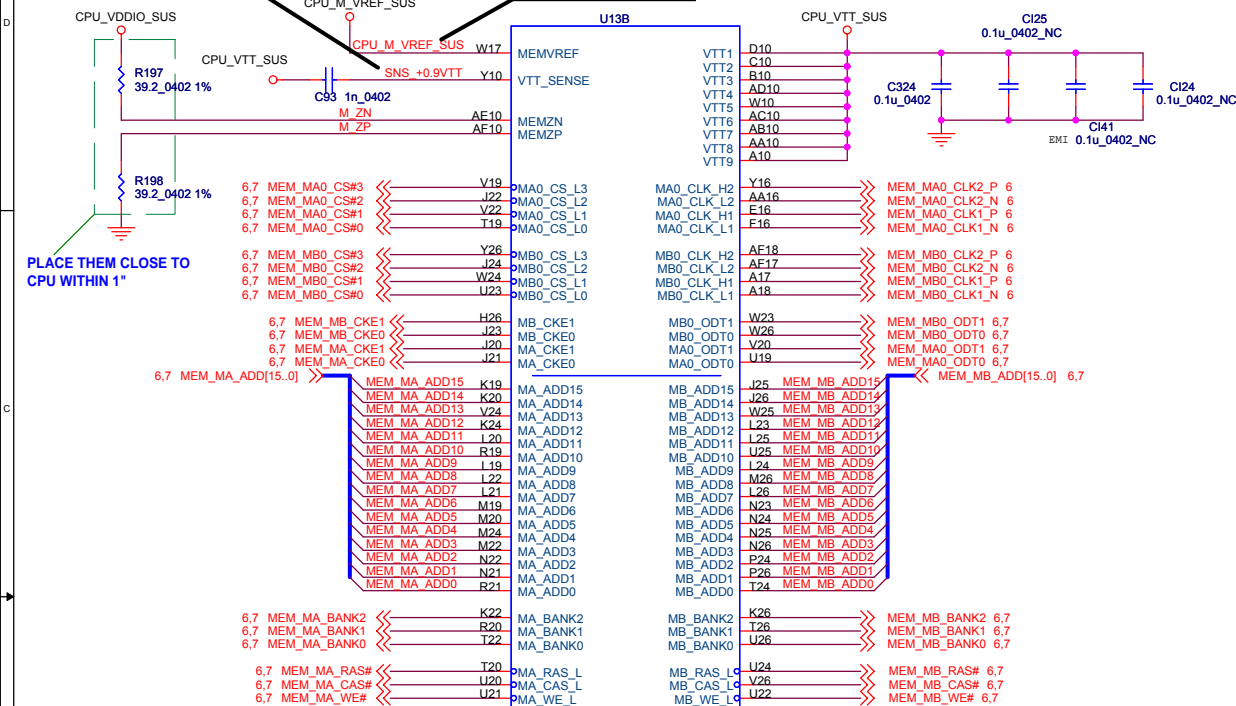
### LAYOUT: Place bypass cap on topside of board

NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS  
PLACE CLOSE TO VLDT0 POWER PINS

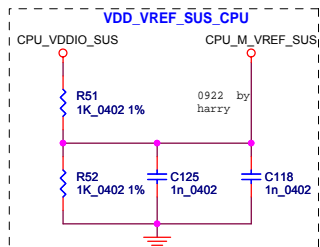
Athlon 64 S1 Processor Socket

		<b>MICRO-STAR INT'L CO.,LTD.</b>	
Title			
<b>AMD S1 HT I/F</b>			
Size	Document Number		Rev
Custom	<b>MS-14141</b>		0.A
Date:	Tuesday, September 26, 2006		Sheet 2 of 37

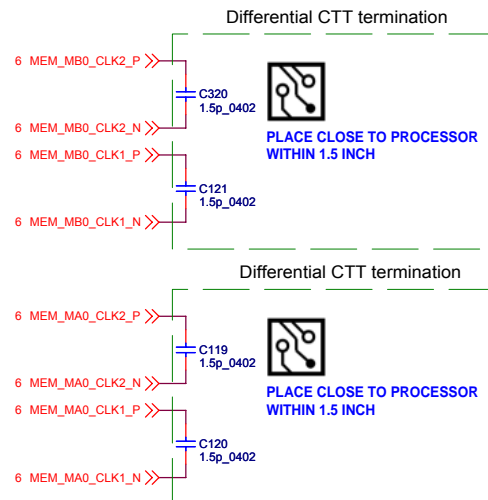
15MIL trace, 20MIL space  
shorter than 1"



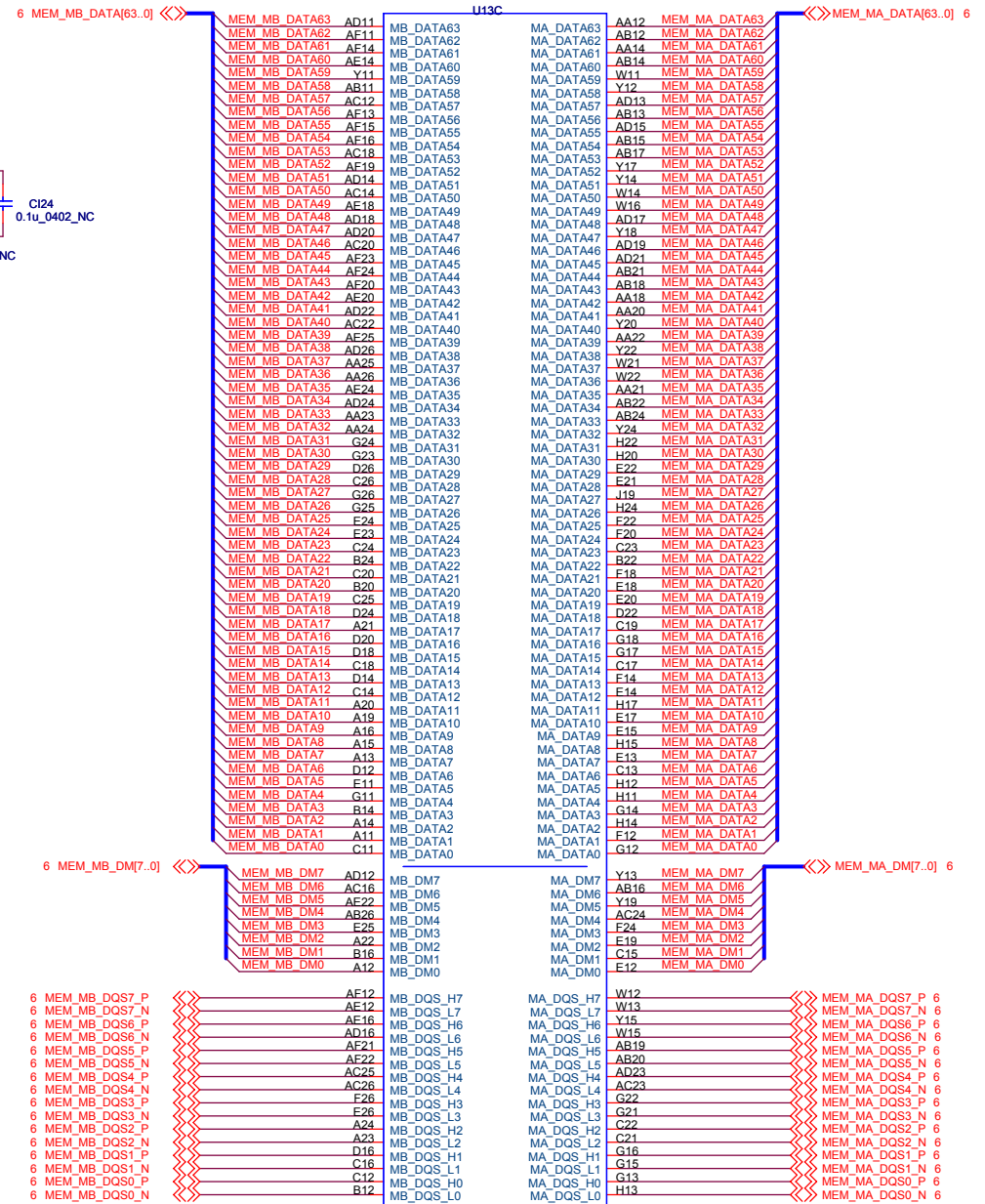
## DDR II: CMD/CTRL/CLK

Athlon 64 S1  
Processor  
Socket

**LAYOUT:PLACE CLOSE TO CPU**



## Processor DDR2 Memory Interface



**DDR: DATA**  
Athlon 64 S1  
Processor  
Socket

Athlon 64 S1g1  
uPGA638  
Top View



**MICRO-STAR INT'L CO.,LTD.**

Title  
**AMD S1 DDRII MEMORY I/F**Size  
A3

Document Number

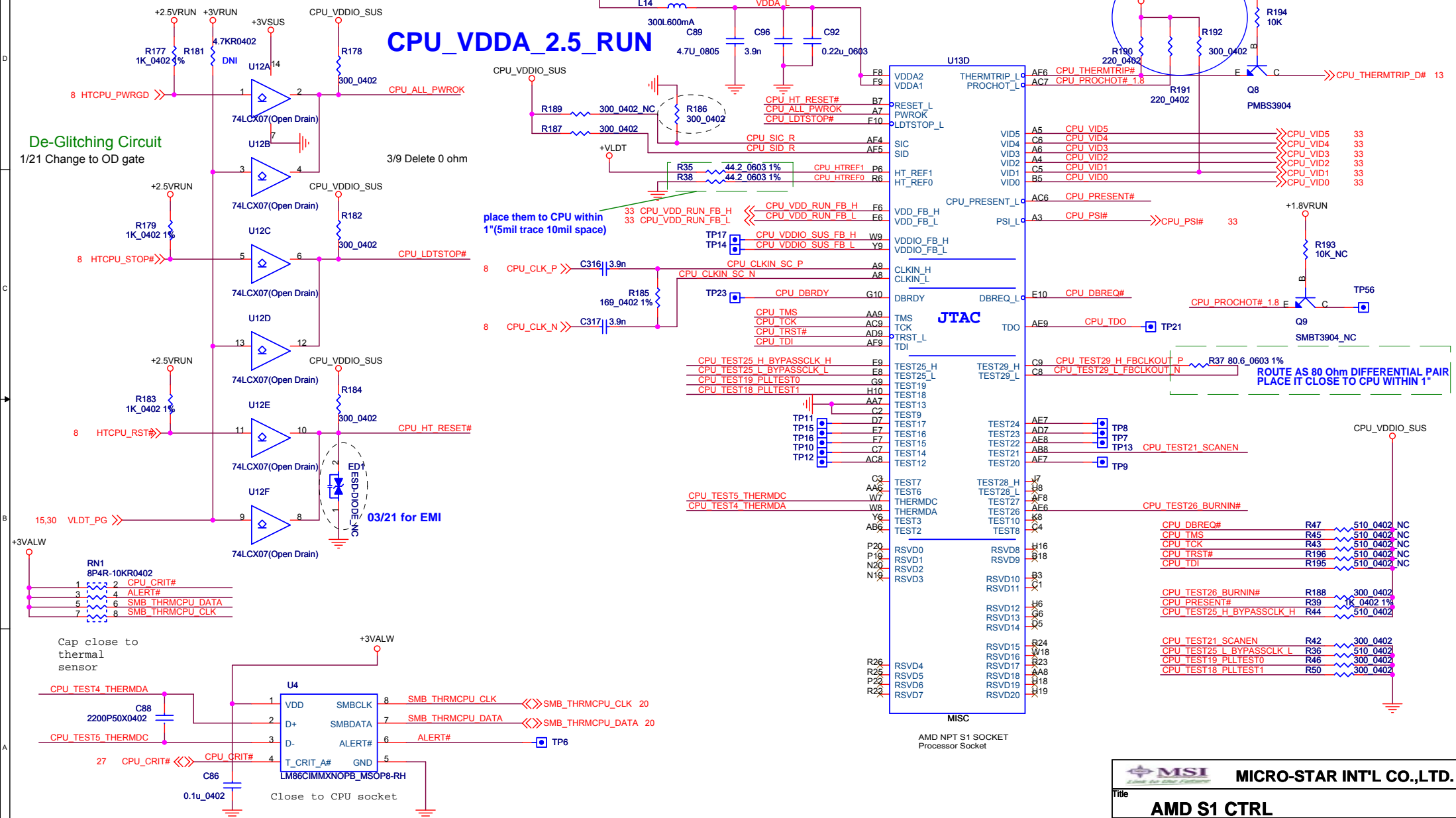
A3	<b>MS-14141</b>
----	-----------------

Rev	0.A
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MS-14141		Date: Tuesday, September 26, 2006		Sheet 3 of 37	
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**LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.**

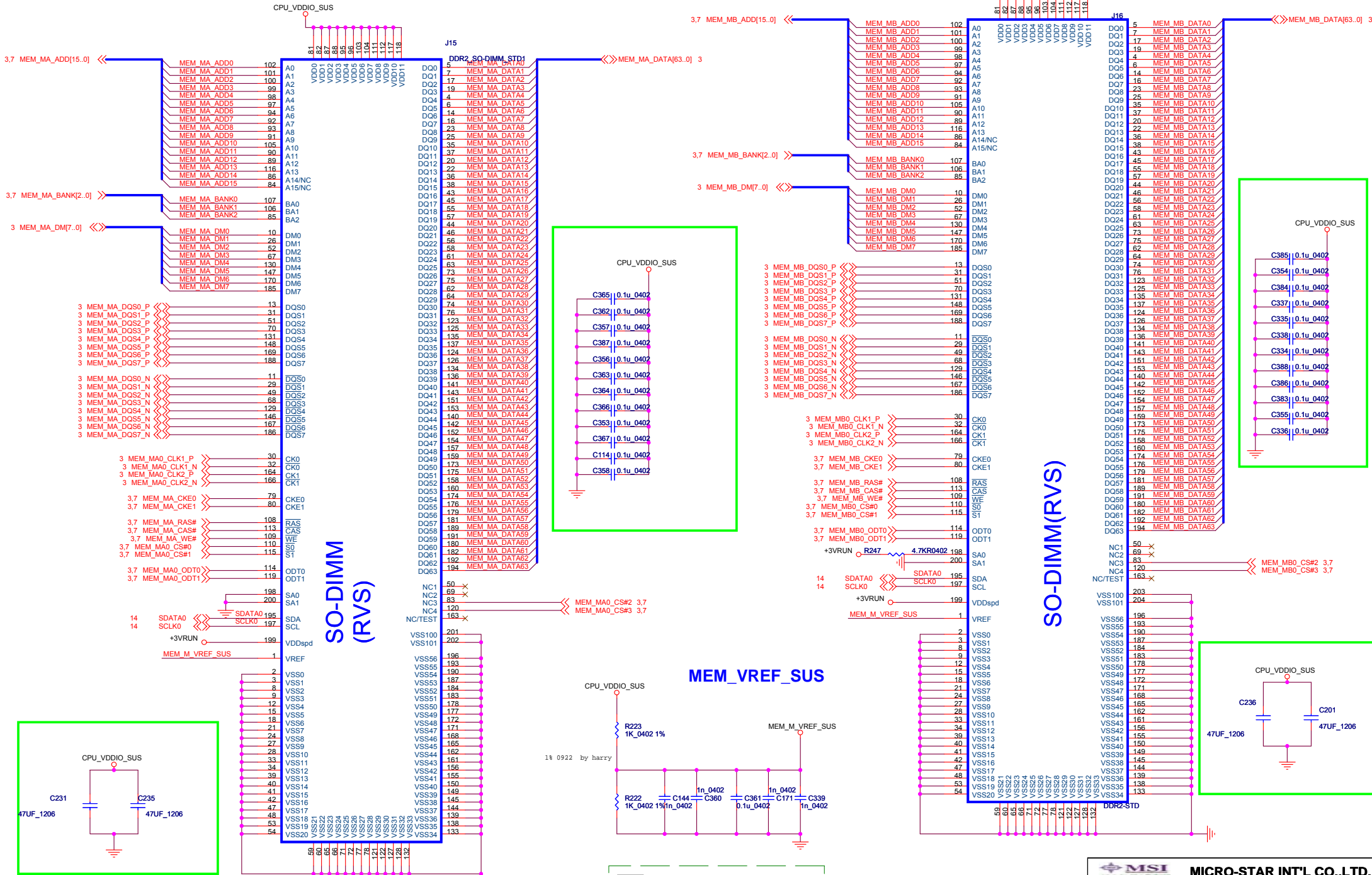
0824  
CPU\_VDDIO\_SUS



Title			
<b>AMD S1 CTRL</b>			
Size B	Document Number	Rev 0.A	
	<b>MS-14141</b>		
Date:	Tuesday, September 26, 2006	Sheet	4 of 37

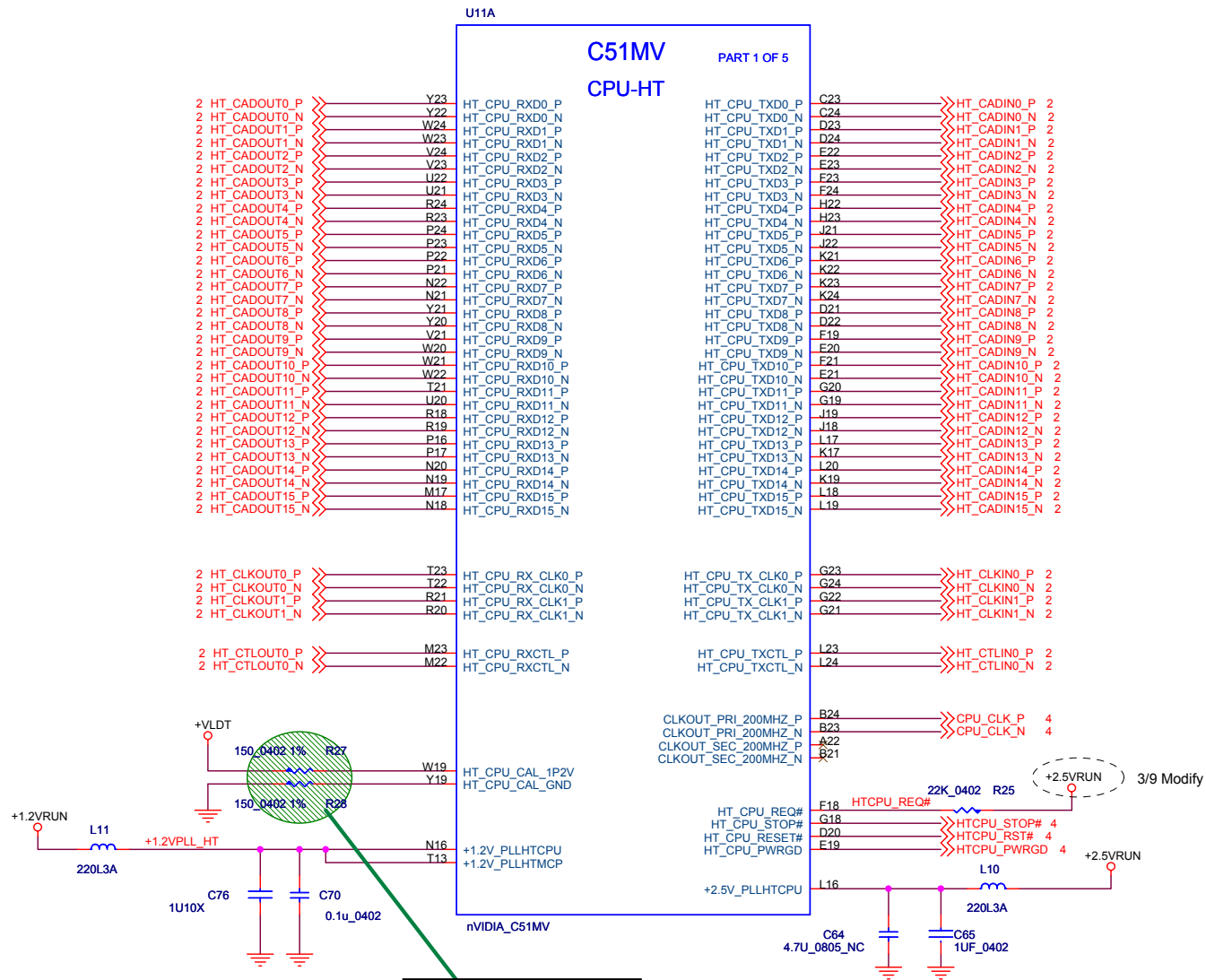




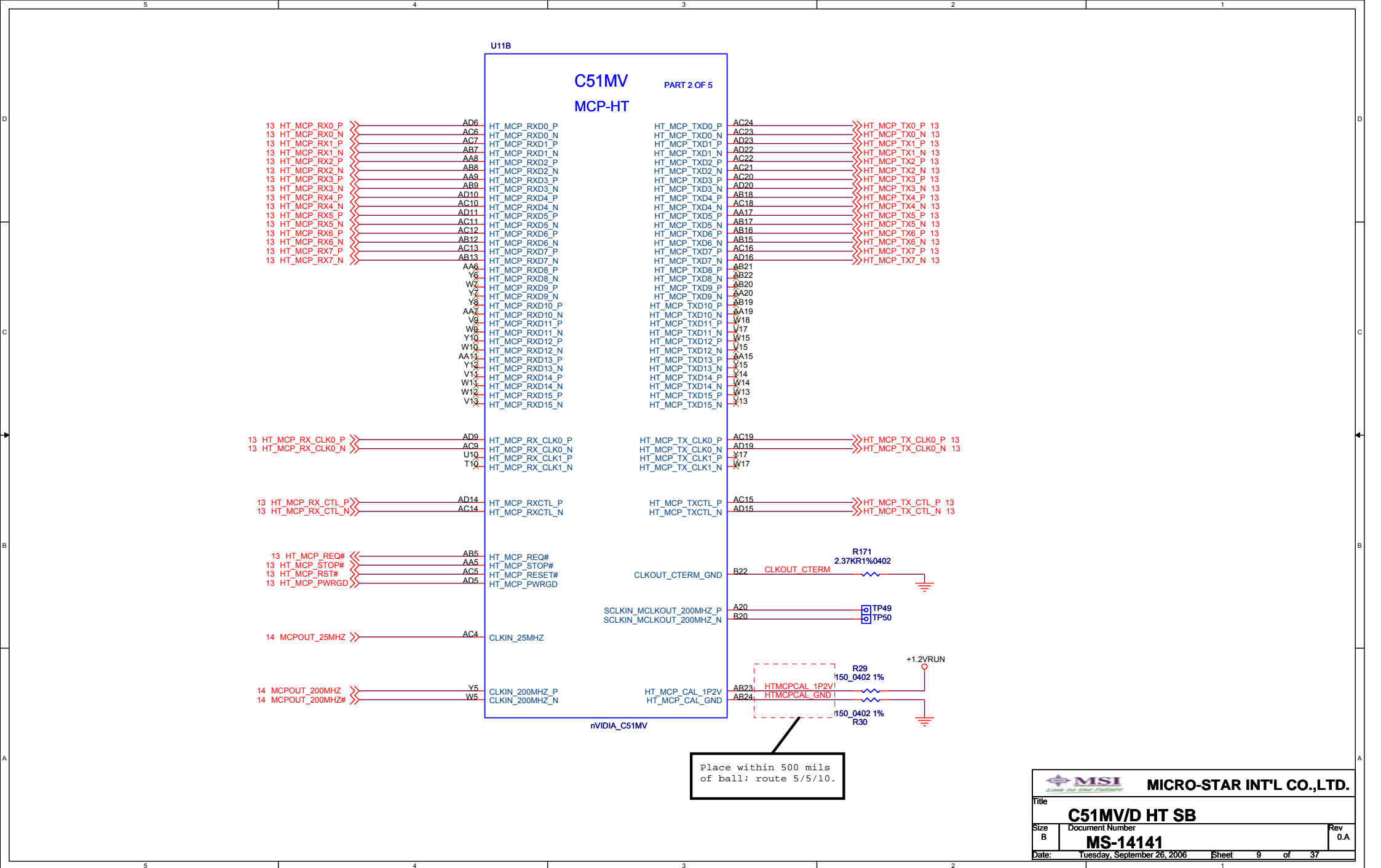


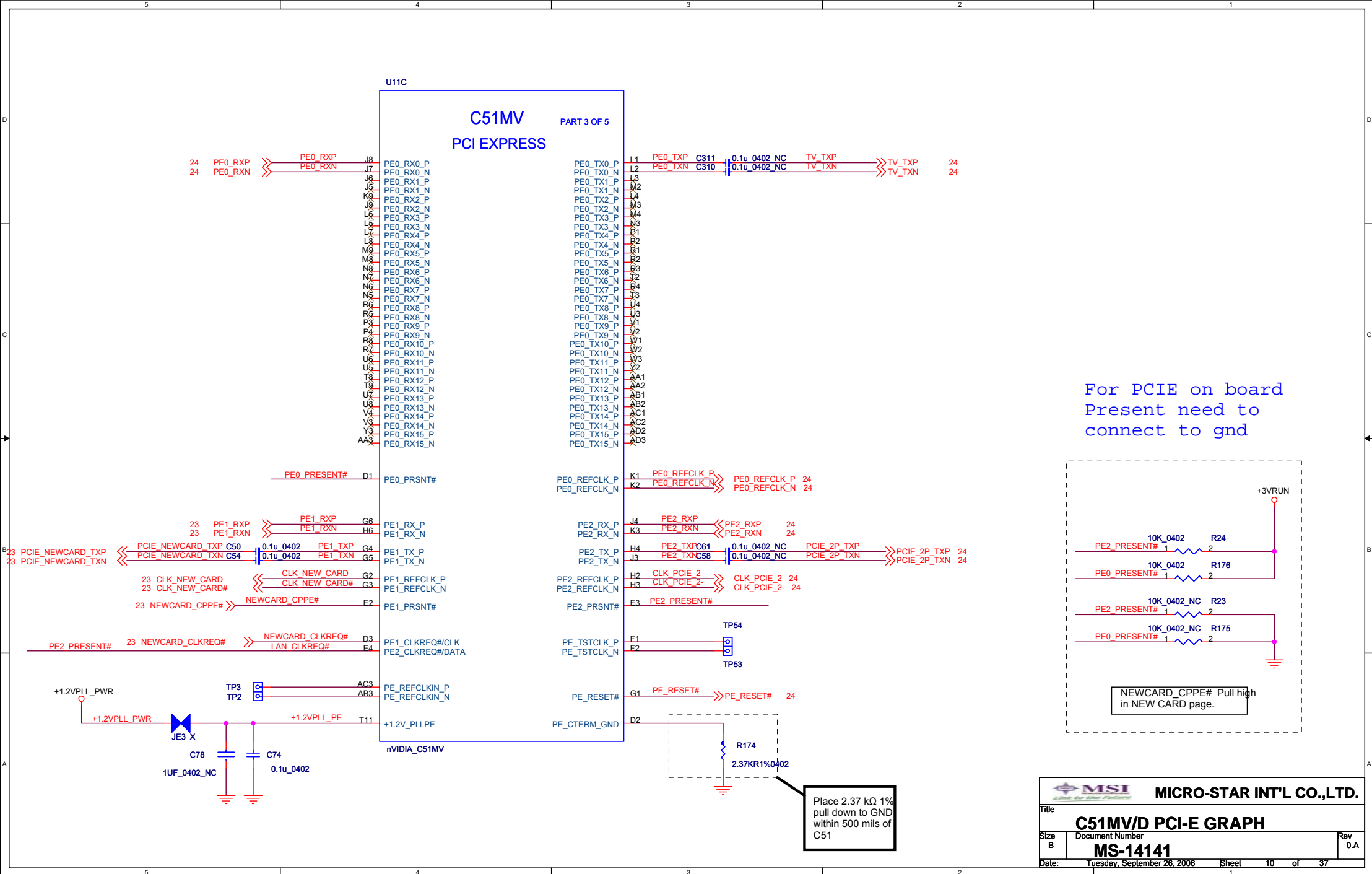
LAYOUT: PLACE CLOSE TO DIMMS





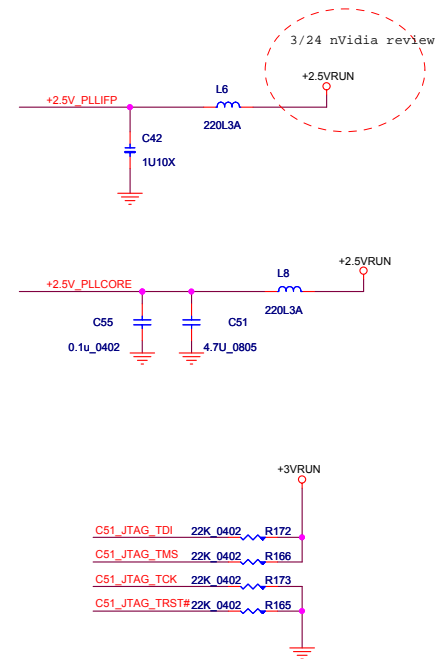
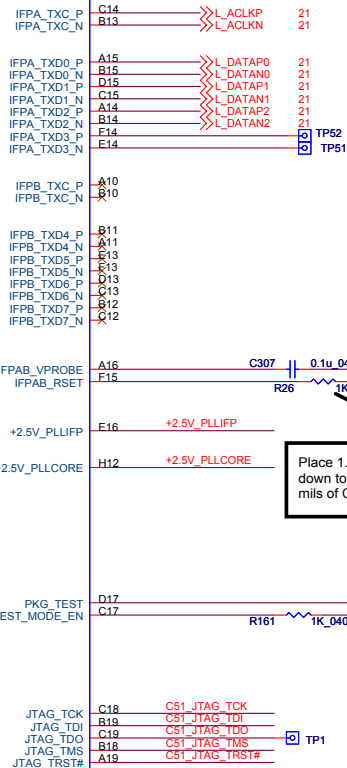
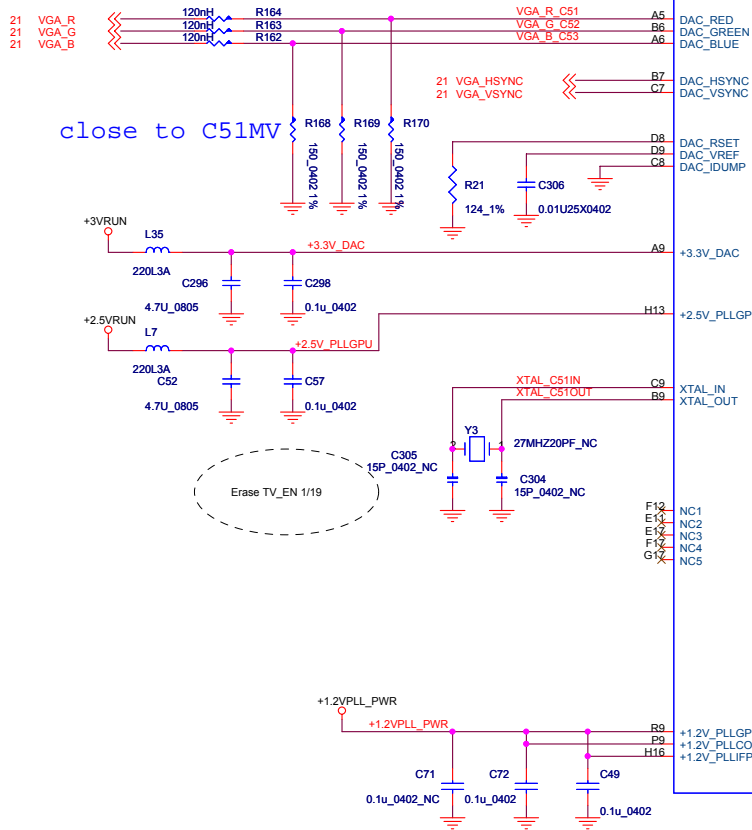






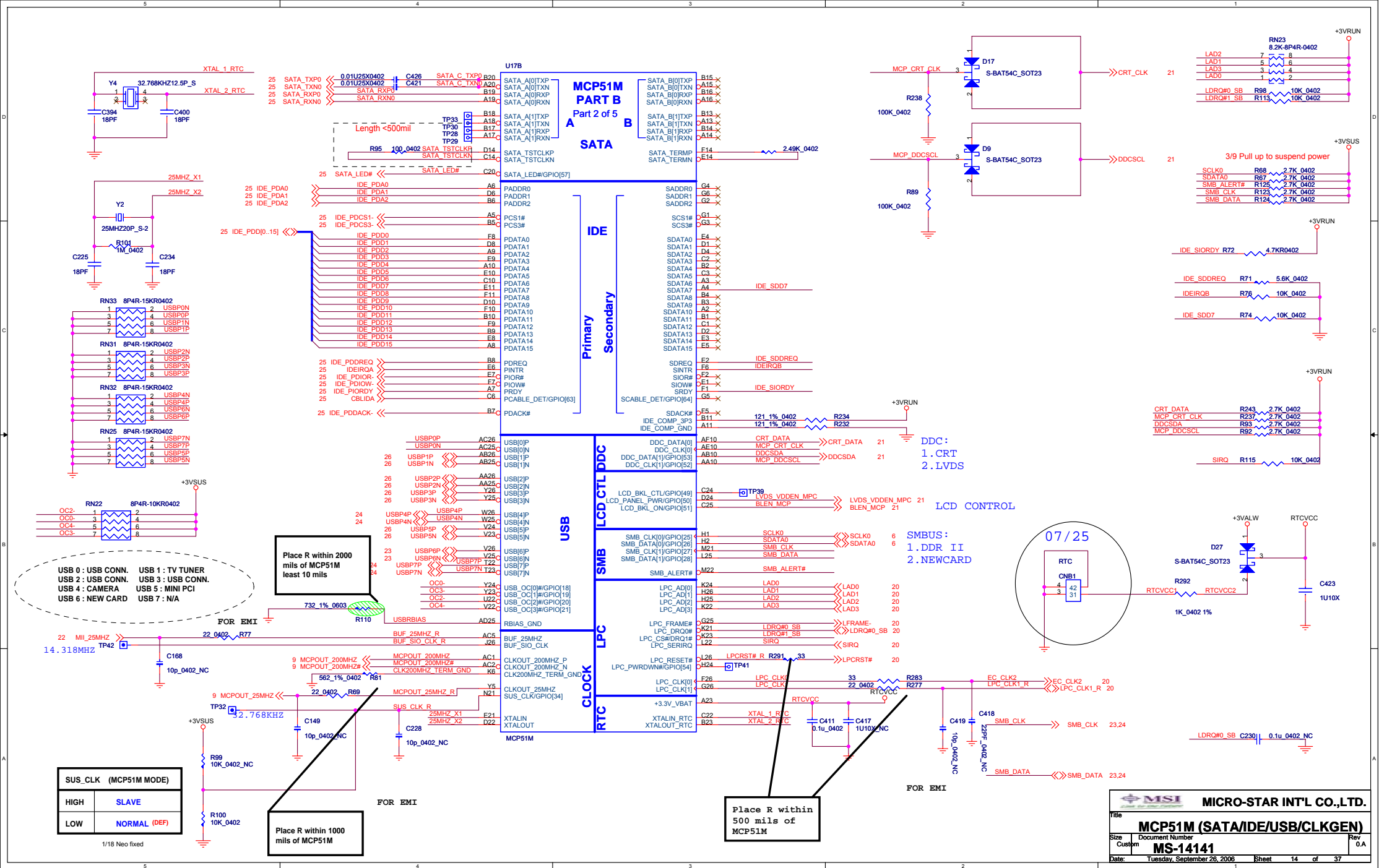
C51MV  
FLAT PANEL

PART 4 OF 5










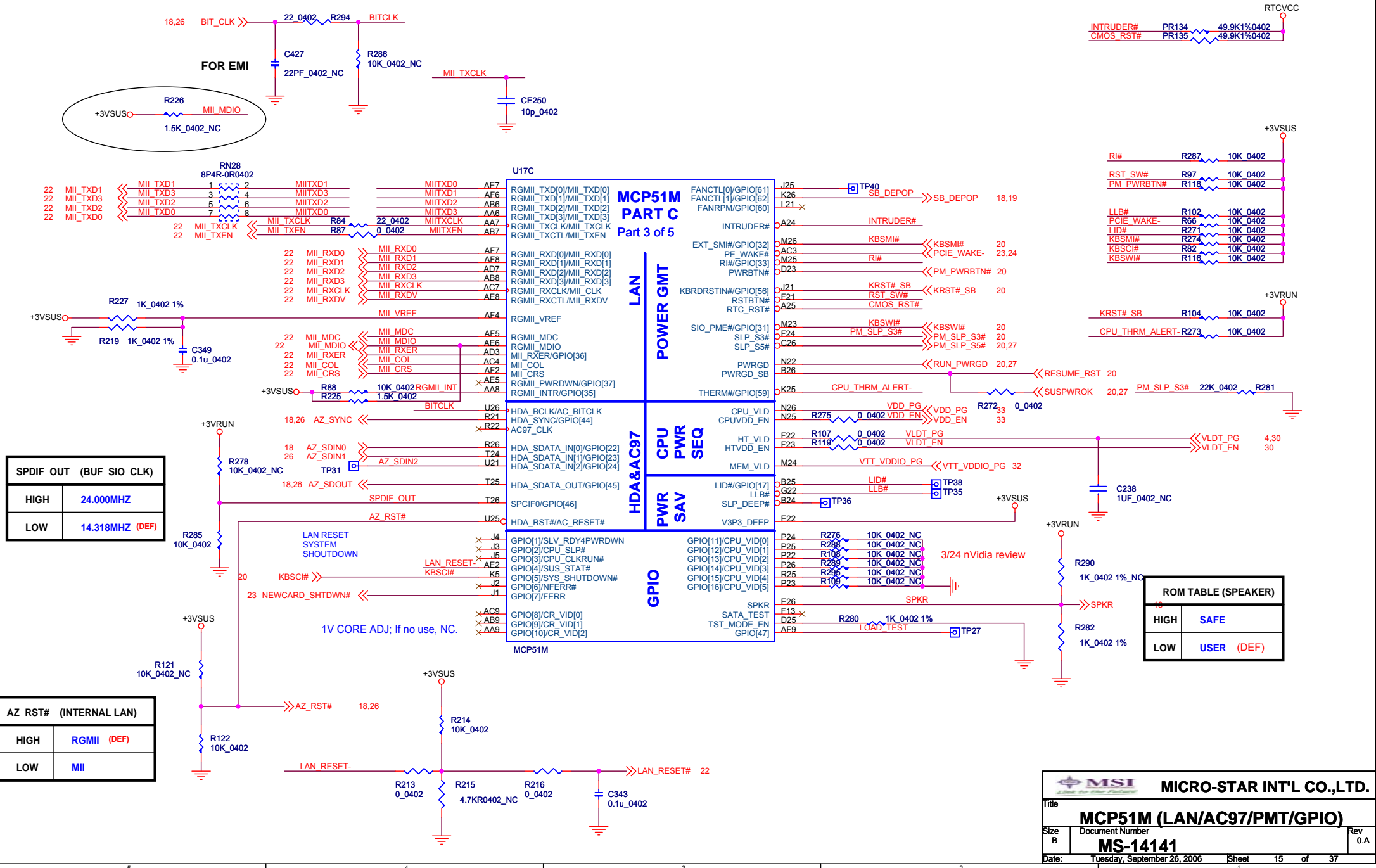


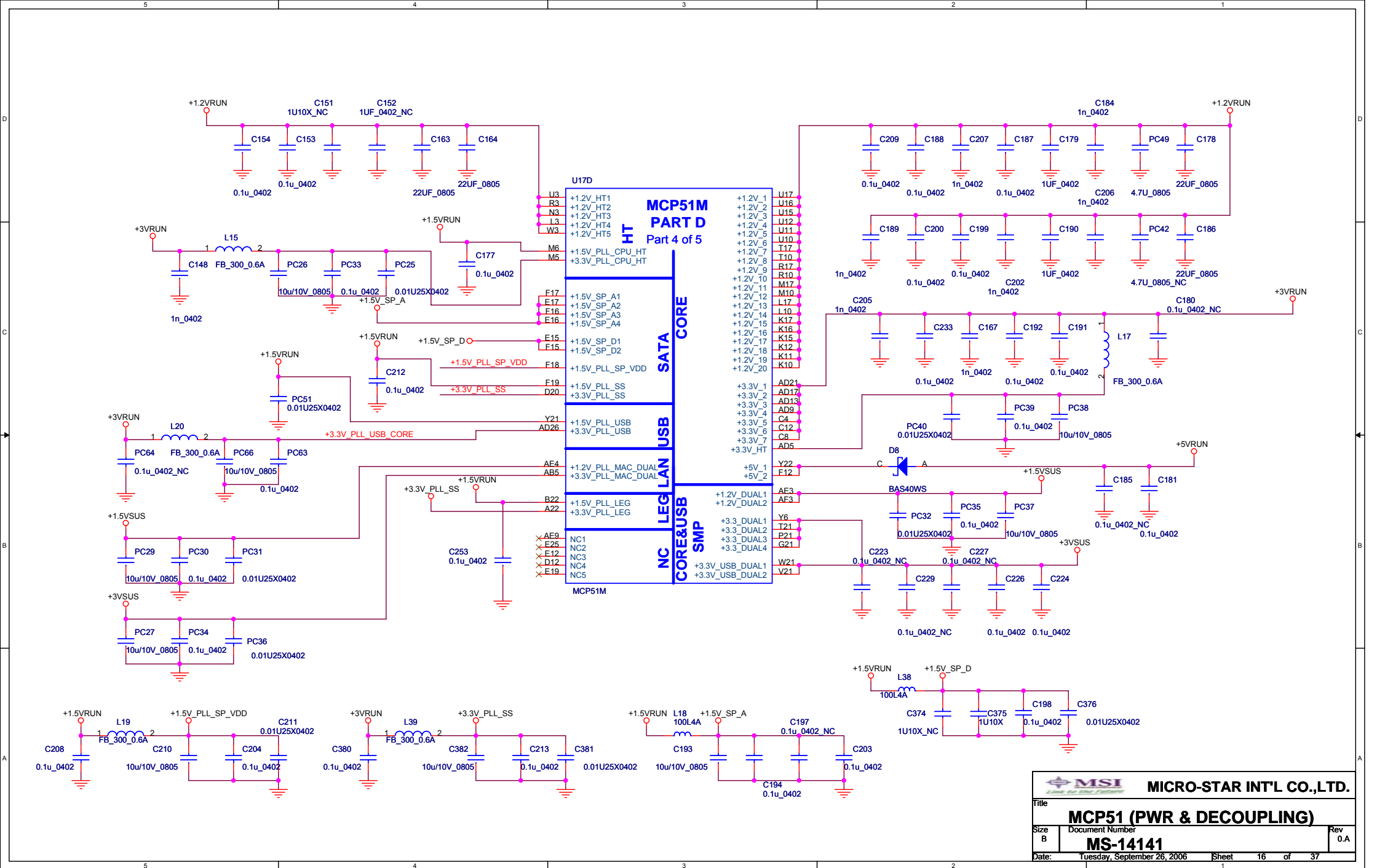
SPDIF_OUT (BUF_SIO_CLK)	
HIGH	24.000MHZ
LOW	14.318MHZ (DEF)

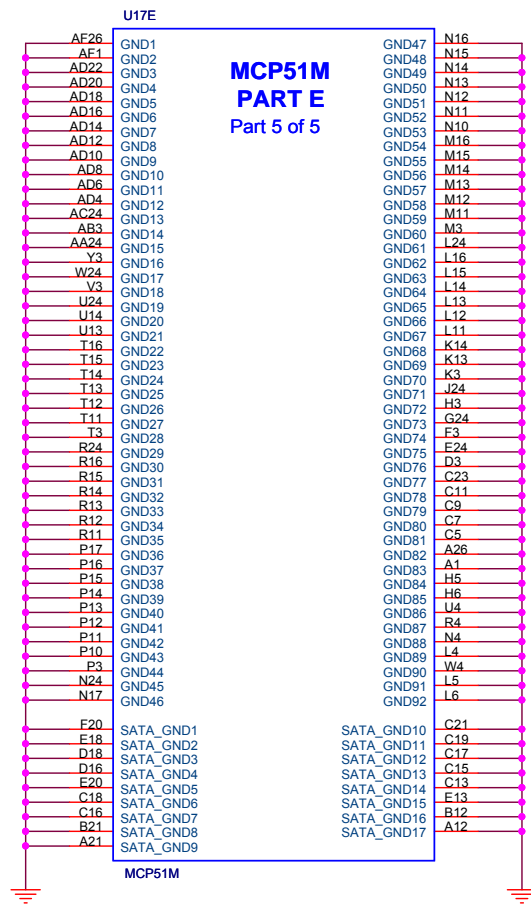
AZ_RST# (INTERNAL LAN)	
HIGH	RGMII (DEF)
LOW	MII

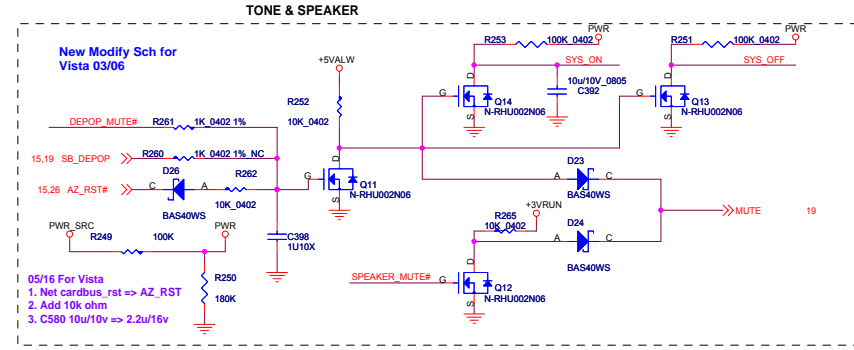
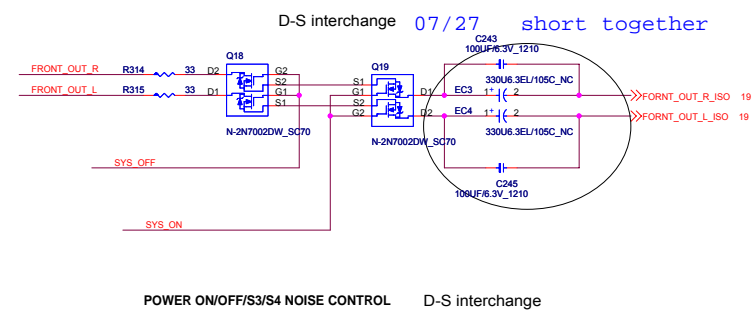
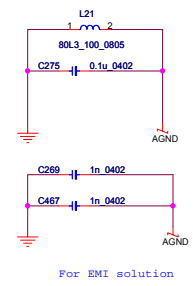
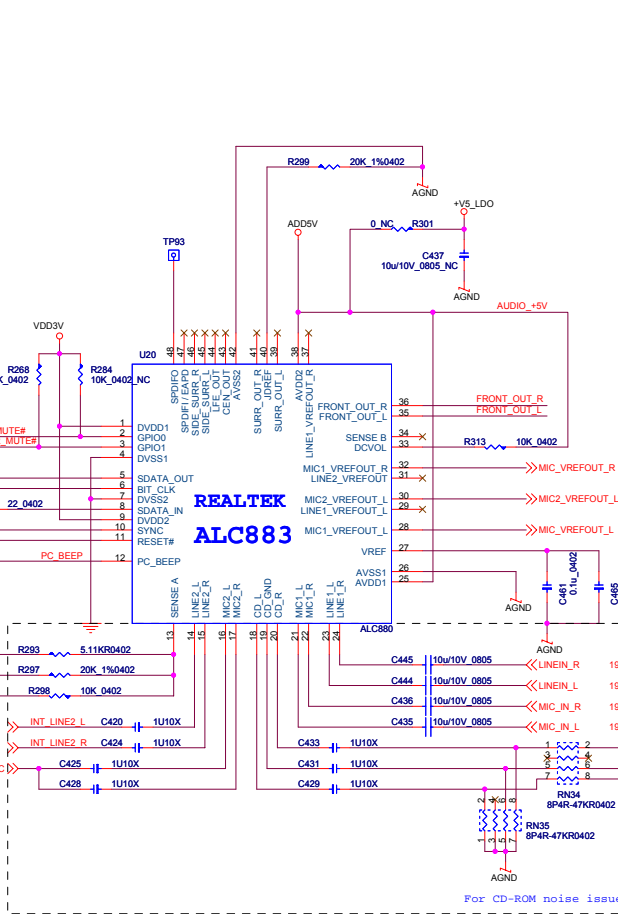
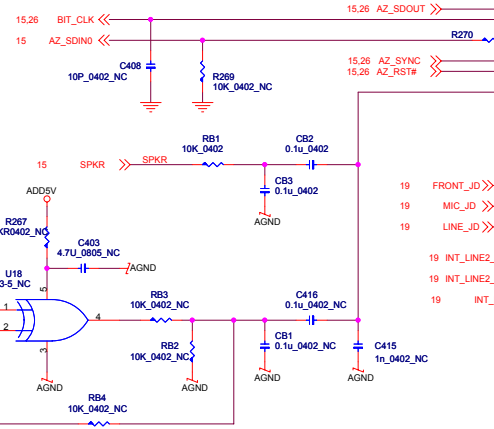
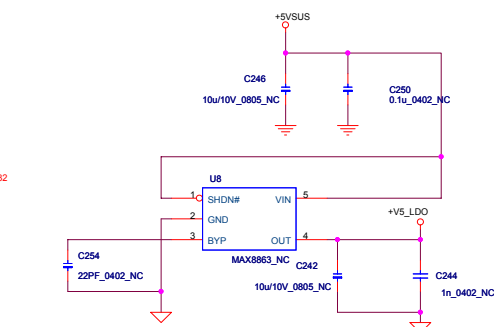
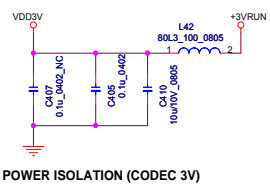
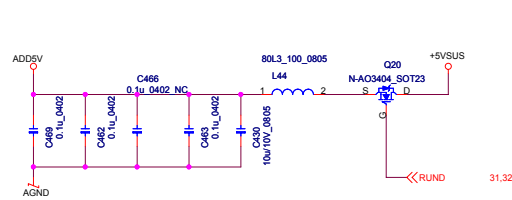
ROM TABLE (SPEAKER)	
16	
HIGH	SAFE
LOW	USER (DEF)

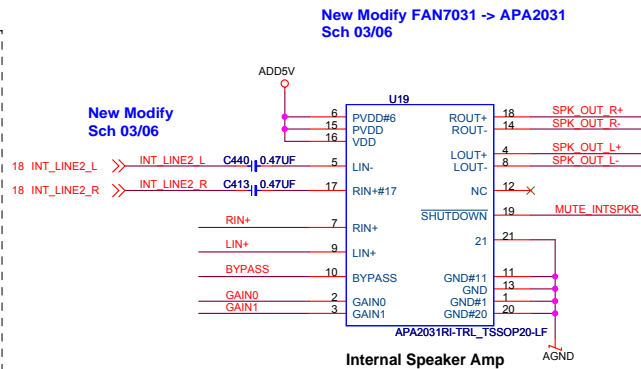
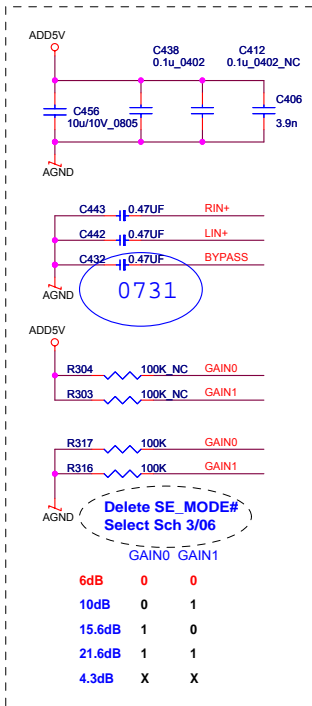
		<b>MICRO-STAR INT'L CO.,LTD.</b>	
<b>Title</b> <b>MCP51M (LAN/AC97/PMT/GPIO)</b>			
<b>Size</b> B	<b>Document Number</b> <b>MS-14141</b>		<b>Rev</b> 0.A
<b>Date:</b>	<b>Tuesday, September 26, 2006</b>	<b>Sheet</b>	<b>15 of 37</b>



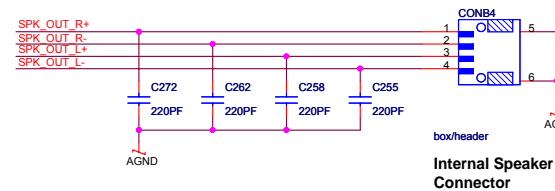
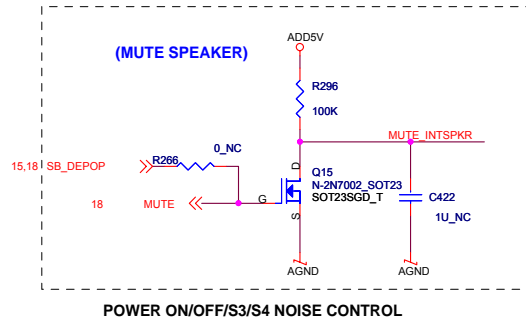
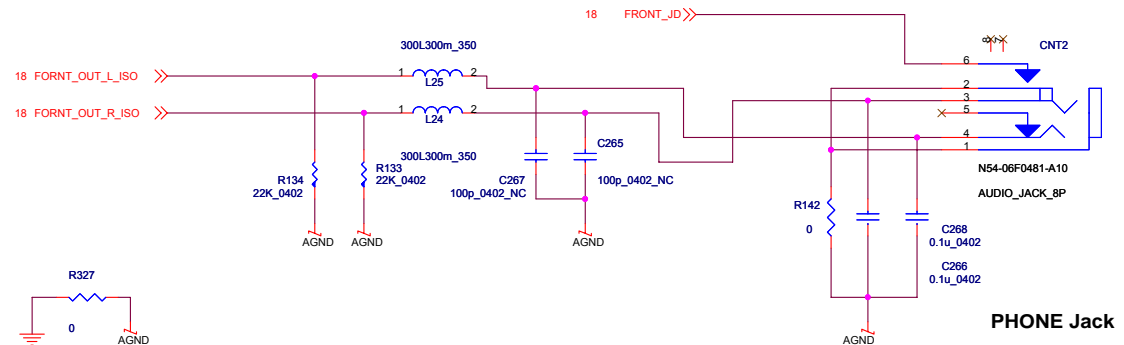
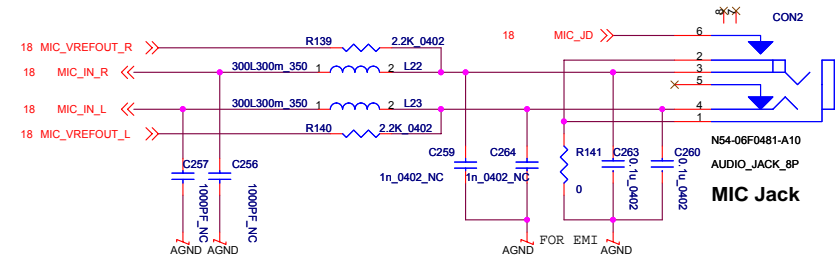
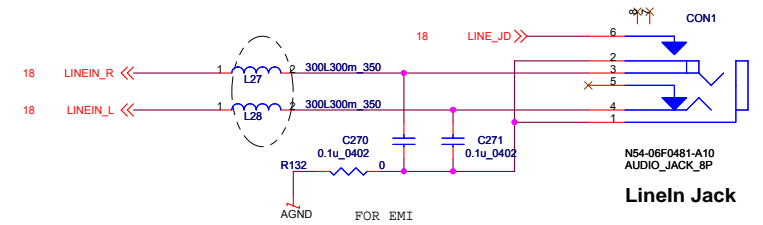
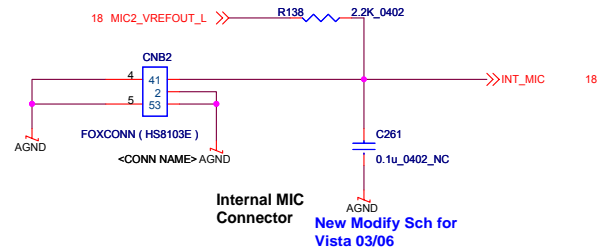


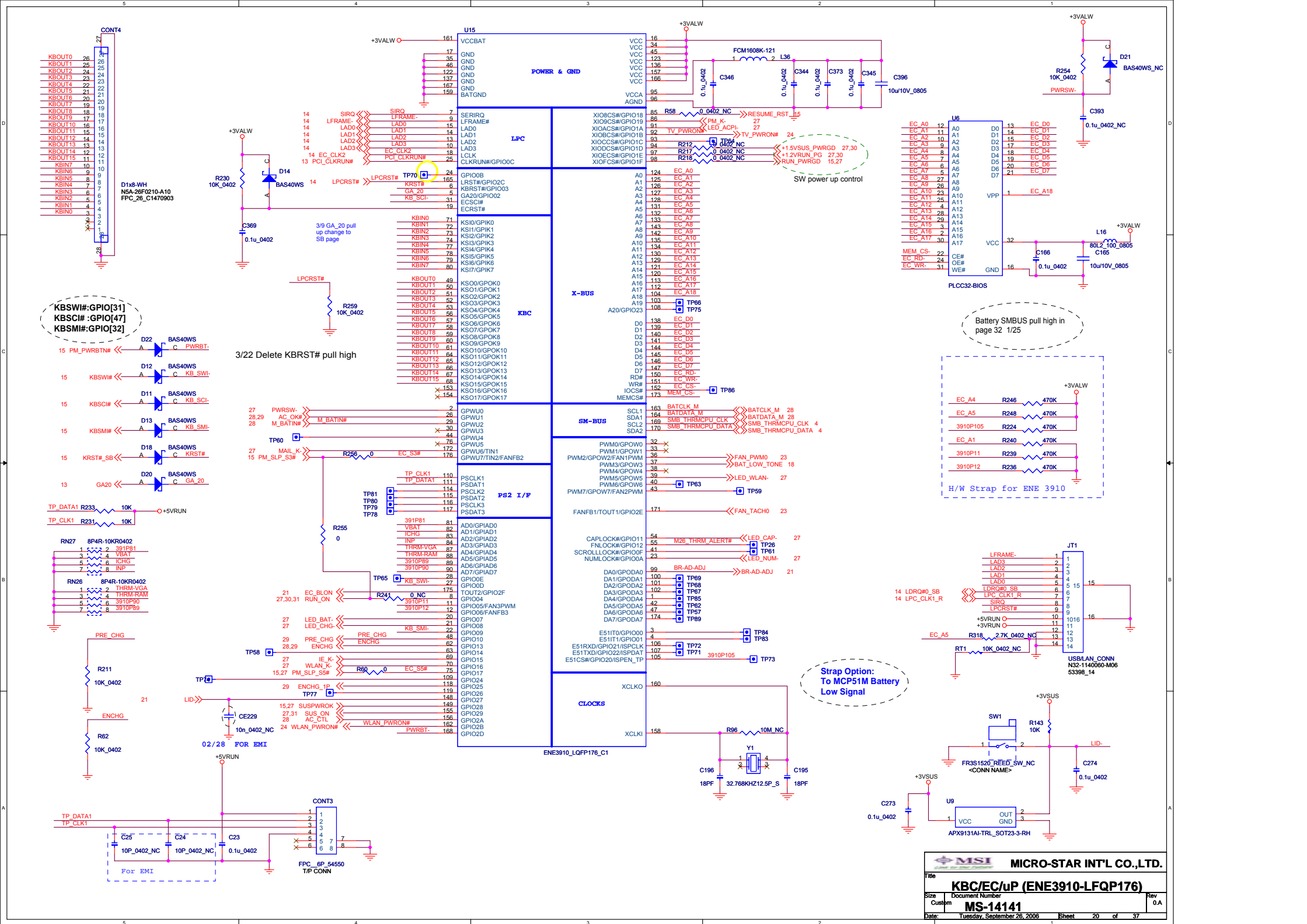




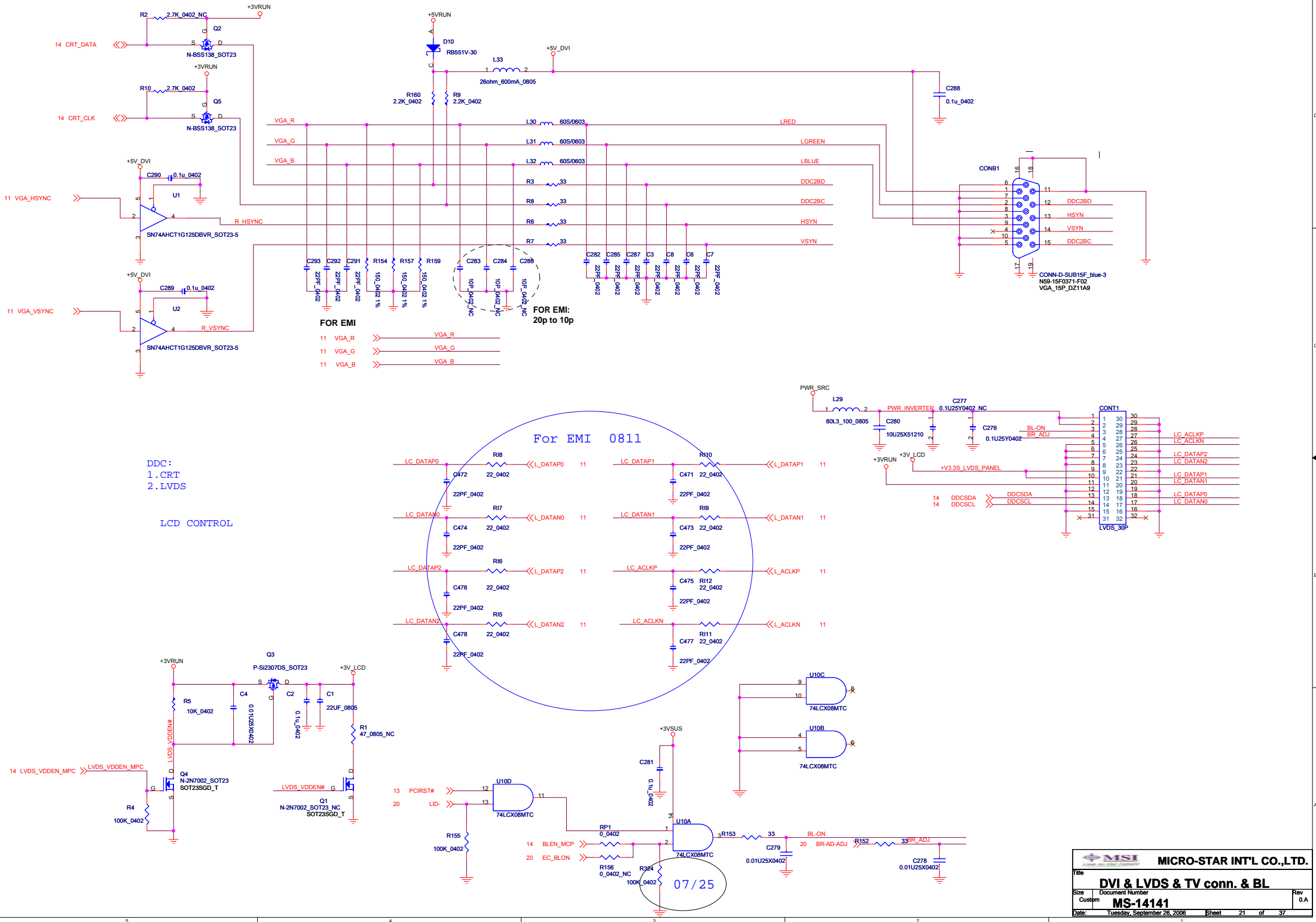


Delete Sch 3/06  
ISOLATION  
INTERNAL AMP &  
LINEOUT

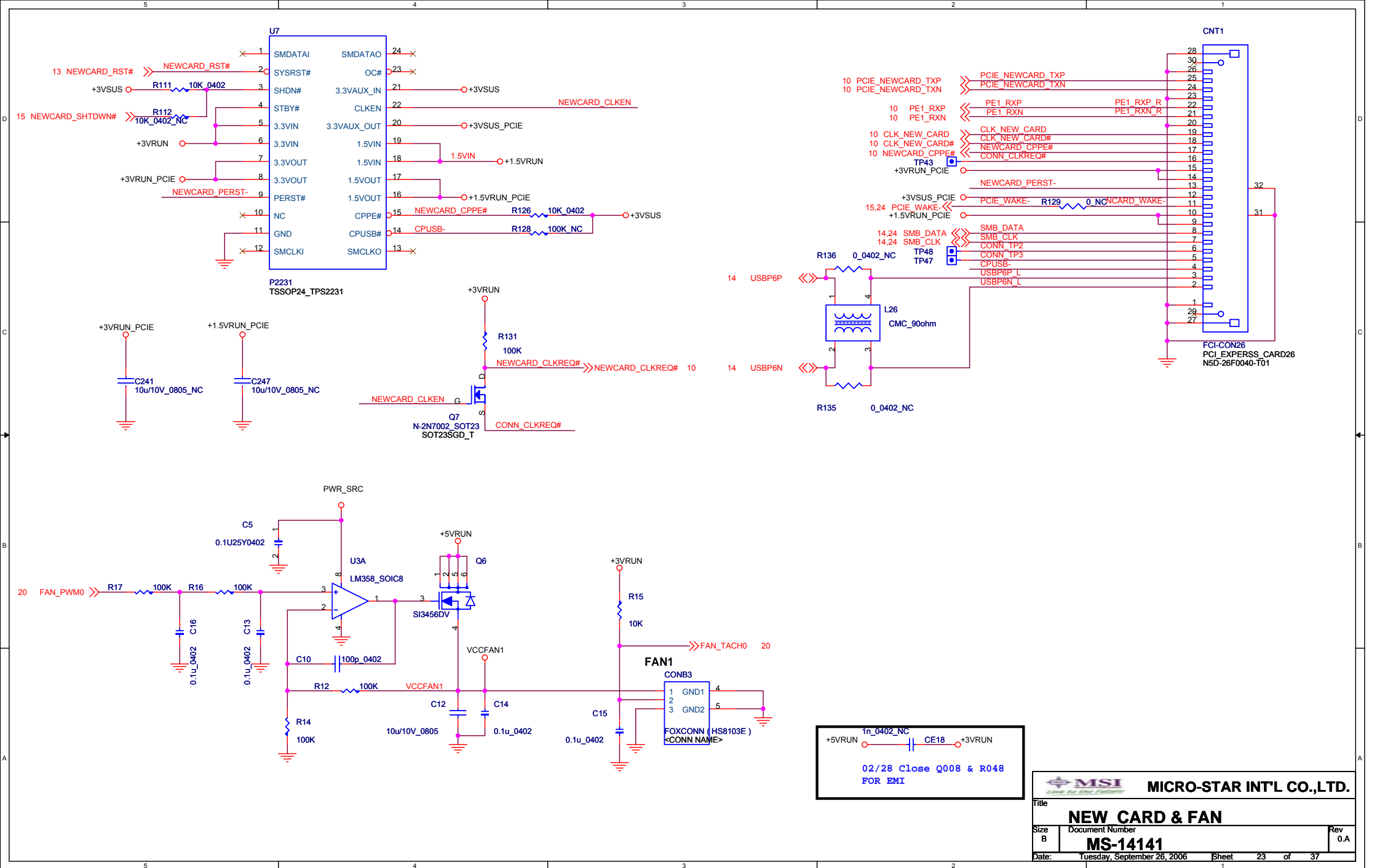


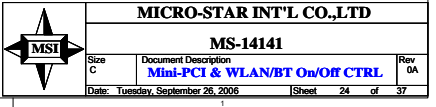


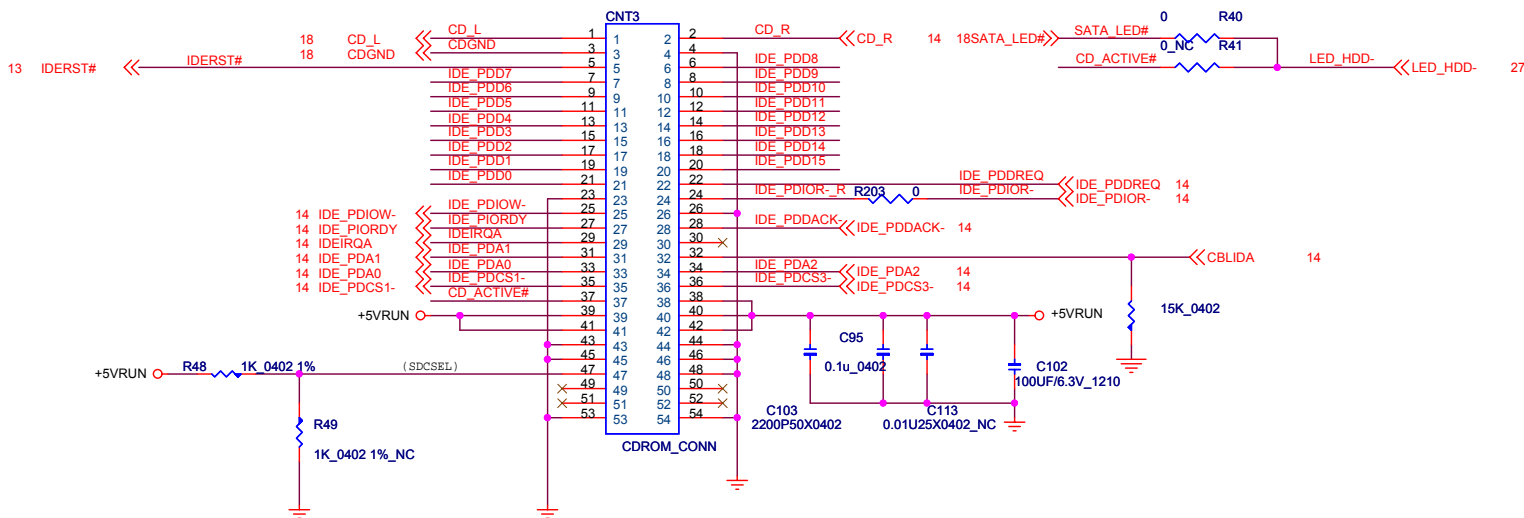
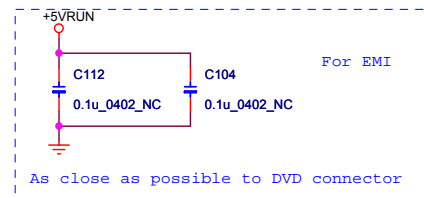
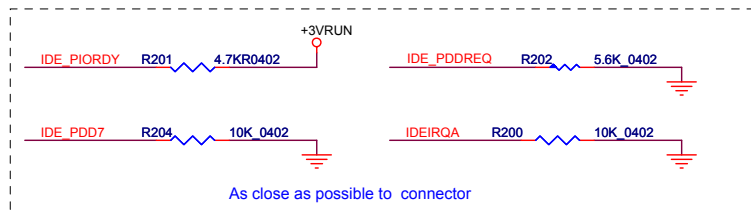
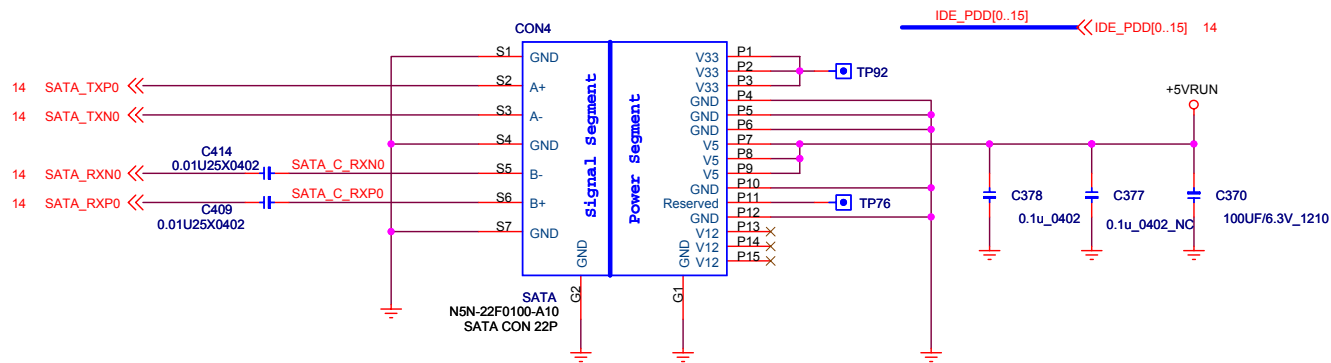






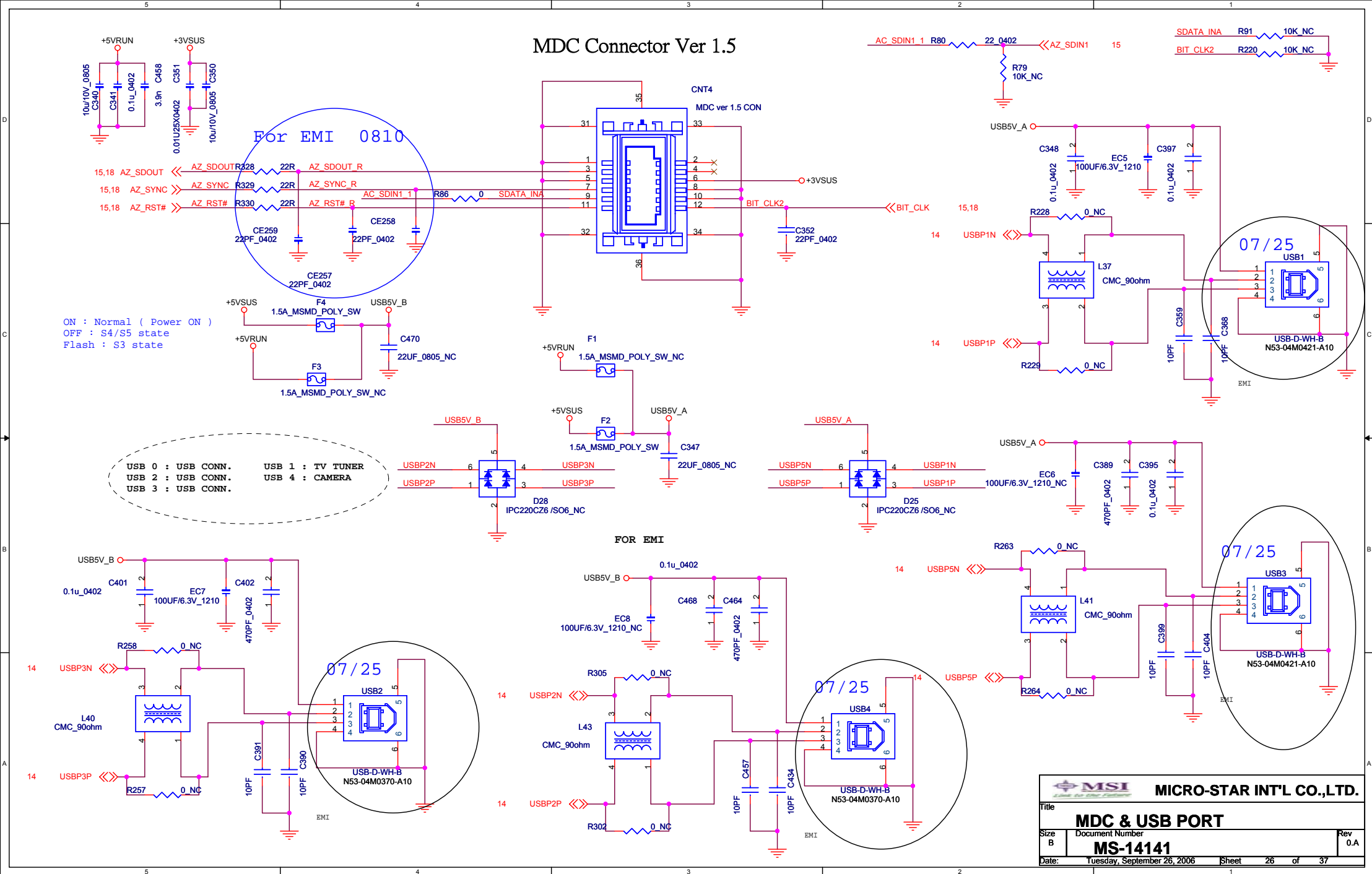




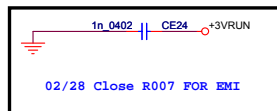
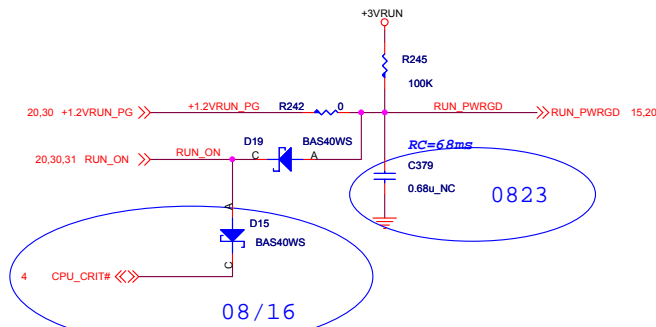
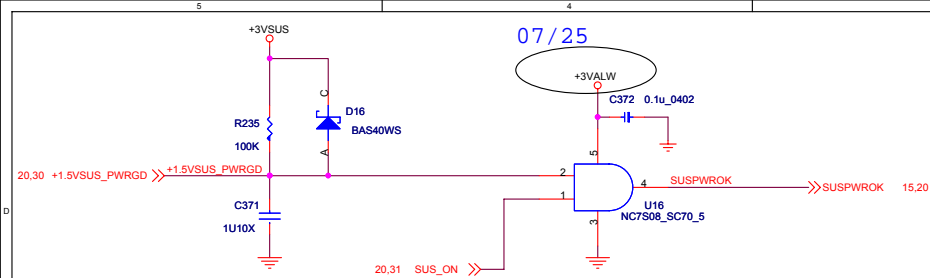


<b>MICRO-STAR INT'L CO.,LTD.</b>	
<b>Title</b> <b>HDD &amp; CDROM</b>	
<b>Size</b> B	<b>Document Number</b> <b>MS-14141</b>
<b>Date:</b> Tuesday, September 26, 2006	
Sheet 25 of 37	
Rev 0.A	

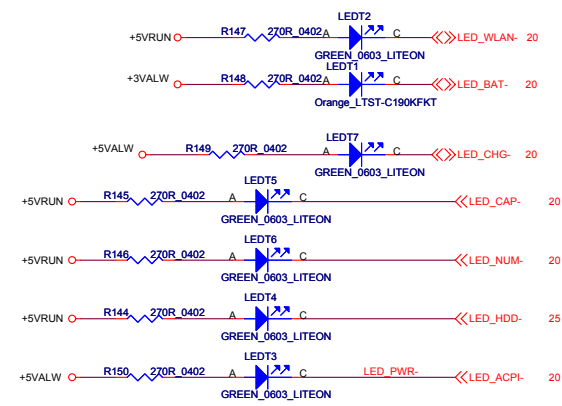
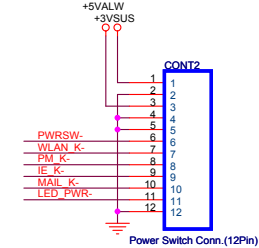
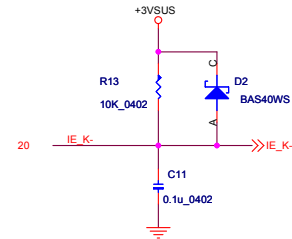
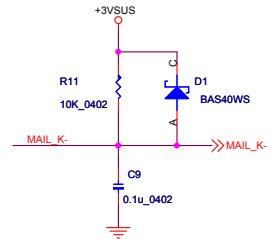
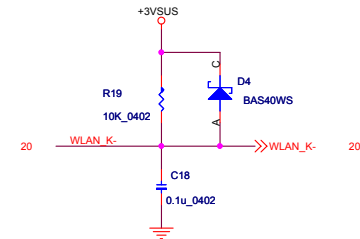
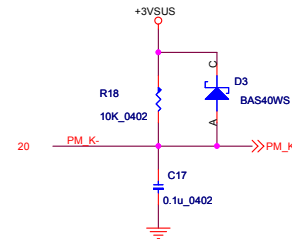
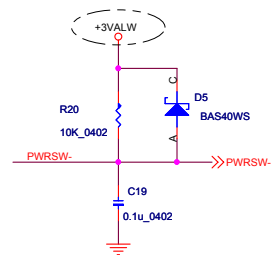
# MDC Connector Ver 1.5

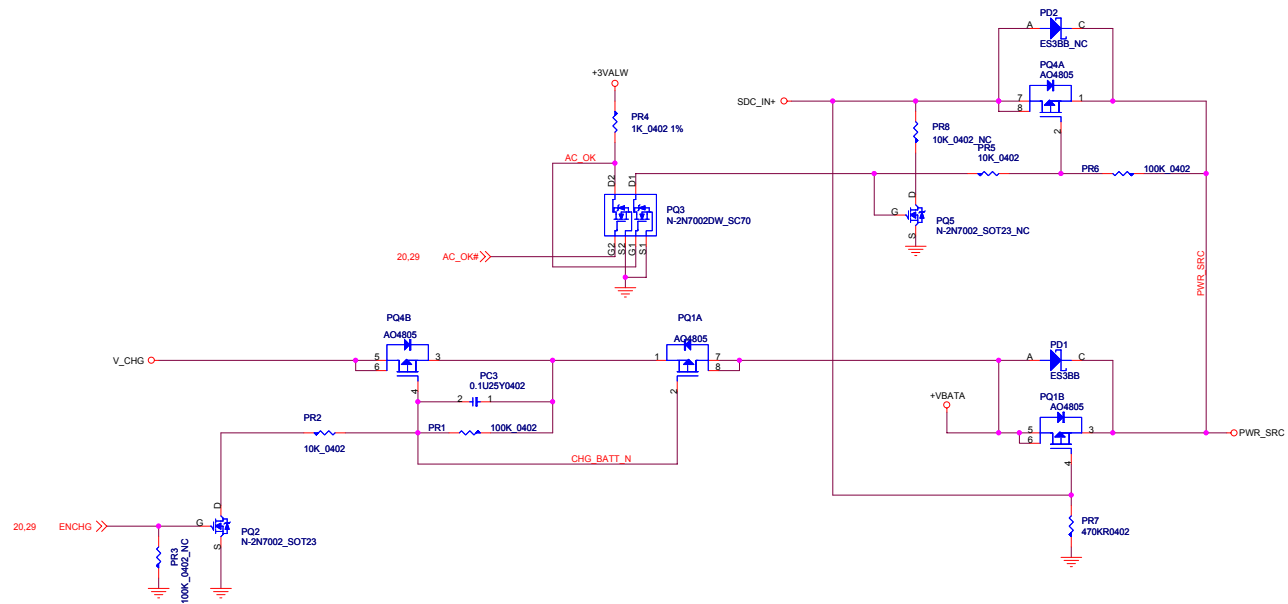
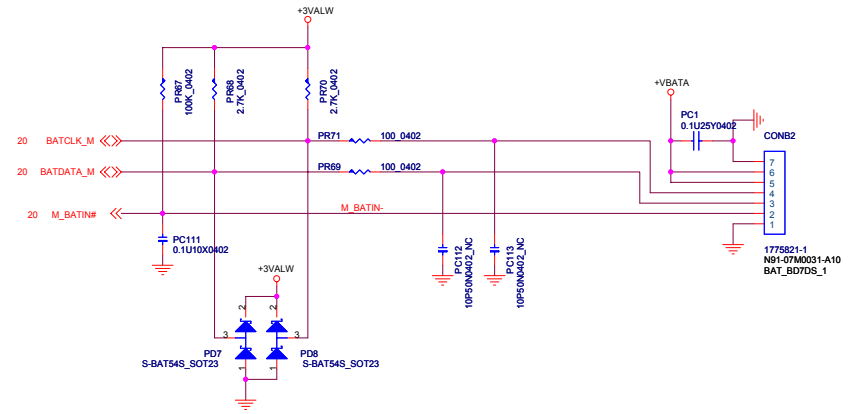
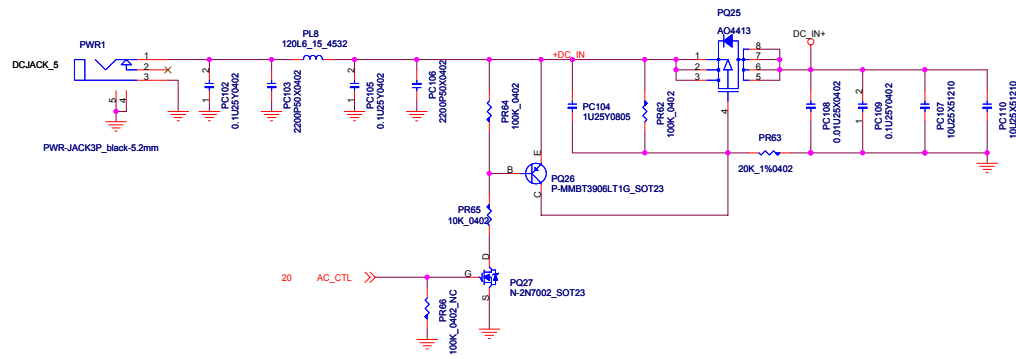






15,20 PM\_SLP\_S5# >> R279 0\_0402 VTT\_VDDIO\_EN >> VTT\_VDDIO\_EN 32











Current limit at 3.8A for SMDR\_VTERM

Current limit at 6A for +1.8VSUS

$$V_{out} = 1.5(1 + (R5/R9))$$

$$R5 = 10K, R9 = 49.9K$$

$$V_{out} = 1.8V$$

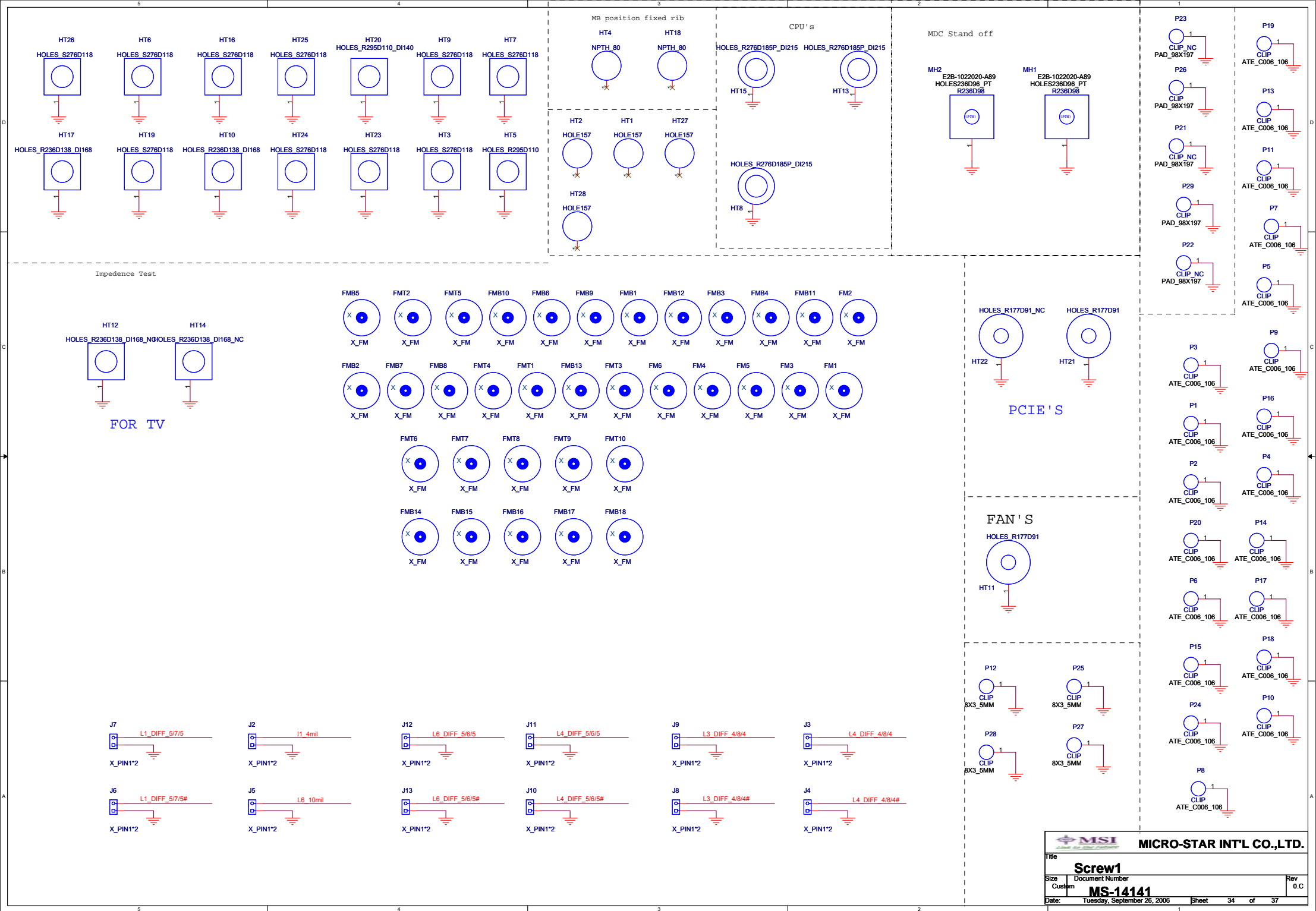
**+1.8VRUN**

2/18 add LDO +1.8VRUN (300mA) schematic

MSI MICRO-STAR INT'L CO.,LTD.			
Title			
DDR2 1.8V VTT 0.9V			
Size	Document Number		Rev
Custom	MS-14141		0.A
Date:	Tuesday, September 26, 2006	Sheet	32 of 37









South Brige AL FOIL\_NC



MDC\_Module\_NC



RJ45\_MYLAR



DDR\_MYLAR



M/B\_MYLAR



HD\_MYLAR



HD\_MYLAR



Screw



Screw



Screw



Screw



PCB1



Screw



Screw



Screw



Screw



Screw



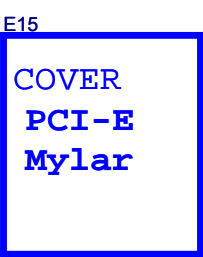
RTC battery



HD\_MYLAR




PCI-EXPRESS-CARD  
E23-1016011-T01



PCI-E\_MYLAR



BIOS\_LABEL\_NC

				<b>MICRO-STAR INT'L CO.,LTD.</b>			
Title <b>Screw2</b>							
Size A		Document Number <b>MS-14141</b>					Rev 0.C
Date:		Tuesday, September 26, 2006		Sheet	35	of	37



- History 0A--> 0B
- 1.P14. correct CNB1 RTC Batt . RTCVCC and GND pin define for Con type from Horizoutally to Vertically
  - 2.P26. correct USB 1,2,3,4 pin define 5V,GND,D+,D-
  - 3.P27. correct U16 power source from +3VSUS to +3VALW
  - 4.P21. correct U10A pin2 pull down 100K to avoid LCD white Screen on boot intial.
  - 5.P18. correct Q19 D1 D2 short together with Front\_out\_R\_ISO and Front \_out L\_ISO
  - 6.P4. correct R190,191,192,193,194 power source from +1.8VRUN to CPU\_VDDIO\_SUS
  - 7.P19. correct c432 bypass Cap. from 10U to 0.47U.
  - 8.P21. EMI change COM choke to RC for LVDS signal
  - 9.P26. EMI change add 0R for AZ\_SDOOUT,SYNC,RST for test
  - 10.P27 Shit D15 from CRTL SUSPWROK to RUN\_PWRGD for LM86 CPU\_Crit# to shutdown system power and programe by EC at 105C
  - 11.P30,P31,P32, Cancel ALL power GAP G1,G2,G3,G4,G5,G6,G7 to Short.