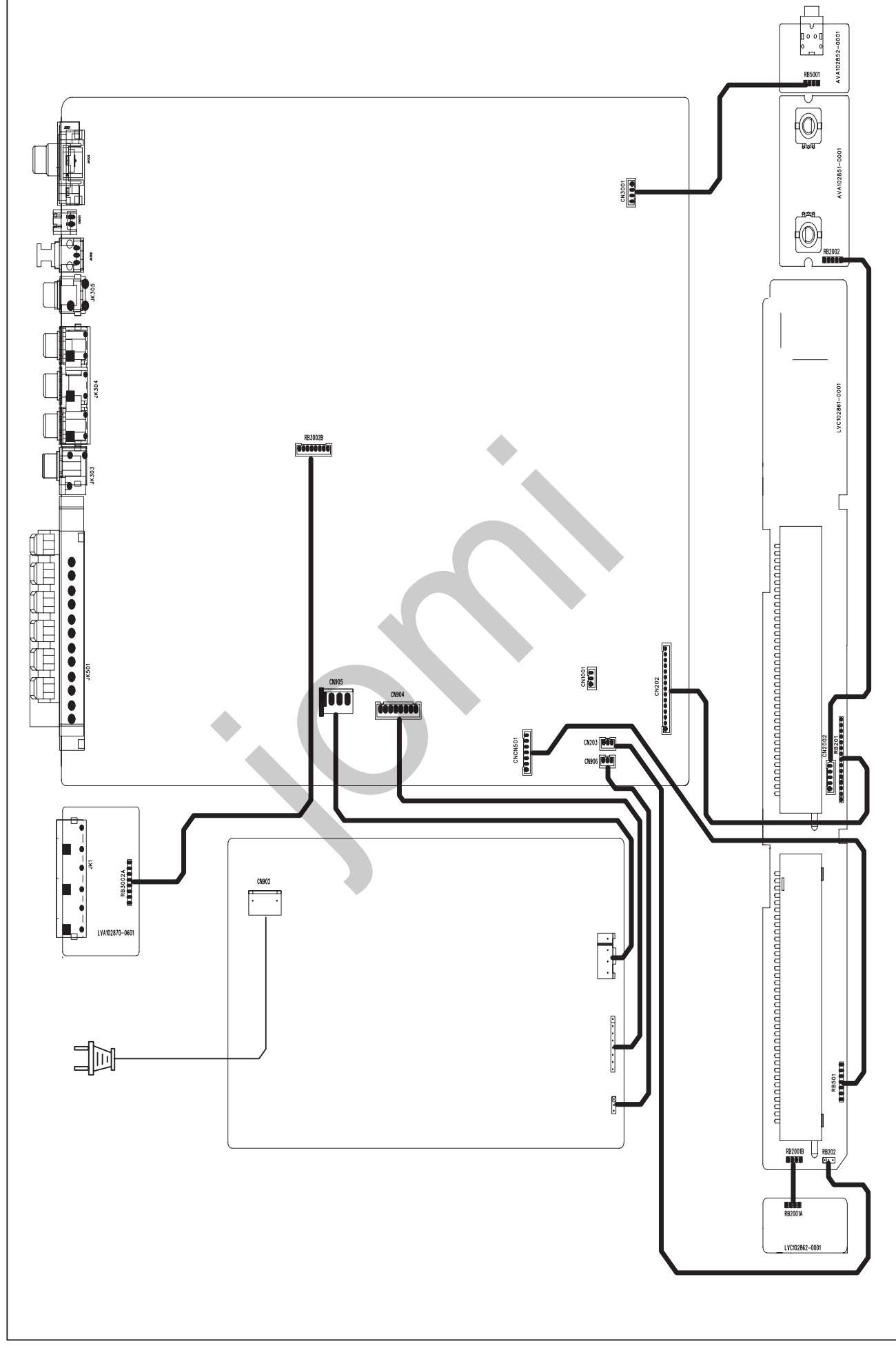


## 4-1



## WIRING DIAGRAM

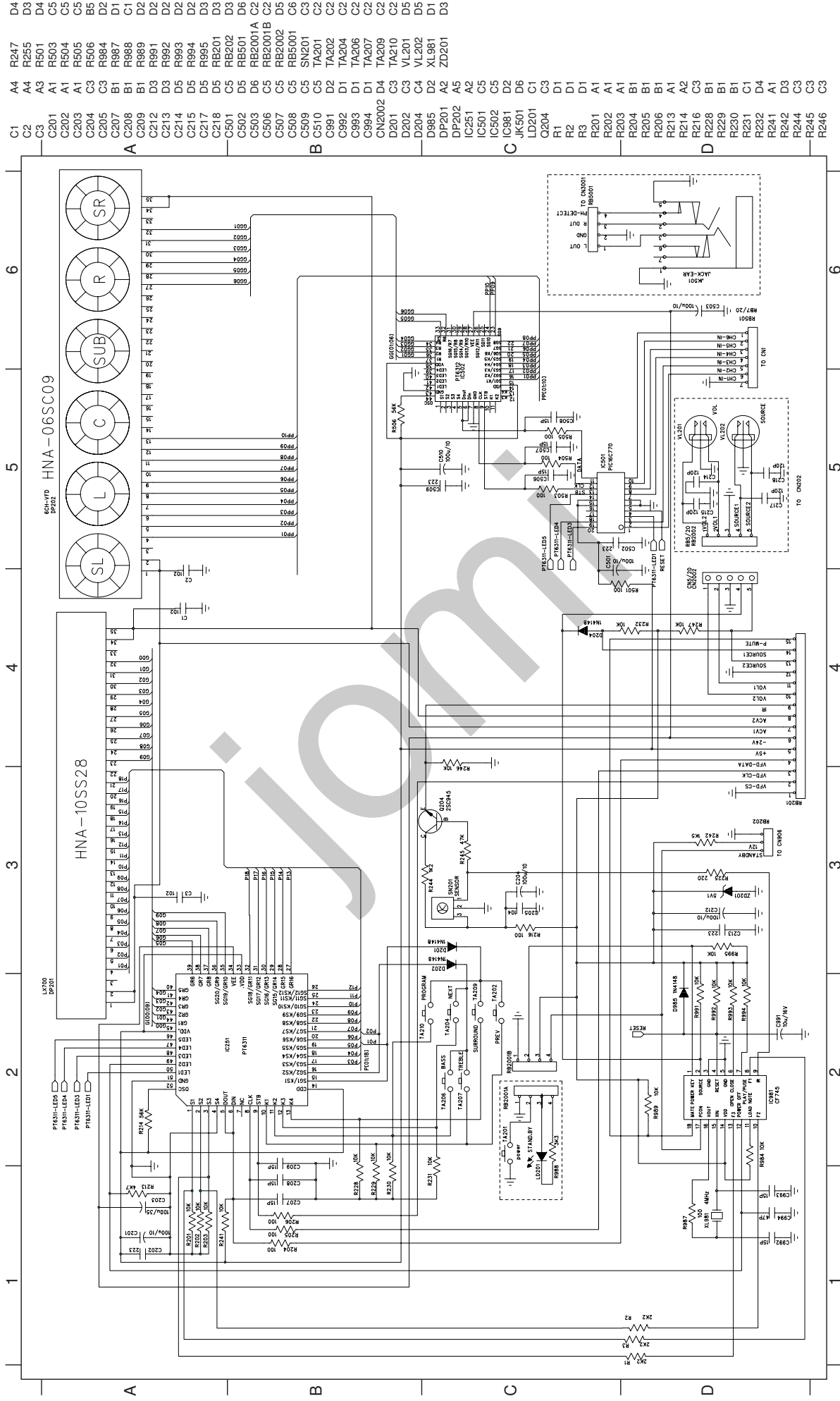




CIRCUIT DIAGRAM

5-2

5-2



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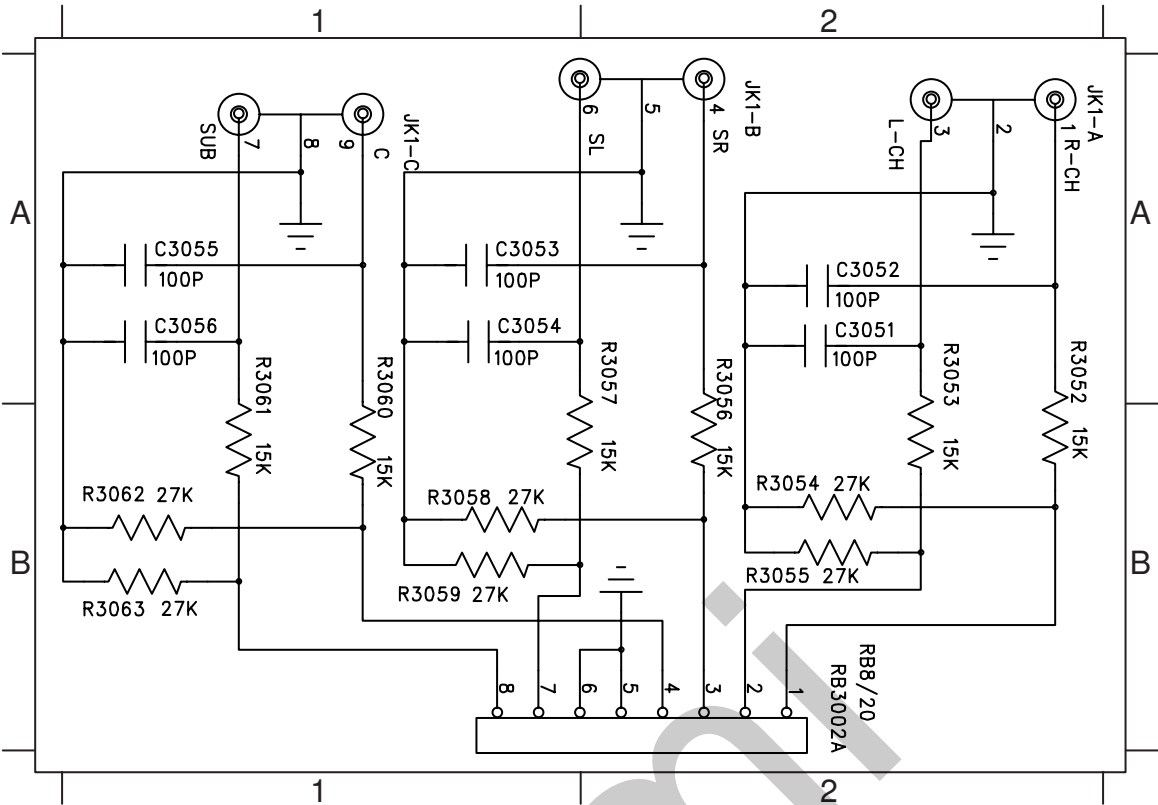
# SOURCE + PHONE / 6 CH IN BOARD

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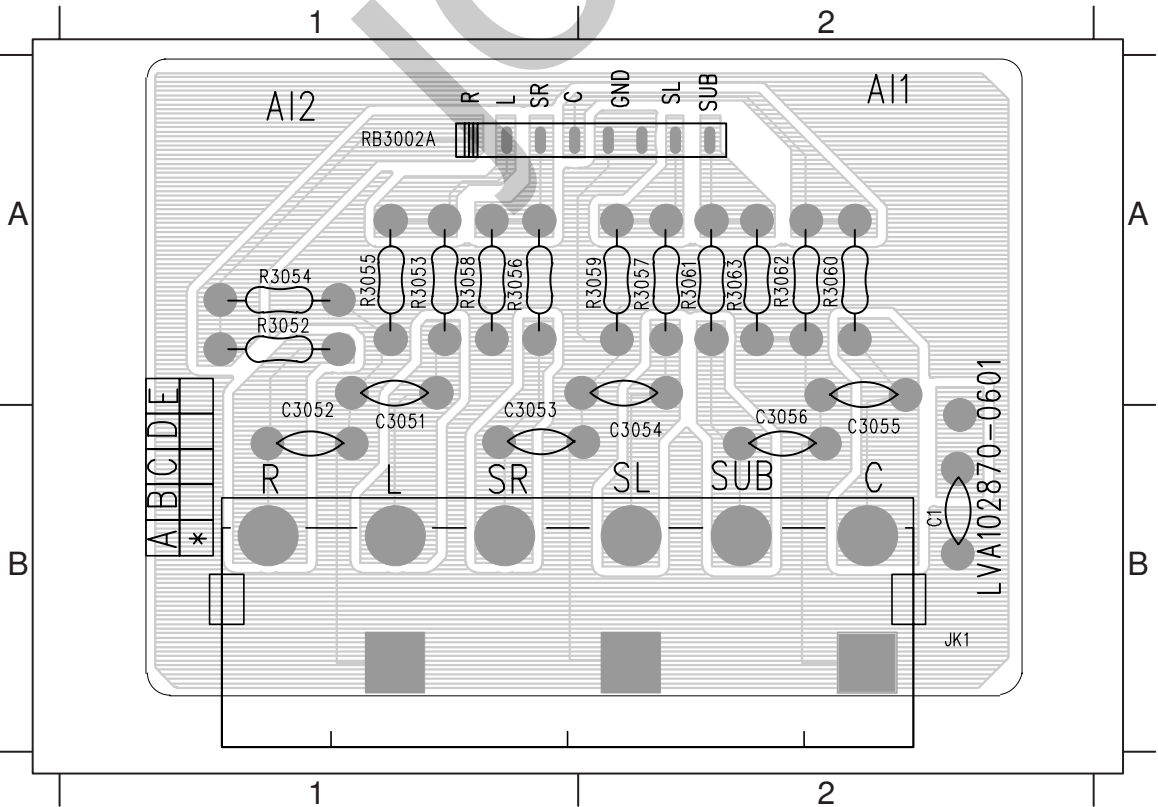
Source + Phone Circuit Diagram .....	6-2
Source + Phone PCB Layout .....	6-2
6 CH IN Circuit Diagram .....	6-3
6 CH IN PCB Layout .....	6-3
Electrical Parts List(Source + Phone / 6CH IN) .....	6-4

CIRCUIT DIAGRAM - 6 CH IN PCB



C3051	A2
C3052	A2
C3053	A1
C3054	A1
C3055	A1
C3056	A1
JK1-A	A2
JK1-B	A2
JK1-C	A1
R3052	A2
R3053	A2
R3054	B2
R3055	B2
R3056	A2
R3057	A2
R3058	B1
R3059	B1
R3060	A1
R3061	A1
R3062	B1
R3063	B1
RB3002A	B2

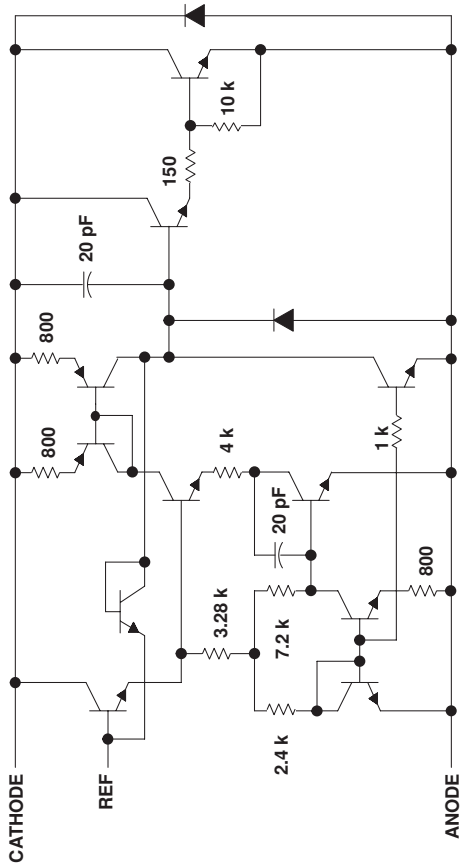
PCB LAYOUT - 6 CH IN PCB



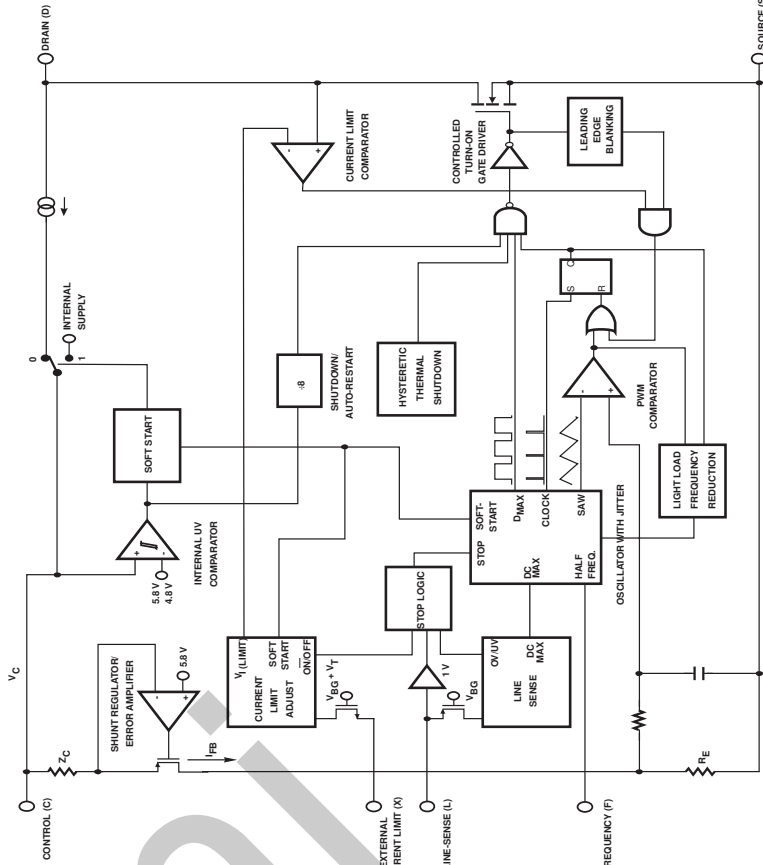
C1	B2
C3051	B1
C3052	B1
C3053	B1
C3054	B2
C3055	B2
C3056	B2
JK1	B2
R3052	A1
R3053	A1
R3054	A1
R3055	A1
R3056	A1
R3057	A2
R3058	A1
R3059	A2
R3060	A2
R3061	A2
R3062	A2
R3063	A2
RB3002A	A1

# POWER BOARD

TL431 EQUIVALENT SCHEMATIC



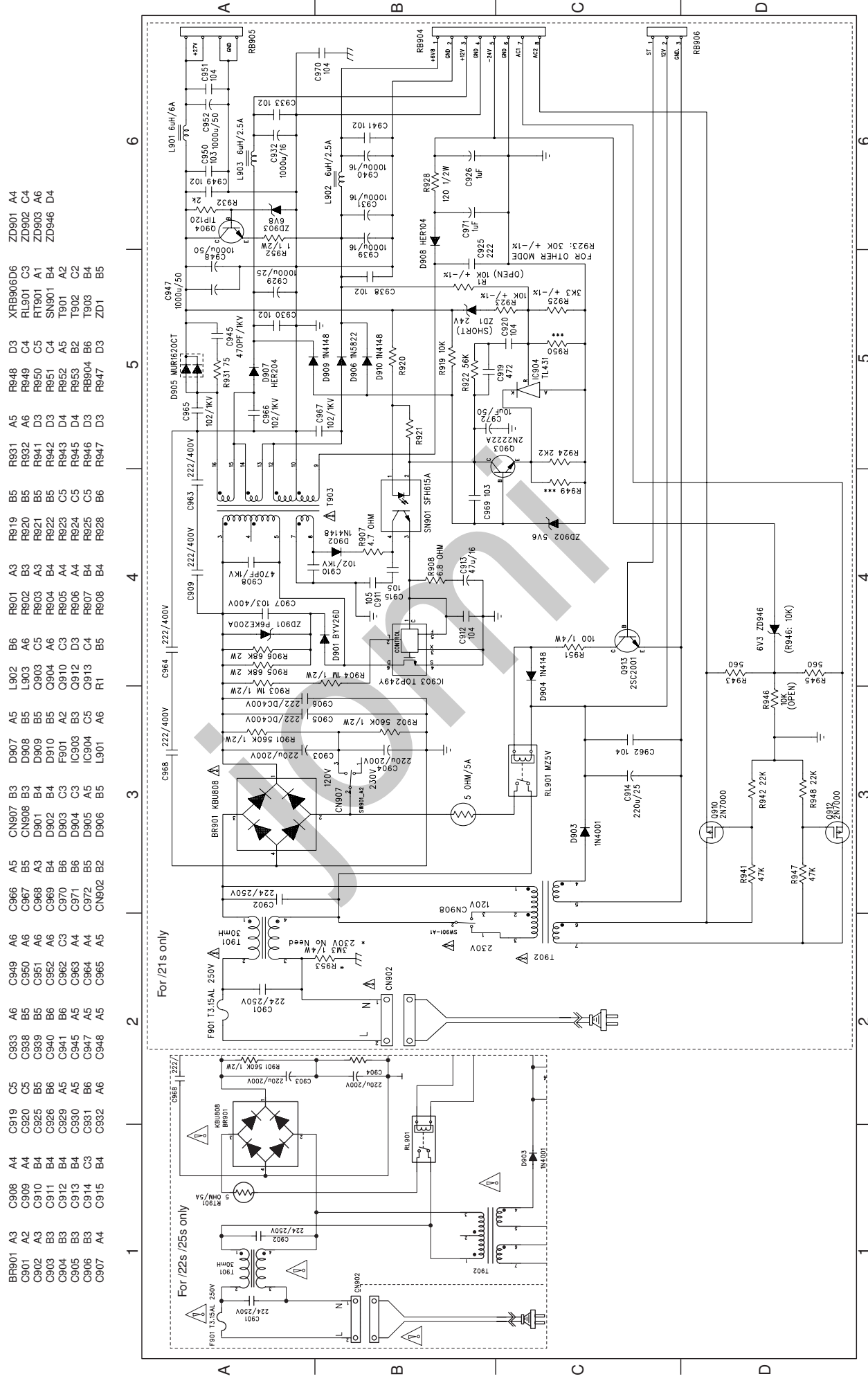
TOP249 BLOCK DIAGRAM



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Circuit Diagram .....	7-2
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Electrical Parts List.....	7-4

## CIRCUIT DIAGRAM





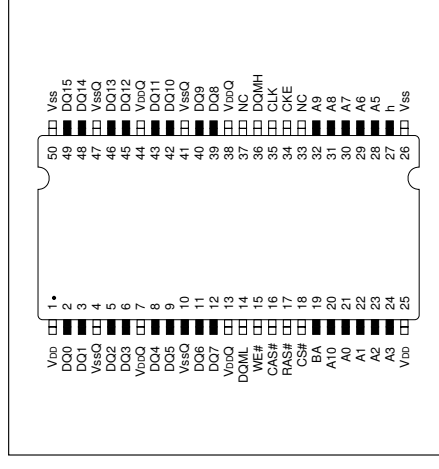
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PCB Layout(Component View) .....	8-10
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### 2131 INTERNAL IC DIAGRAM

**SYNCHRONOUS DRAM**  
**1MX16Y3VTW**

## PIN ASSIGNMENT (Top View)

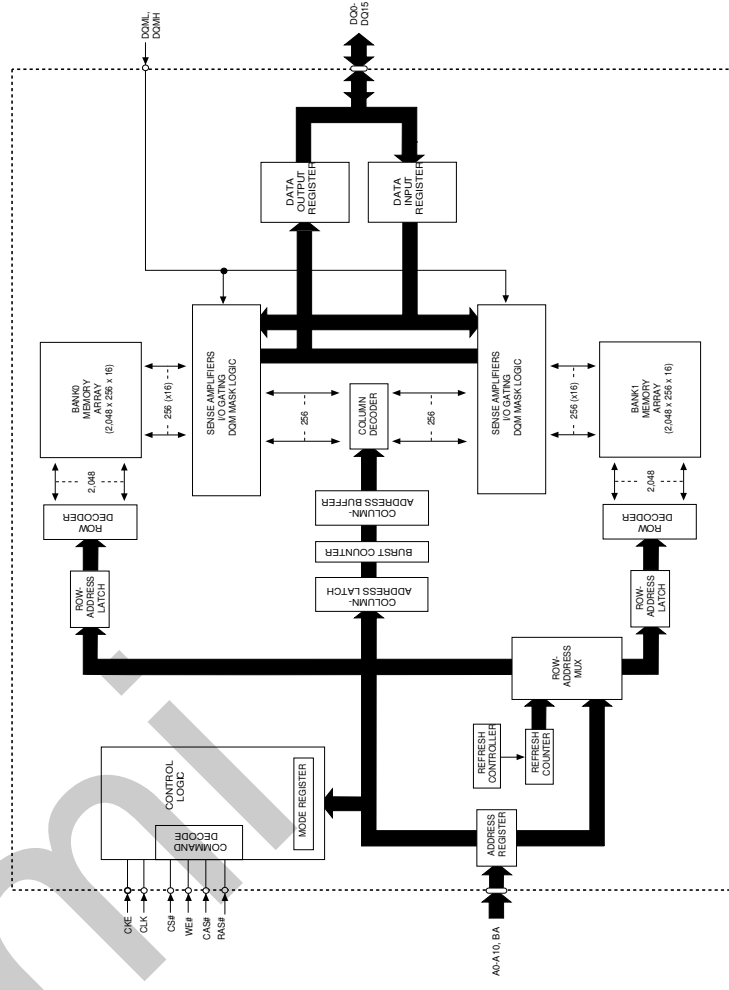
### 50 - Pin TSOP



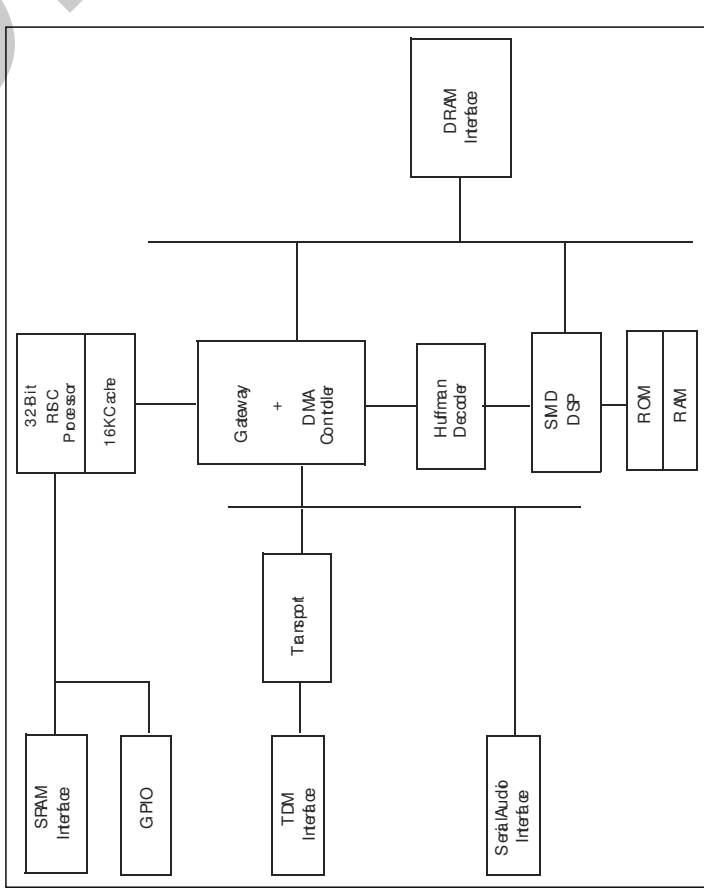
**Note:** The # symbol indicates signal is active LOW.

	1 Meg x 16
Configuration	512Kx16x2banks
Refresh Count	2K or 4K
Row Addressing	2K (A0-A10)
Bank Addressing	2 (BA)
Column Addressing	256 (A0-A7)

## FUNCTIONAL BLOCK DIAGRAM

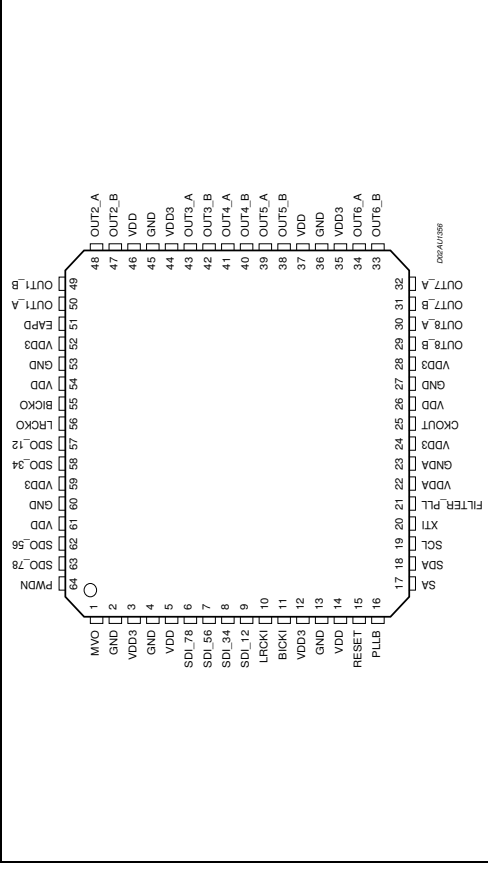


## ESS4008 INTERNAL IC DIAGRAM

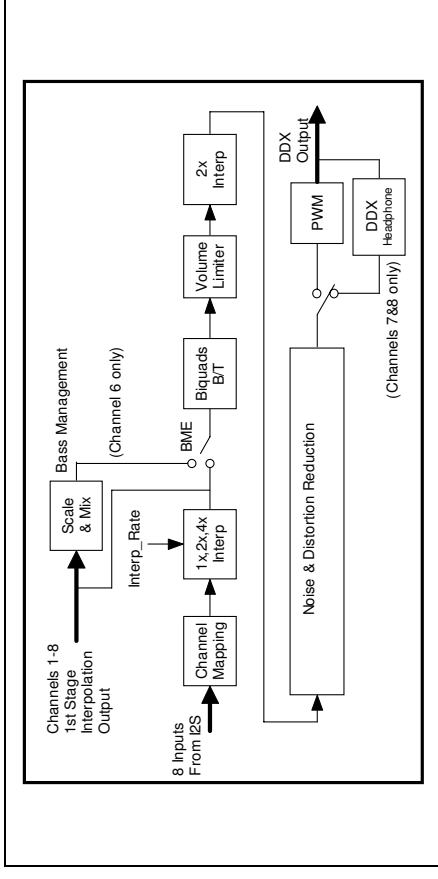


# DIGITAL AUDIO PROCESSOR STA308

### PIN CONNECTION (Top view)



## SIGNAL FLOW DIAGRAM



PIN	NAME	TYPE	DESCRIPTION	PAD TYPE
1	MVO	I	Master Volume Override	CMOS Input Buffer with Pull-Down
3, 12, 24, 28, 35, 44, 52, 59	VDD3		3.3V Digital Supply	3.3V Digital Power
2, 4, 13, 27, 36, 45, 53, 60	GND		Digital Ground	Supply Voltage (pad ring)
5, 14, 26, 37, 46, 54, 61	VDD		2.5V Digital Supply	2.5V Digital Power
6	SDI_78	I	Input I2S Serial Data Channels 7 & 8	5V Tolerant TTL Input Buffer
7	SDI_56	I	Input I2S Serial Data Channels 5 & 6	5V Tolerant TTL Input Buffer
8	SDI_34	I	Input I2S Serial Data Channels 3 & 4	5V Tolerant TTL Input Buffer
9	SDI_12	I	Input I2S Serial Data Channels 1 & 2	5V Tolerant TTL Input Buffer
10	LRCCK	I	Inputs I2C Left/Right Clock	5V Tolerant TTL Input Buffer
11	BICKI	I	Inputs I2C Serial Clock	5V Tolerant TTL Input Buffer
15	RESET	I	Global Reset	5V Tolerant TTL Schmitt Trigger Input Buffer
16	PLL_B	I	PLL Bypass	CMOS Input Buffer with Pull-Down
17	SA	I	Select Address (I2C)	CMOS Input Buffer with Pull-Down
18	SDA	I/O	I2C Serial Data	Bidirectional Buffer: 5V Tolerant TTL Schmitt Trigger Input; 3.3V Capable 2 mA
19	SCL	I	I2C Serial Clock	Slew-rate control Output; 5V Tolerant TTL Schmitt Trigger Input Buffer

OCTAL BUFFER / LINE DRIVER  
74HCT244

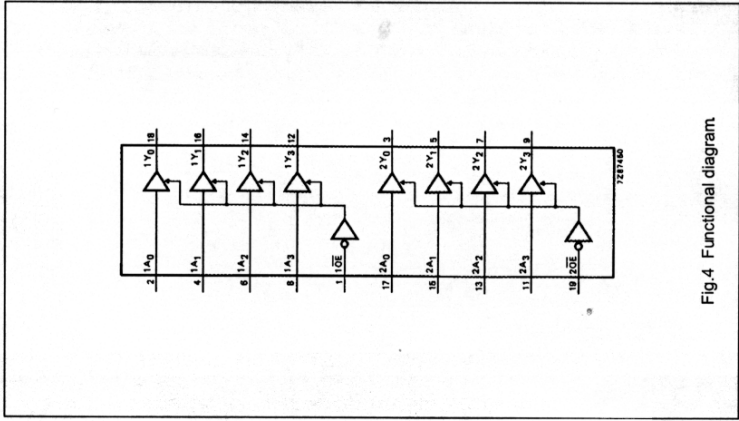
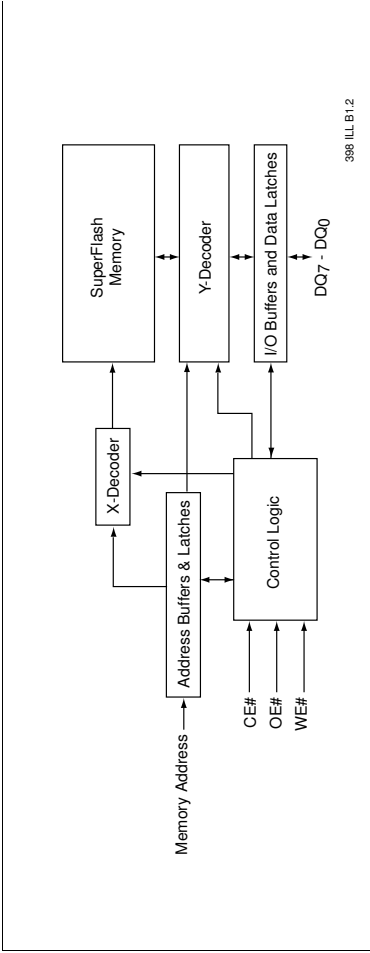


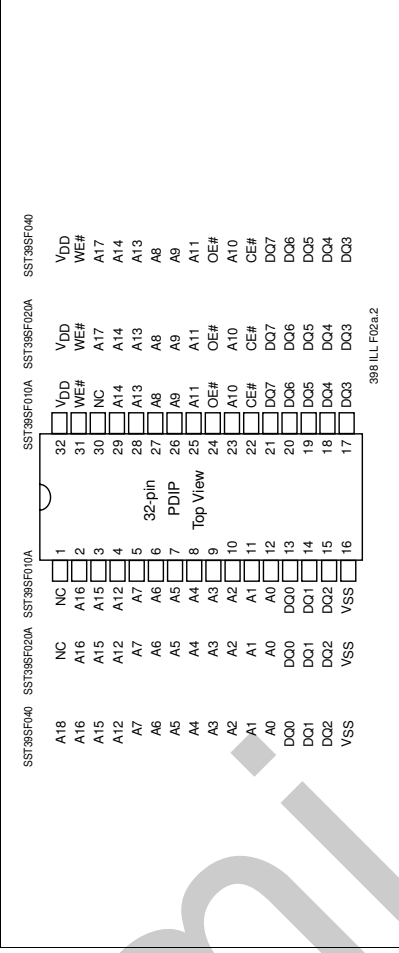
Fig.4 Functional diagram

MULTI-PURPOSE FLASH  
SST39SF020A

FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENTS FOR 32-PIN PDIP

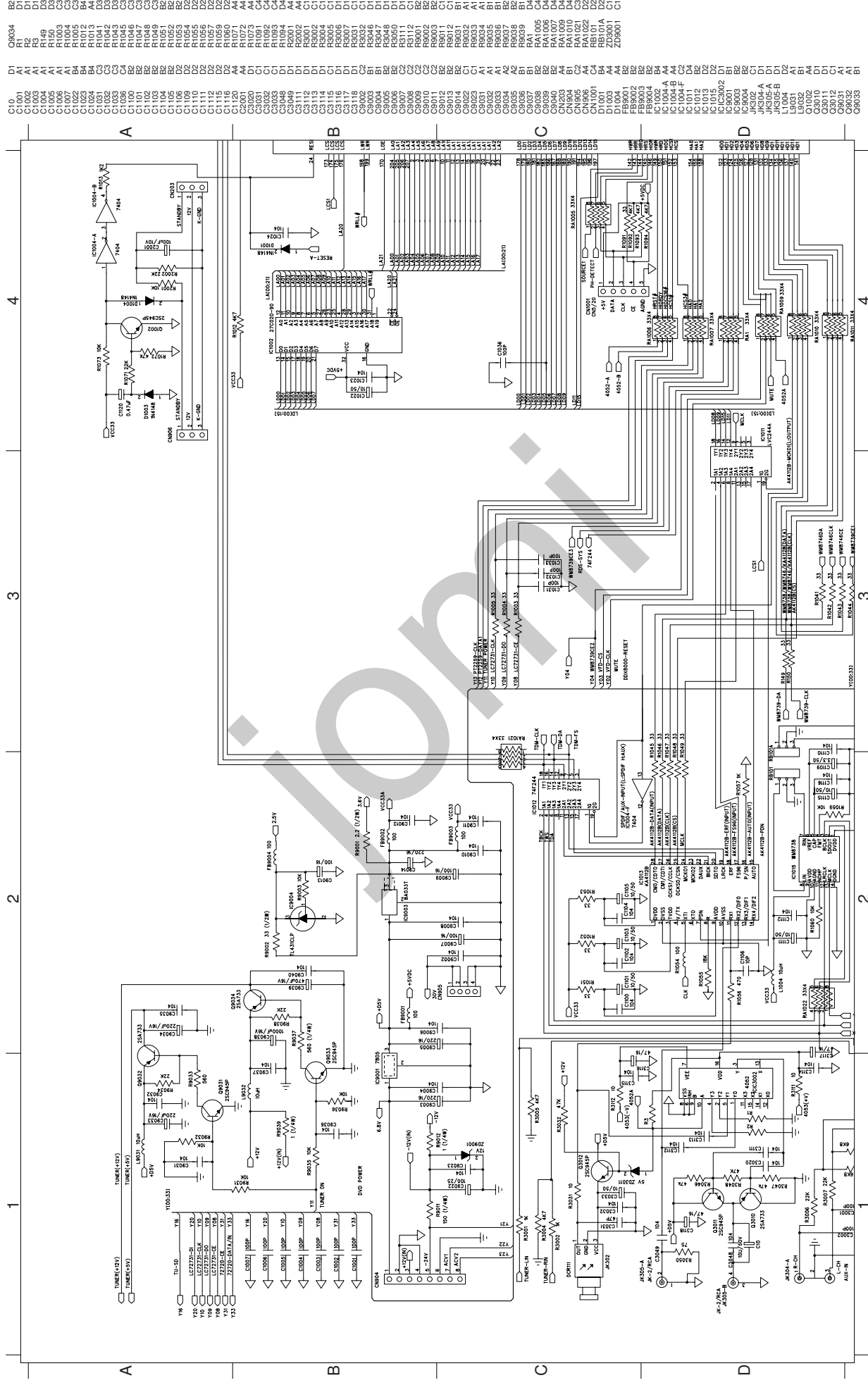


PIN DESCRIPTION

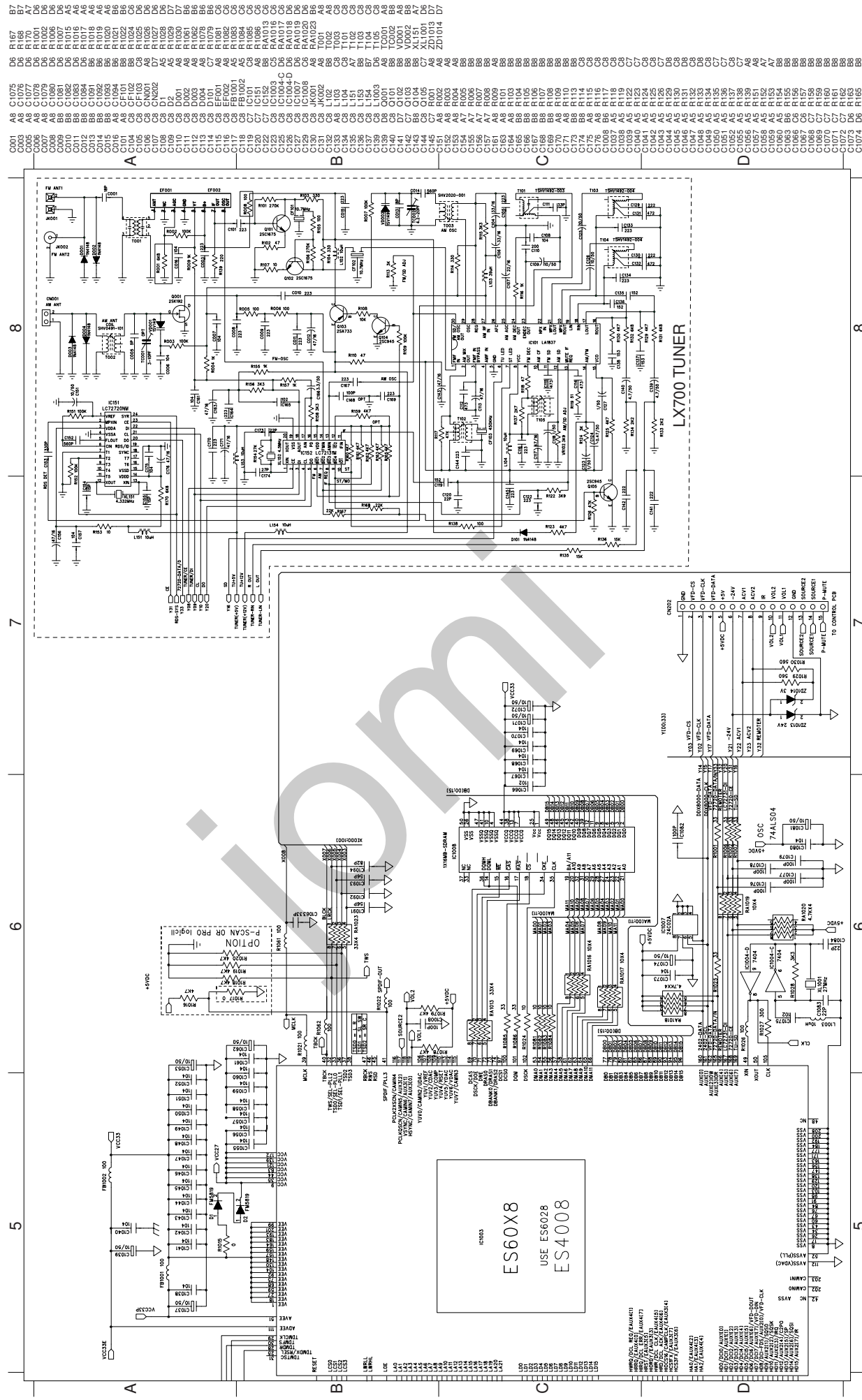
Symbol	Pin Name	Functions
$A_{MS}^{-1}A_0$	Address Inputs	To provide memory addresses. During Sector-Erase $A_{MS}$ - $A_{12}$ address lines will select the sector.
DQ7-DQ0	Data Input/output	To output data during Read cycles and receive input data during Write cycles. Data is internally latched during a Write cycle. The outputs are in tri-state when OE# or CE# is high.
CE#	Chip Enable	To activate the device when CE# is low.
OE#	Output Enable	To gate the data output buffers.
WE#	Write Enable	To control the Write operations.
VDD	Power Supply	To provide 5.0V supply (4.5-5.5V)
VSS	Ground	
NC	No Connection	Unconnected pins.

1.  $A_{MS}$  = Most significant address  
 $A_{MS}$  =  $A_{16}$  for SST39SF010A,  $A_{17}$  for SST39SF020A, and  $A_{18}$  for SST39SF040

## CIRCUIT DIAGRAM (TOP LEFT)



### CIRCUIT DIAGRAM (TOP RIGHT)



**CIRCUIT DIAGRAM (BOTTOM LEFT)**

