LG Electronics Inc.

SERVICE MANUAL MODEL: TCH-M550

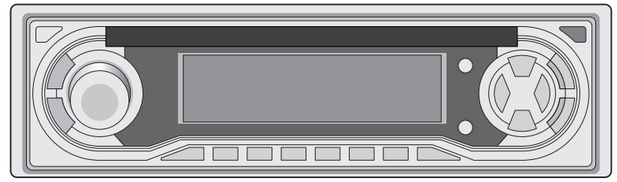
LG

DETACHABLE FRONT PANEL CAR CD RECEIVER

SERVICE MANUAL

CAUTION

BEFORE SERVICING THE UNIT, READ THE “SAFETY PRECAUTIONS” IN THIS MANUAL.



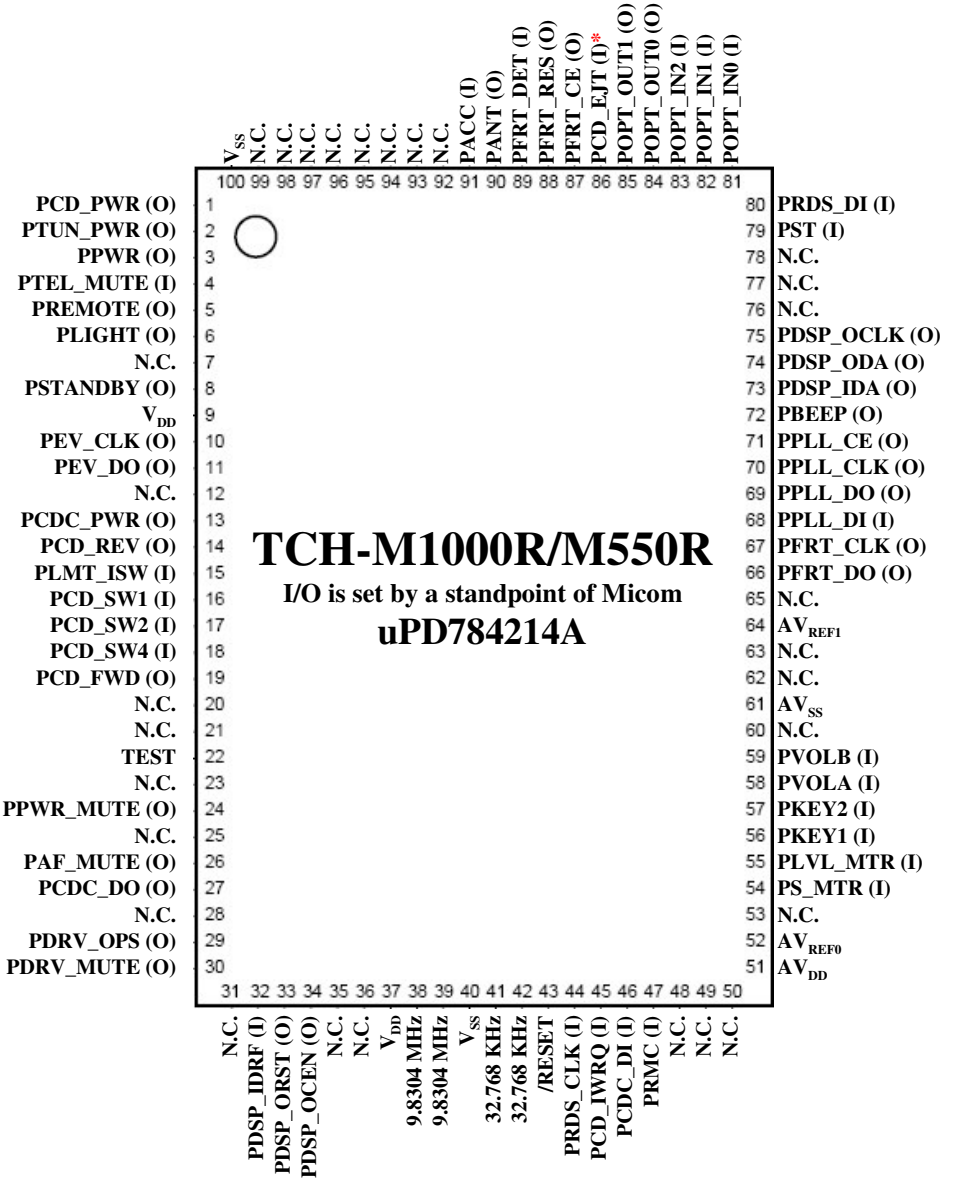
MODEL : TCH-M550

LG Electronics Inc.

❑ INTERNAL BLOCK DIAGRAM of ICs

■ IC401 uPD784214A

1) PORT ASSIGNMENT



* : TCH-M1000R only

Download Pin:

CLK : 38 pin (X1)

V_{PP} : 22pin (TEST/VPP)

V_{DD} : 9 pin (VDD), 37 pin (VDD), 51 pin (AVDD)

RESET : 43 pin (/RESET)

SCK : 67 pin (/SCK2)

SO : 66 pin (SI2)

SI : 65 pin (SOS2)

GND : 40 pin (VSS), 100 pin (VSS), 61 pin (AVSS)

2) PORT DESCRIPTION

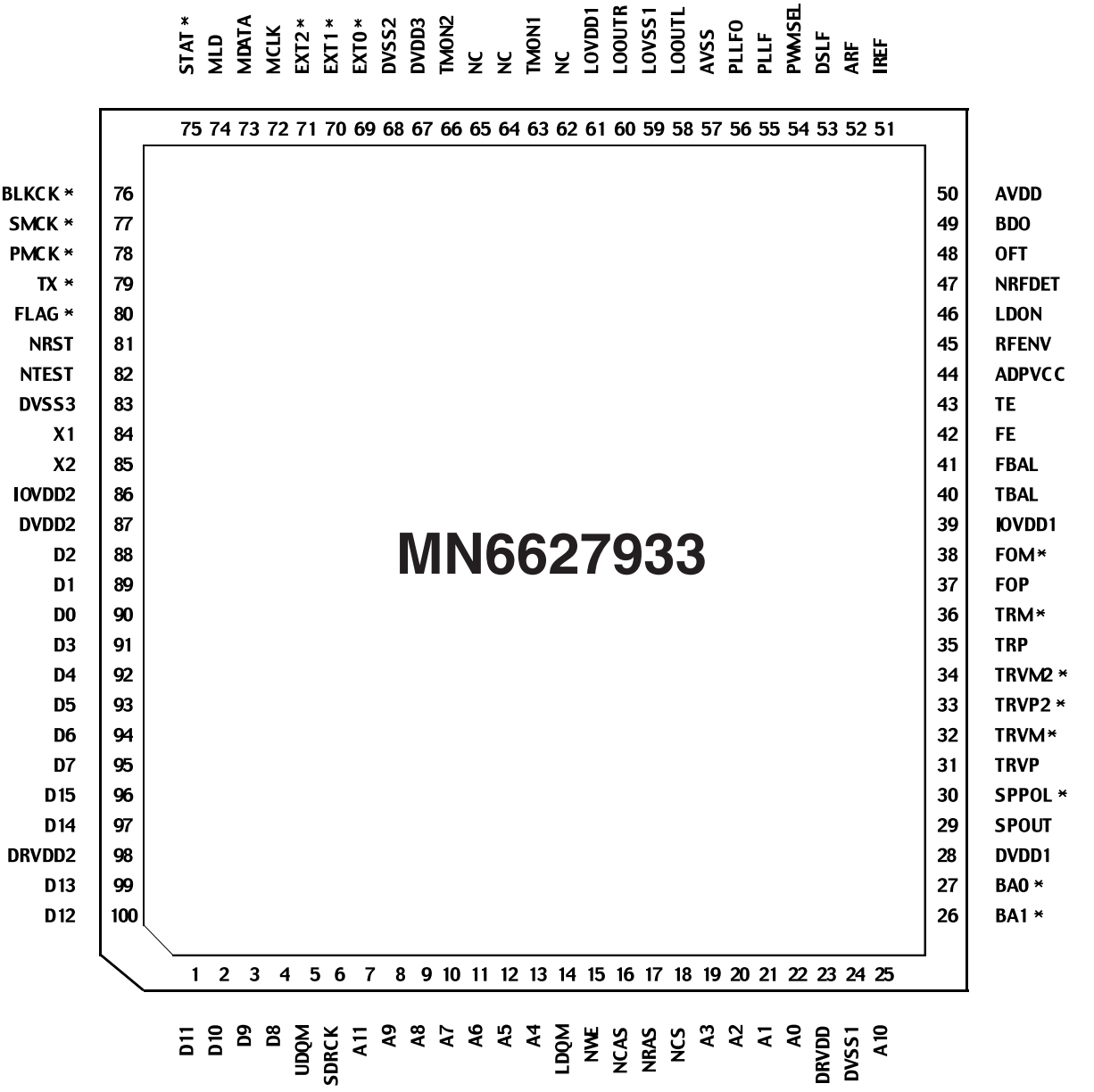
Pin	Name in Micom	Name in Model	Enable I/O	I/O setted	Output Format	Descripation
1	P60/A16	PCD_PWR	I/O	O	CMOS	DSP power suppler ON output
2	P61/A17	PTUN_PWR	I/O	O	CMOS	Tuner power supplier ON output
3	P62/A18	PPWR	I/O	O	CMOS	System power supplier ON output
4	P63/A19	PTEL_MUTE	I/O	I	-	Telephone mute input
5	P64/RD	PREMOTE	I/O	O	CMOS	External power amplifier enable output
6	P65/WR	PLIGHT	I/O	O	CMOS	LCD backlight ON output
7	P66/WAIT	N.C.	I/O	O	CMOS	Not to be used (Open)
8	P67/ASTB	PSTANDBY	I/O	O	CMOS	To power amp, "STADN-BY" command output
9	VDD	VDD	-	-	-	Positive power supply
10	P100/T15TO5	PEV_CLK	I/O	O	CMOS	Clock for interface with volume controller
11	P101/T16/TO6	PEV_DO	I/O	O	CMOS	To volume controller, data output
12	P102/T17/TO7	N.C.	I/O	O	CMOS	Not to be used (Open)
13	P103/T18/TO8	PCDC_PWER	I/O	O	CMOS	CD changer power supplier ON output
14	P30/TO0	PCD_REV	I/O	O	CMOS	In MD, load motor "reverse" command output
15	P31/TO1	PLMT_ISW	I/O	I	-	In MD, limit switch state input
16	P32/TO2	PCD_SW1	I/O	I	-	In MD, SW1 state input
17	P33/TI1	PCD_SW2	I/O	I	-	In MD, SW2 state input
18	P34/TI2	PCD_SW4	I/O	I	-	In MD, SW4 state input
19	P35/TI100	PCD_FWD	I/O	O	CMOS	In MD, load motor "forward" command output
20	P36/T101	N.C	I/O	O	CMOS	Not to be used (Open)
21	P37/EXA	N.C	I/O	O	CMOS	Not to be used (Open)
22	TEST/VPP	TEST	-	-	-	pull down (470 ~ 10k)
23	P90	N.C	I/O	O	N-ch	Not to be used (Open)
24	P91	PPWR_MUTE	I/O	O	N-ch	To power amp, "Mute" command output
25	P92	N.C	I/O	O	N-ch	Not to be used (Open)
26	P93	PAF_MUTE	I/O	O	N-ch	To tuner pack, AF mute output
27	P94	PCD_IDO	I/O	O	N-ch	To CD changer, data output
28	P95	N.C	I/O	O	N-ch	Not to be used (Open)
29	P120/RTP0	PDRV_OPS	I/O	O	CMOS	In MD, motor driver's power save command output
30	P121/RTP1	PDRV_OMUTE	I/O	O	CMOS	In MD, all motor's output "cut off" command output
31	P122/RTP2	N.C	I/O	O	CMOS	Not to be used (Open)
32	P123/RTP3	PDSP_IDRF	I/O	I	-	Focusing OK signal input
33	P124/RTP4	PDSP_ORST	I/O	O	CMOS	DSP reser output
34	P125/RTP5	PCD_OCEN	I/O	O	CMOS	DSP chip enable output
35	P126/RTP6	N.C	I/O	O	CMOS	Not to be used (Open)
36	P127/RTP7	N.C	I/O	O	CMOS	Not to be used (Open)
37	VDD	VDD	-	-	-	Positive power supply (+5V)
38	X2	X2	-	-	-	X'tal 9.8304MHz
39	X1	X1	I	-	-	X'tal 9.8304MHz
40	VSS	GND	-	-	-	Ground
41	XT2	XT2	-	-	-	Sub clock 32.768kHz
42	XT1	XT1	I	-	-	Sub clock 32.768kHz
43	/RESET	RESET	I	-	-	System reser input
44	P00/INTP0	PRDS_CLK	I/O	I	-	From tuner pack, RDS clock input
45	P01/INTP1	PCD_IWRQ	I/O	I	-	Sub-Q read standard level signal input
46	P02/INTP2/NMI	PCDCDI	I/O	I	-	From CD changer, data input
47	P03/INTP3	PRMC	I/O	I	-	Remote controller's signal input (interrupt3)
48	P04/INTP4	N.C	I/O	O	CMOS	Not to be used (Open)
49	P05/INTP5	N.C	I/O	O	CMOS	Not to be used (Open)
50	P06/INTP36	N.C	I/O	O	CMOS	Not to be used (Open)
51	AVDD	AVDD	-	-	-	Positive power supply to A/D converter
52	AVREF0	AVREF0	-	-	-	Reference voltage applied to A/D converter
53	P10/ANI0	N.C	I	I	-	Not to be used (Open)
54	P11/ANI1	PS_MTR	I	I	-	Radio station's strength signl input
55	P12/ANI2	PLVL_MTR	I	I	-	Sound level's signal input
56	P13/ANI3	PKEY1	I	I	-	Key # 1 line input
57	P14/ANI4	PKEY2	I	I	-	Key # 2 line input
58	P15/ANI5	PVOLA	I	I	-	Encoder volume terminal #A input
59	P16/ANI6	PVOLB	I	I	-	Encoder volume terminal #B input
60	P17/ANI7	N.C	-	-	-	Not to be used (Open)

61	AVSS	AVSS	I/O	I	-	Ground for A/D converter and D/A converter
62	P130/ANO0	N.C.	I/O	I	CMOS	Not to be used (Open)
63	P131/ANO1	N.C.	I/O	I	CMOS	Not to be used (Open)
64	AVREF1	AVREF1	I/O	I	-	Reference voltage applied to A/D converter
65	P70/RxD2/SI2	N.C.	I/O	I	CMOS	Not to be used (Open)
66	P71/RxD2/SO2	PFRT_DO	I/O	I	CMOS	To LCD driver, data output
67	P72/ASCK2/SCK2	PFRT_CLK	I/O	I	CMOS	Clock output for interface with LCD driver
68	P20/RxD1/SI1	PPLL_DI	I/O	I	-	From PLL IC, data input
69	P21/TxD1/SO1	PPLL_DO	I/O	I	CMOS	To PLL IC, data output
70	P22/ASCK1/SCK1	PPLL_CLK	I/O	I	CMOS	Clock output for interface with PLL IC
71	P23/PCL	PPLL_CE	I/O	I	CMOS	PLL IC enable output
72	P24/BUZ	PBEEP	-	-	CMOS	Beep sound output (2.4kHz)
73	P25/SIO/SDA0	PDSP_IDA	I/O	O	-	From DSP, data input
74	P26/SO0	PDSP_ODA	I/O	O	CMOS	To DSP, data output
75	P27/SCK0/SCL0	PDSP_OCLK	I/O	O	CMOS	Clock output for interface with DSP
76	P80/A0	N.C.	I/O	O	CMOS	Not to be used (Open)
77	P81/A1	N.C.	I/O	O	CMOS	Not to be used (Open)
78	P82/A2	N.C.	I/O	I	-	Not to be used (Open)
79	P83/A3	PST	I/O	I	-	Sterep indigater's signal or SD signal input
80	P84/A4	PRDS_DI	I/O	I	-	From tuner pack, RDS data input
81	P85/A5	PORT_IN0	I/O	I	-	For diode option check, signal 1 or 2 input 0
82	P86/A6	PORT_IN1	I/O	I	-	For diode option check, signal 1 or 2 input 1
83	P87/A7	PORT_IN2	I/O	I	-	For diode option check, signal 1 or 2 input 2
84	P40/AD0	PORT_OUT0	I/O	O	CMOS	For diode option check, signal 1 output
85	P41/AD1	PORT_OUT1	I/O	O	CMOS	For diode option check, signal 2 output
86	P42/AD2	PCD_EJT	I/O	I	-	Eject key input
87	P43/AD3	PFRT-CE	I/O	O	CMOS	LCD driver enable output
88	P44/AD4	PFRT-RES	I/O	O	CMOS	LCD driver reset output
89	P45/AD5	PFRT_DET	I/O	I	-	Front pannel existence signal input
90	P46/AD6	PANT	I/O	O	CMOS	Antenna control output
91	P47/AD7	PZCC	I/O	I	-	From ISO jack, ACC signal input
92	P50/A8	N.C.	I/O	O	CMOS	Not to be used (Open)
93	P51/A9	N.C.	I/O	O	CMOS	Not to be used (Open)
94	P52/A10	N.C.	I/O	O	CMOS	Not to be used (Open)
95	P53/A11	N.C.	I/O	O	CMOS	Not to be used (Open)
96	P54/A12	N.C.	I/O	O	CMOS	Not to be used (Open)
97	P55/A13	N.C.	I/O	O	CMOS	Not to be used (Open)
98	P56/A14	N.C.	I/O	O	CMOS	Not to be used (Open)
99	P57/A15	N.C.	I/O	O	CMOS	Not to be used (Open)
100	Vss	VSS	-	-	-	Ground

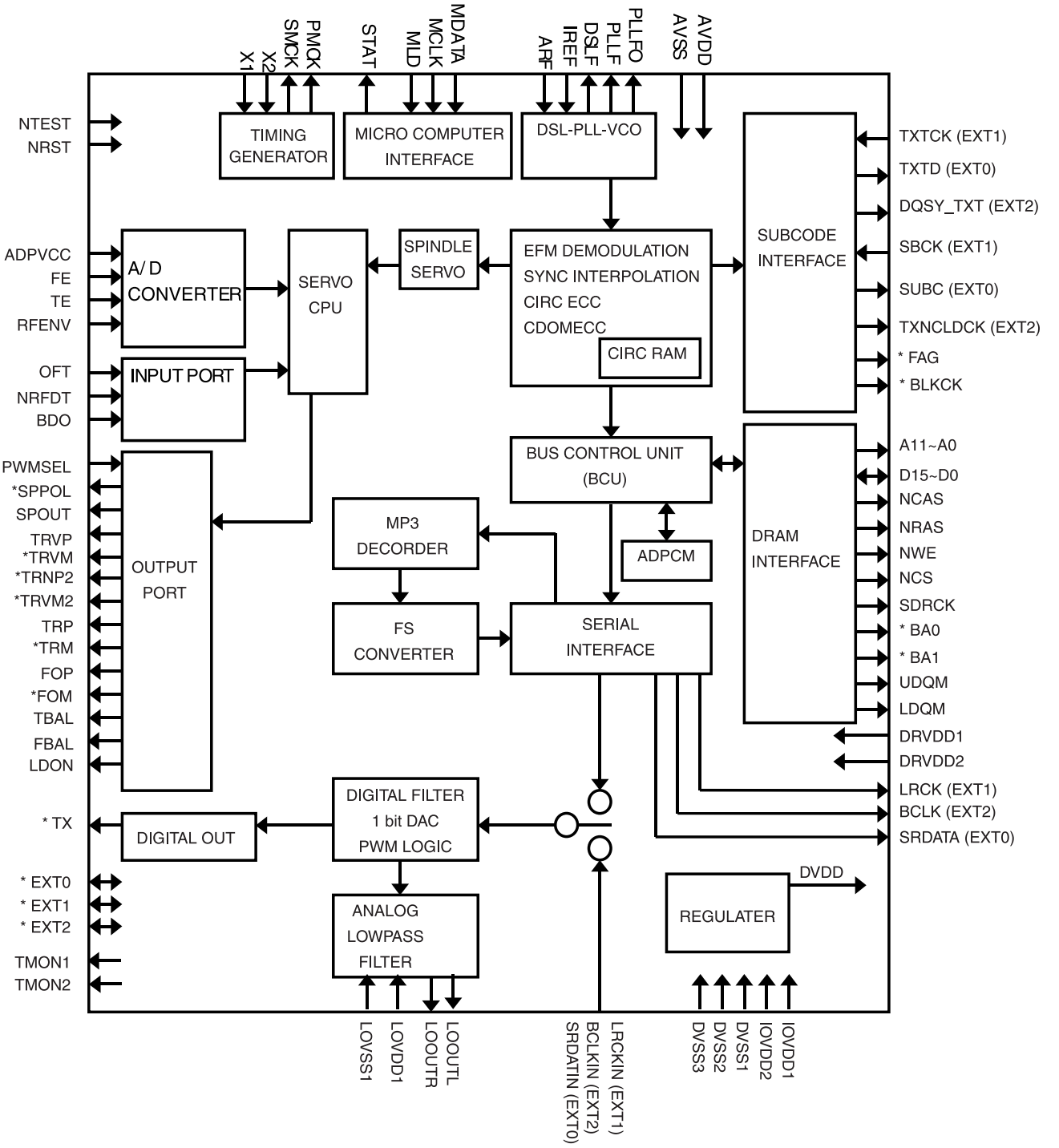
input port setted	26
output port setted	31
Used I/O port	57
Interrupt	4
A/D Converter	4

■ IC501 MN6627933

1) PORT ASSIGNMENT



2) Block Diagram



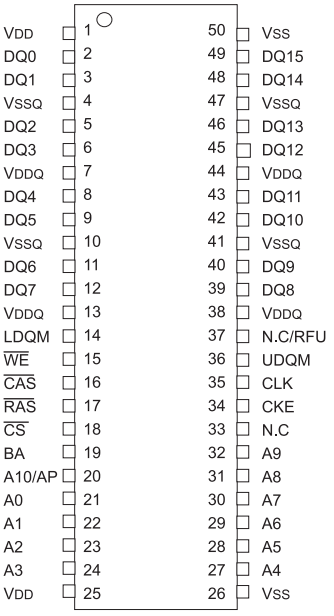
3) PORT DESCRIPTION

Pin No.	Symbol	I/O	Function
1	D11	I/O	DRAM data signal I/O 11
2	D10	I/O	DRAM data signal I/O 10
3	D9	I/O	DRAM data signal I/O 9
4	D8	I/O	DRAM data signal I/O 8
5	UDQM	O	SDRAM upper byte data mask signal output
6	SDRCK	O	SDRAM clock signal output
7	A11	O	DRAM address signal output 11
8	A9	O	DRAM address signal output 9
9	A8	O	DRAM address signal output 8
10	A7	O	DRAM address signal output 7
11	A6	O	DRAM address signal output 6
12	A5	O	DRAM address signal output 5
13	A4	O	DRAM address signal output 4
14	LDQM	O	SDRAM lower byte data mask signal output
15	NWE	O	DRAM write enable signal output
16	NCAS	O	DRAM CAS control signal output
17	NRAS	O	DRAM RAS control signal output
18	NCS	O	SDRAM chip select signal output
19	A3	O	DRAM address signal output 3
20	A2	O	DRAM address signal output 2
21	A1	O	DRAM address signal output 1
22	A0	O	DRAM address signal output 0
23	DRVDD1	I	Power supply 1 for DRAM interface I/O
24	DVSS1	I	Ground 1 for digital circuits
25	A10	O	DRAM address signal output 10
26	*BA1	O	SDRAM bank selection signal output 1
27	*BA0	O	SDRAM bank selection signal output 0
28	DVDD1	I	Power supply 1 for internal digital circuits
29	SPOUT	O	Spindle drive signal output (absolute value)
30	*SPPOL	O	Spindle drive signal output (polarity)
31	TRVP	O	Traverse drive signal output (positive polarity)
32	*TRVM	O	Traverse drive signal output (negative polarity)
33	*TRVP2	O	Traverse drive signal output 2 (positive polarity)
34	*TRVM2	O	Traverse drive signal output 2 (negative polarity)
35	TRP	O	Tracking drive signal output (positive polarity)
36	*TRM	O	Tracking drive signal output (negative polarity)
37	FOP	O	Focus drive signal output (positive polarity)
38	*FOM	O	Focus drive signal output (negative polarity)
39	IOVDD1	I	Power supply 1 for digital I/O
40	TBAL	O	Tracking balance adjustment signal output
41	FBAL	O	Focus balance adjustment signal output
42	FE	I	Focus error signal input
43	TE	I	Tracking error signal input
44	ADPVCC	I	Voltage input for supply voltage monitor
45	RFENV	I	RF envelope signal input
46	LDON	O	Laser ON signal output
47	NRFDET	I	RF detectoion signal input
48	OFT	I	Off-track signal input
49	BDO	I	Dropout signal input
50	AVDD1	I	Power supply 1 for analog circuits
51	IREF	I	Analog reference current input
52	ARF	I	RF signal input
53	DSLF	O	DSL loop filter pin
54	PWMSEL	I	PWM output mode selection input Low: Direct High: 3-state
55	PLLF	O	PLL loop filter pin (for phase comparison)
56	PLLFO	O	PLL loop filter pin (for speed comparison)
57	AVSS1	I	Ground 1 for analog circuits
58	LOOUTL	O	L-ch audio output for line-out output
59	LOVSS1	I	Ground for line-out output

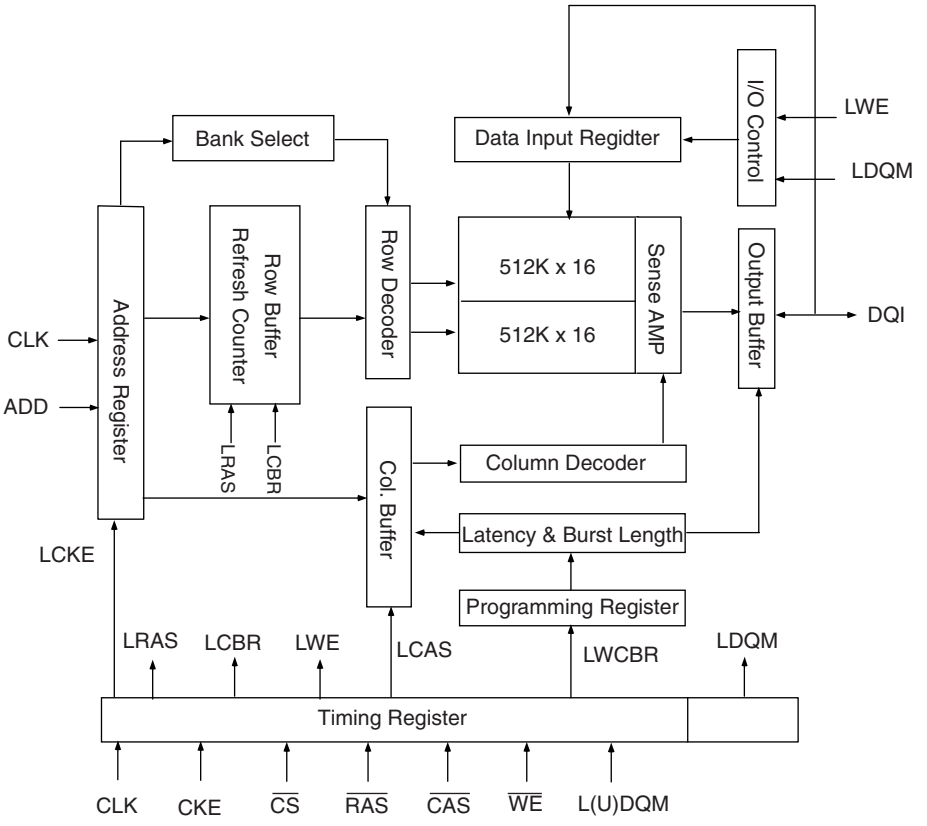
Pin No.	Symbol	I/O	Function
60	LOOUTR	O	R-ch audio output for line-out output
61	LOVDD1	I	Power supply for line-out output
62	N.C.	-	-
63	TMON1	O	Test monitor output 1
64	N.C.	-	-
65	N.C.	-	-
66	TMON2	O	Test monitor output 2
67	DVDD3	I	Power supply 3 for digital circuits
68	DVSS2	I	Ground 2 for digital circuits
69	*EXT0	I/O	Expansion I/O port 0
70	*EXT1	I/O	Expansion I/O port 1
71	*EXT2	I/O	Expansion I/O port 2
72	MCLK	I	Microcontroller command clock signal input
73	MDATA	I	Microcontroller command data signal input
74	MLD	I	Microcontroller command load signal input
75	*STAT	O	Status signal output
76	*BLKCK	O	Subcode block clock signal output
77	*SMCK	O	4.2336-/8.4672-MHz clock signal output
78	*PMCK	O	88.2-kHz clock signal output
79	*TX	O	Digital audio interface signal output
80	*FLAG	O	Flag signal output
81	NRST	I	LSI reset signal input
82	NTEST	I	Test mode setting input
83	DVSS3	I	Ground 3 for digital circuits
84	X1	I	Crystal oscillator circuit input
85	X2	O	Crystal oscillator circuit output
86	IOVDD2	I	Power supply 2 for digital I/O
87	DVDD2	I	Power supply 2 for internal digital circuits
88	D2	I/O	DRAM data signal I/O 2
89	D1	I/O	DRAM data signal I/O 1
90	D0	I/O	DRAM data signal I/O 0
91	D3	I/O	DRAM data signal I/O 3
92	D4	I/O	DRAM data signal I/O 4
93	D5	I/O	DRAM data signal I/O 5
94	D6	I/O	DRAM data signal I/O 6
95	D7	I/O	DRAM data signal I/O 7
96	D15	I/O	DRAM data signal I/O 15
97	D14	I/O	DRAM data signal I/O 14
98	DRVDD2	I	Power supply 2 for DRAM interface I/O
99	D13	I/O	DRAM data signal I/O 13
100	D12	I/O	DRAM data signal I/O 12

■ IC503 M12L16161A

1) PORT ASSIGNMENT



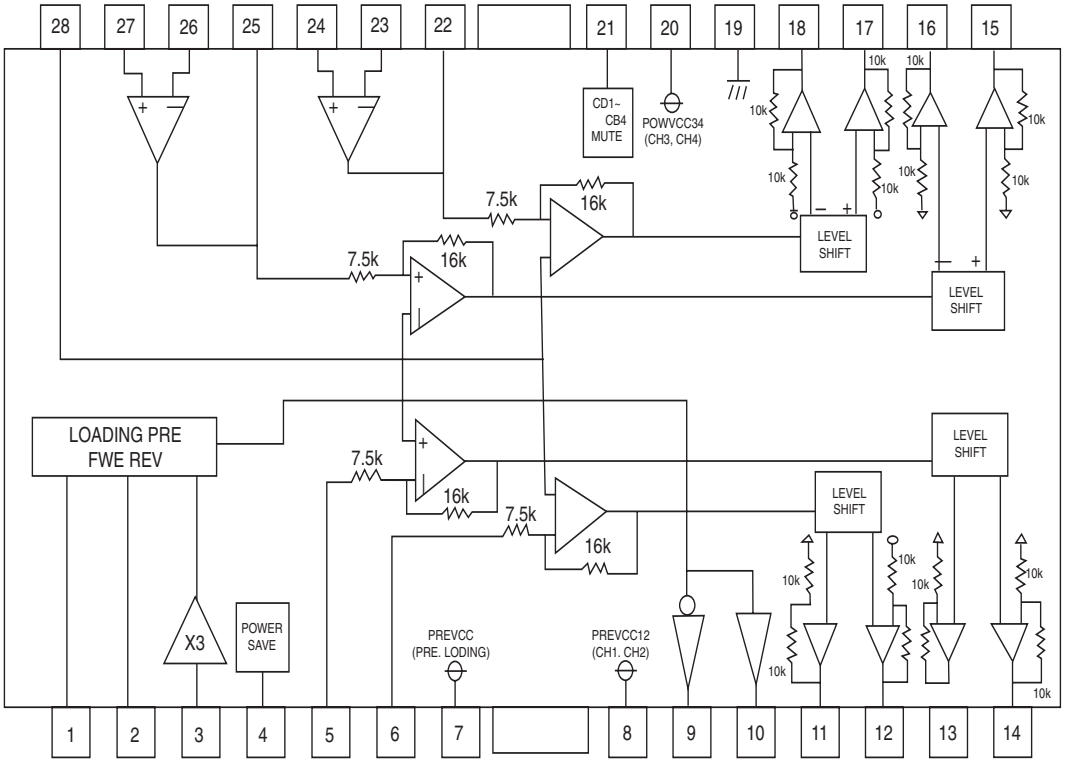
2) BLOCK DIAGRAM



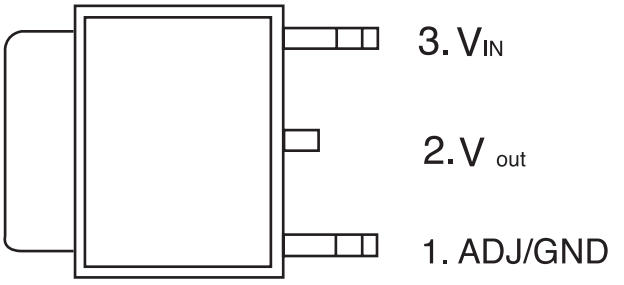
■ PIN Function table

Pin	Name	Input Function
CLK	System Clock	Active on the positive going edge to sample all inputs.
CS	Chip Select	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and L(U)DQM.
CKE	Clock Enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A0~A10/AP	Address	Row/Column addresses are multiplexed on the same pins. Row address: RA0~RA10, column address: CA0~CA7
BA	Bank Select Address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
RAS	Row Address Strobe	Latches row addresses on the positive going edge of the CLK with RAS low. Enables row access & precharge.
CAS	Column Address Strobe	Latches column addresses on the positive going edge of the CLK with CAS low. Enables column access.
WE	Write Enable	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
L(U)DQM	Data Input / Output Mask	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when L(U)DQM active.
DQ0~15	Data Input / Output	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	Power Supply/Ground	Power and ground for the input buffers and the core logic.
VDDQ/VSSQ	Data Output Power/Ground	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C/RFU	No Connection/ Reserved for Future Use	This is recommended to be left No Connection on the device.

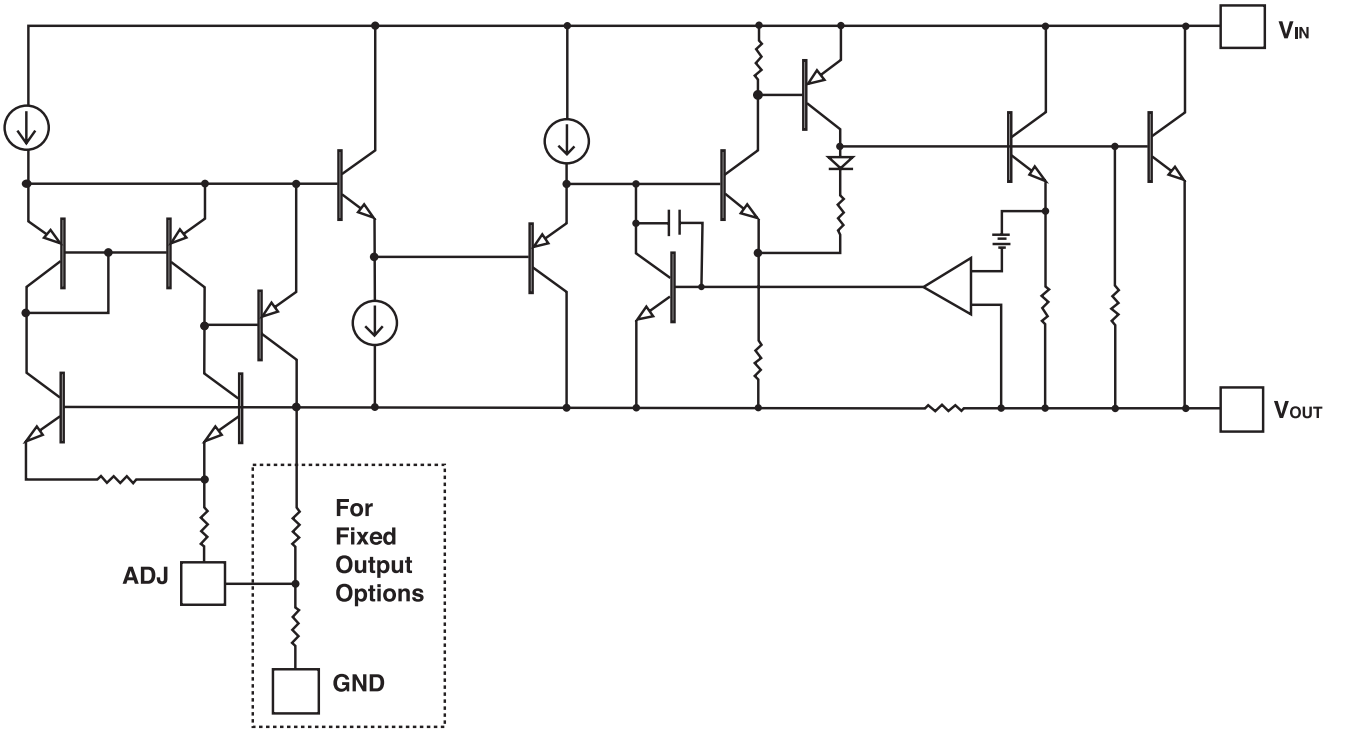
■ IC504 BA5810FP



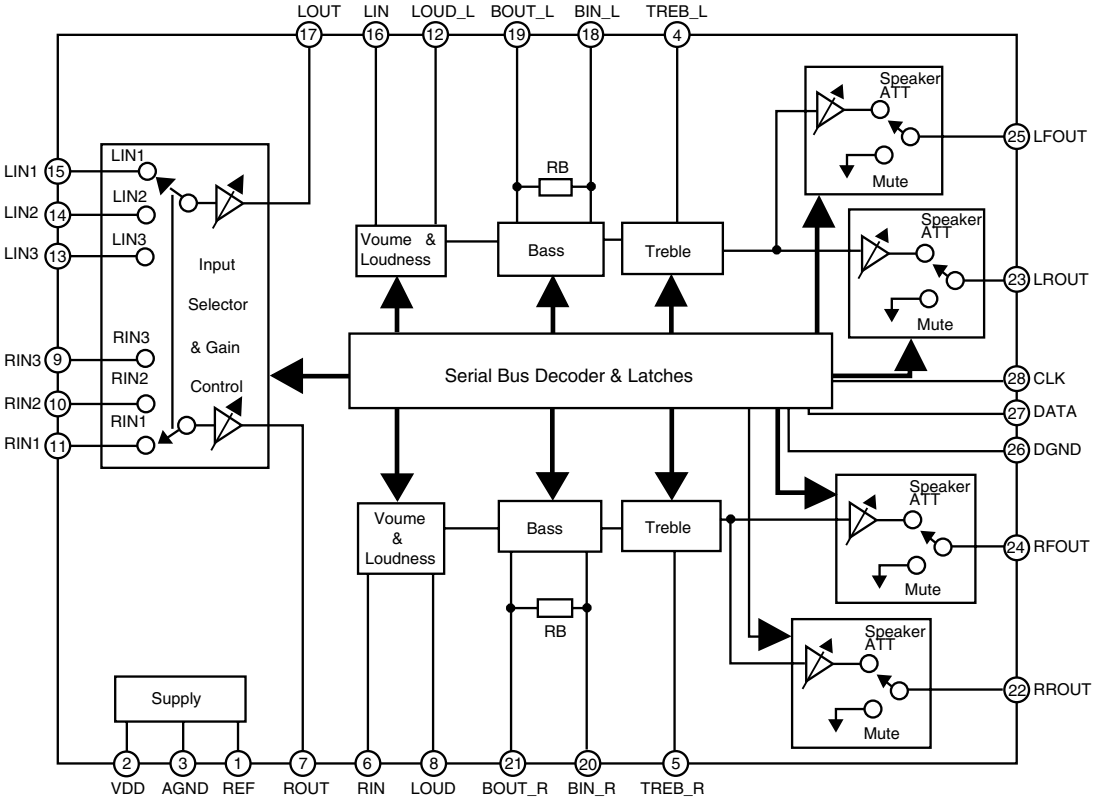
■ IC505 AMC1117



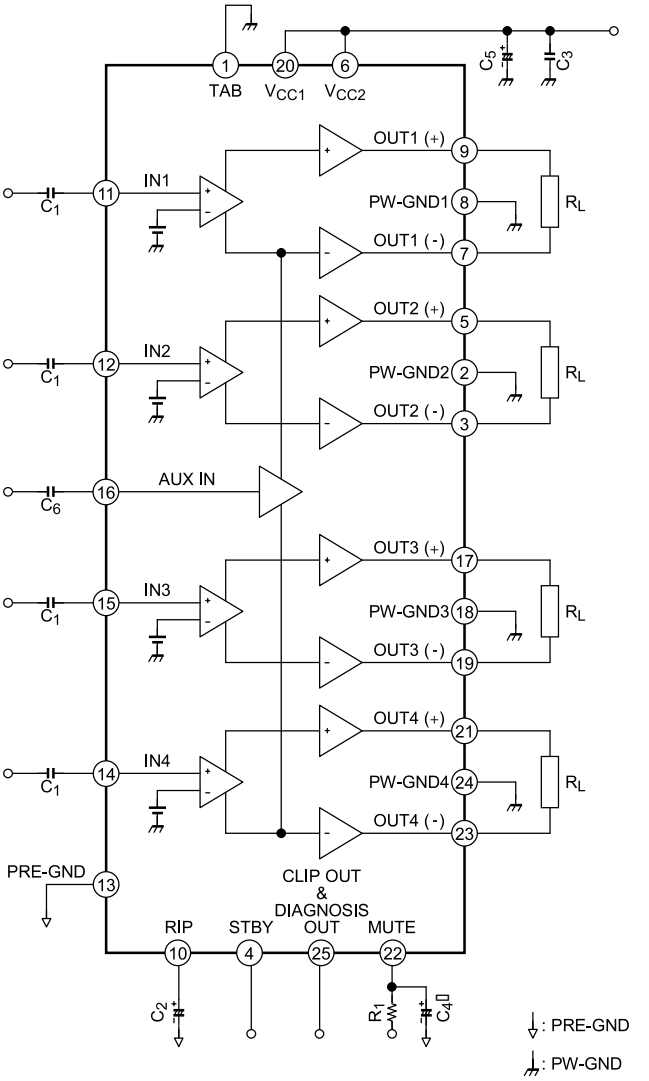
■ BLOCK DIAGRAM



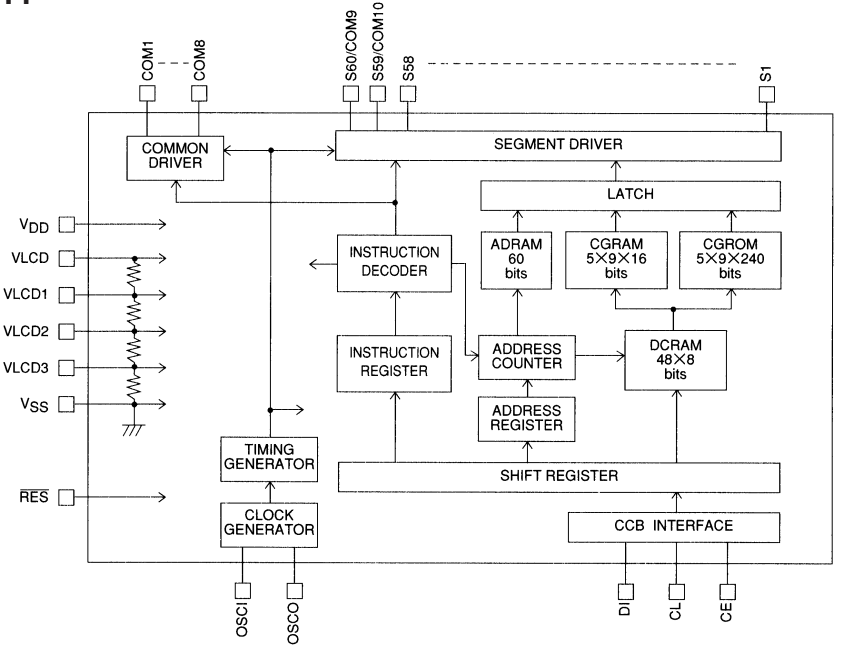
■ IC601 PT2313L



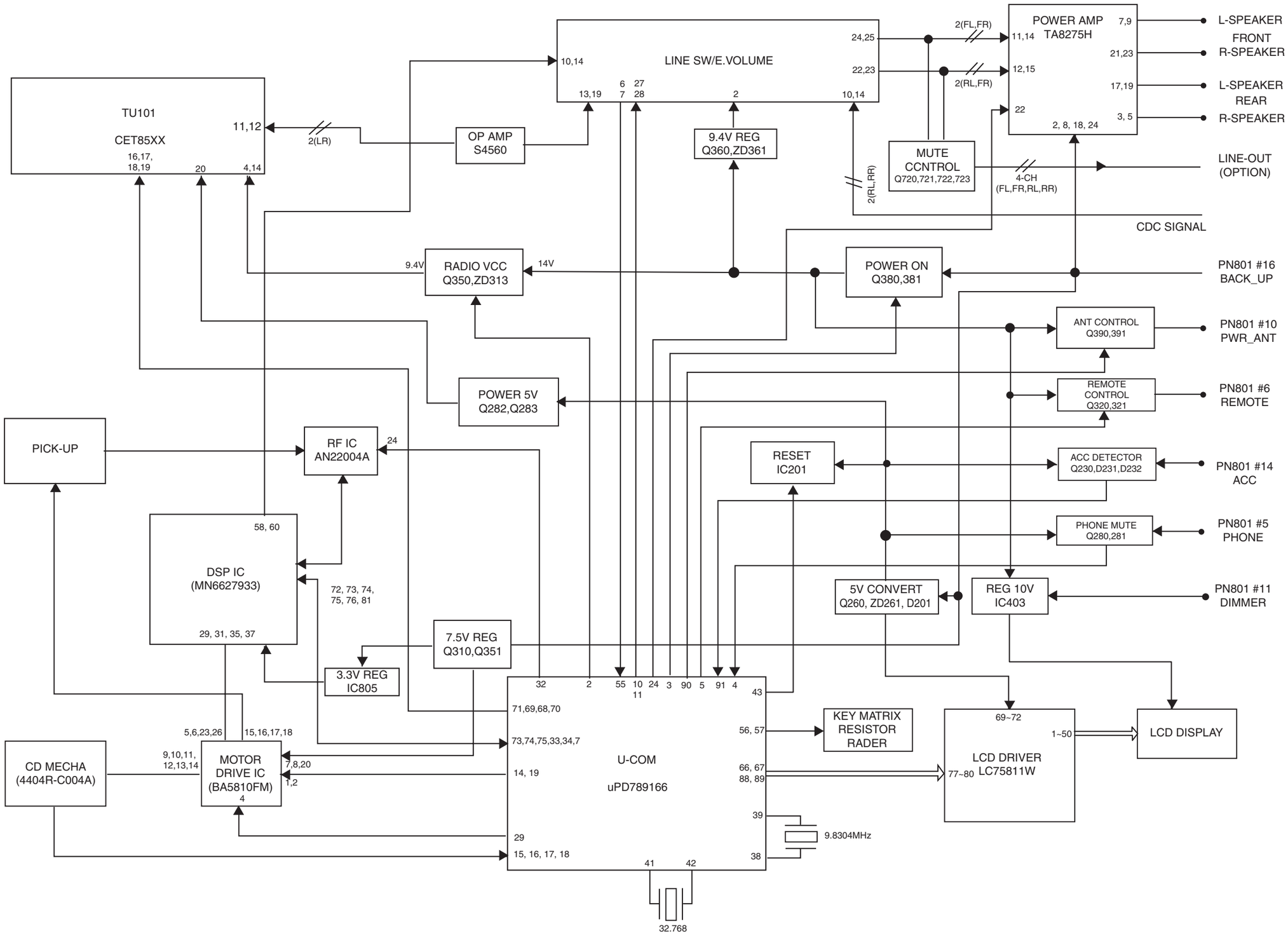
■ IC801 TA8275H



■ IC901 LC75811

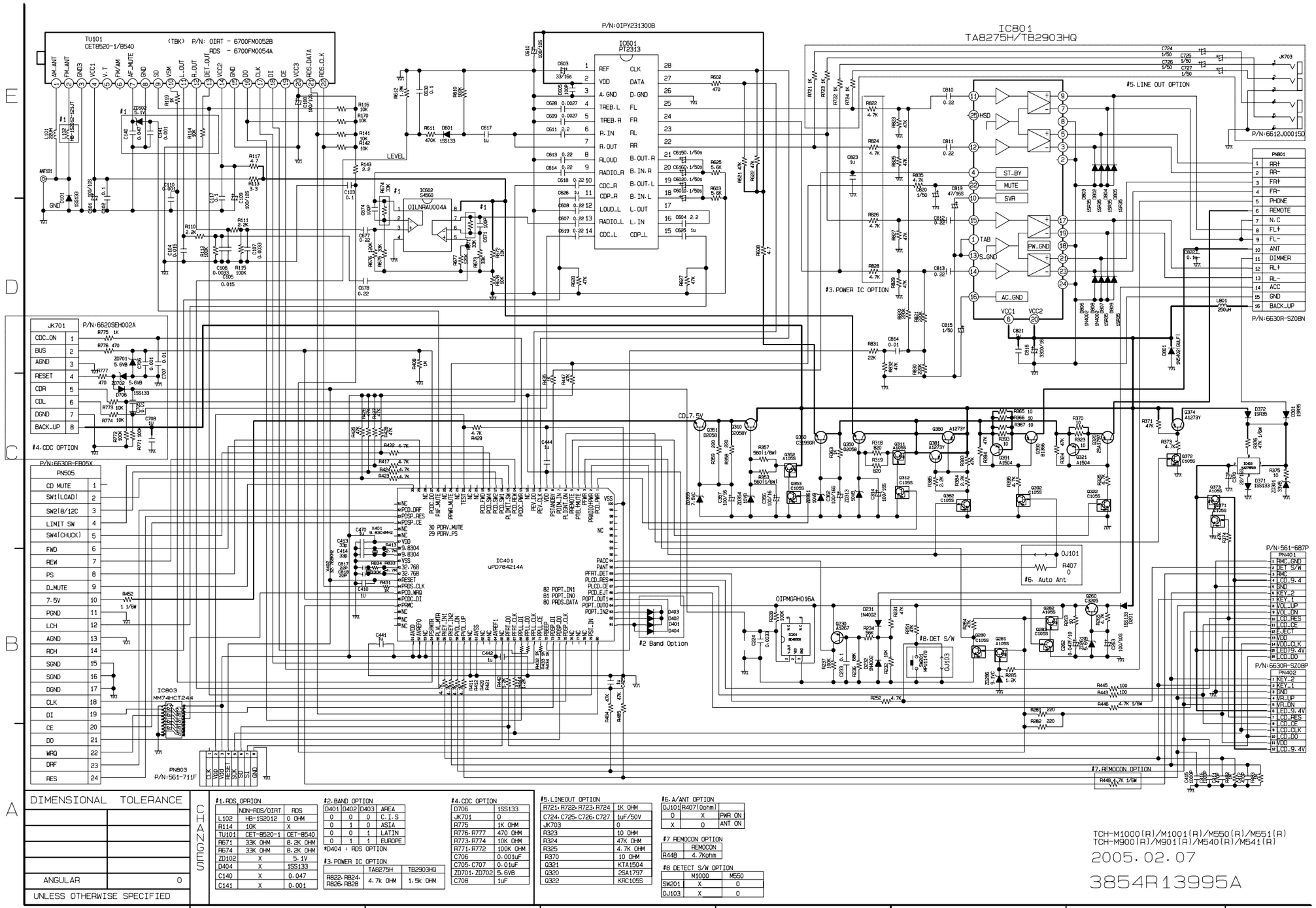


❑ BLOCK DIAGRAM



❑ SCHEMATIC DIAGRAM

• MAIN SCHEMATIC DIAGRAM



DIMENSIONAL TOLERANCE	
ANGULAR	0
UNLESS OTHERWISE SPECIFIED	

CHANGES

#1.RDS OPRION

	NON-RDS/OIRT	RDS
L102	HB-1S2012	0 OHM
R114	10K	X
TU101	CET-8520-1	CET-8540
R671	33K OHM	8.2K OHM
R674	33K OHM	8.2K OHM
ZD102	X	5.1V
D404	X	1SS133
C140	X	0.047
C141	X	0.001

#2.BAND OPTION

D401	D402	D403	AREA
0	0	0	C.I.S
0	1	0	ASIA
0	0	1	LATIN
0	1	1	EUROPE

#D404 : RDS OPTION

#3.POWER IC OPTION

	TA8275H	TB2903HQ
R822,R824, R826,R828	4.7k OHM	1.5k OHM

#4.CDC OPTION

D706	1SS133
JK701	0
R775	1K OHM
R776,R777	470 OHM
R773,R774	10K OHM
R771,R772	100K OHM
C706	0.001uF
C705,C707	0.01uF
ZD701,ZD702	5.6VB
C708	1uF

#5.LINEOUT OPTION

R721,R722,R723,R724	1K OHM
C724,C725,C726,C727	1uF/50V
JK703	0
R323	10 OHM
R324	47K OHM
R325	4.7K OHM
R370	10 OHM
Q321	KTA1504
Q320	2SA1797
Q322	KRC105S

#6.A/ANT OPTION

OJ101	R407(0ohm)	
0	X	PWR ON
X	0	ANT ON

#7 REMOCON OPTION

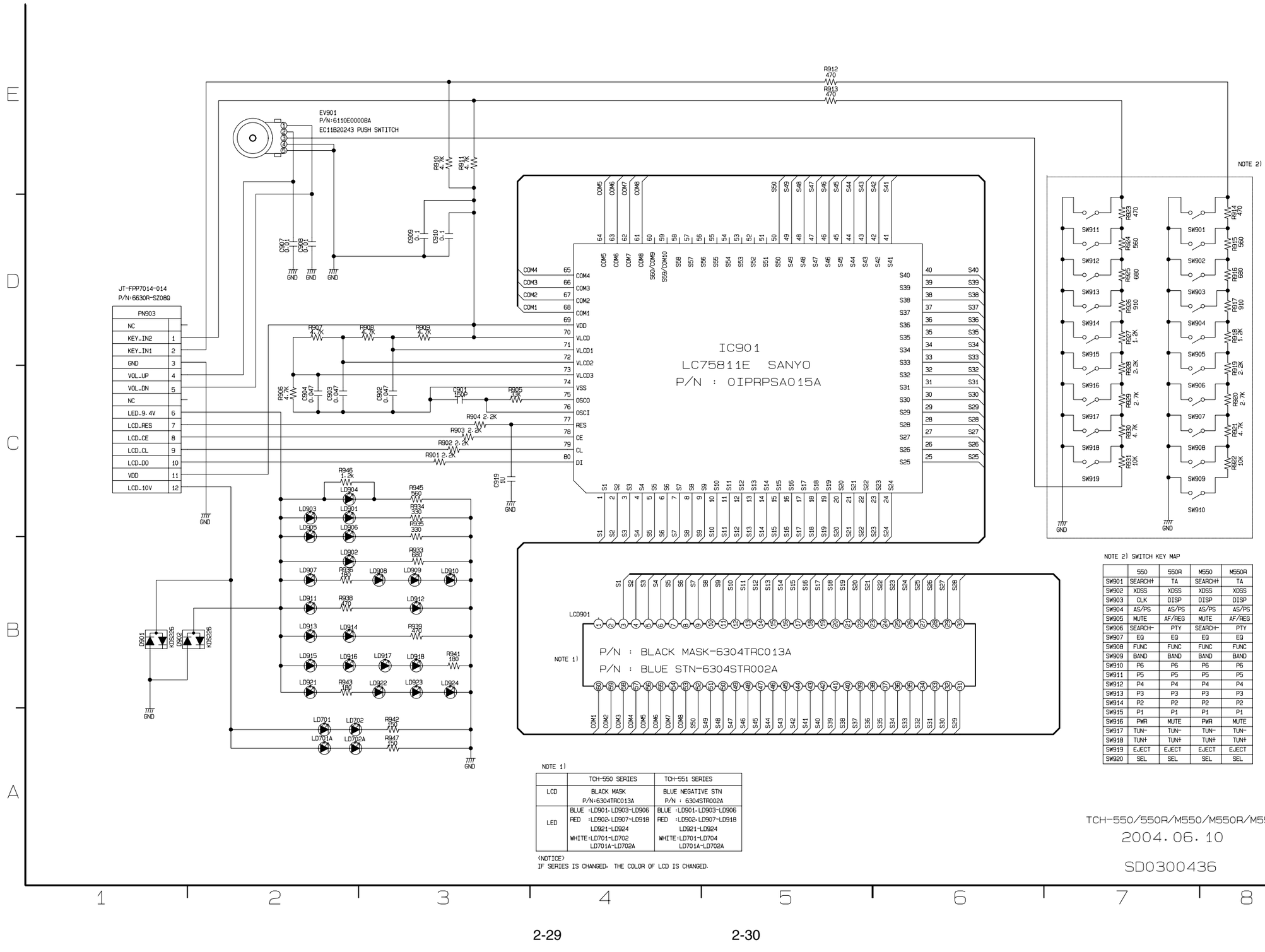
	REMOCON
R448	4.7Kohm

#8.DETECT S/W OPTION

	M1000	M550
SW201	X	0
OJ103	X	0

TCH-M1000(R)/M1001(R)/M550(R)/M551(R)
TCH-M900(R)/M901(R)/M540(R)/M541(R)
2005.02.07
3854R13995A

• FRONT SCHEMATIC DIAGRAM



NOTE 1)

	TCH-550 SERIES	TCH-551 SERIES
LCD	BLACK MASK P/N:6304TRC013A	BLUE NEGATIVE STN P/N : 6304STR002A
LED	BLUE :LD901, LD903~LD906 RED :LD902, LD907~LD918 LD921~LD924 WHITE:LD701~LD702 LD701A~LD702A	BLUE :LD901, LD903~LD906 RED :LD902, LD907~LD918 LD921~LD924 WHITE:LD701~LD704 LD701A~LD702A

〈NOTICE〉
IF SERIES IS CHANGED, THE COLOR OF LCD IS CHANGED.

NOTE 2) SWITCH KEY MAP

	550	550R	M550	M550R
SW901	SEARCH+	TA	SEARCH+	TA
SW902	XDSS	XDSS	XDSS	XDSS
SW903	CLK	DISP	DISP	DISP
SW904	AS/PS	AS/PS	AS/PS	AS/PS
SW905	MUTE	AF/REG	MUTE	AF/REG
SW906	SEARCH-	PTY	SEARCH-	PTY
SW907	EQ	EQ	EQ	EQ
SW908	FUNC	FUNC	FUNC	FUNC
SW909	BAND	BAND	BAND	BAND
SW910	P6	P6	P6	P6
SW911	P5	P5	P5	P5
SW912	P4	P4	P4	P4
SW913	P3	P3	P3	P3
SW914	P2	P2	P2	P2
SW915	P1	P1	P1	P1
SW916	PWR	MUTE	PWR	MUTE
SW917	TUN-	TUN-	TUN-	TUN-
SW918	TUN+	TUN+	TUN+	TUN+
SW919	EJECT	EJECT	EJECT	EJECT
SW920	SEL	SEL	SEL	SEL

TCH-550/550R/M550/M550R/M551
2004.06.10
SD0300436

• CDP SCHEMATIC DIAGRAM