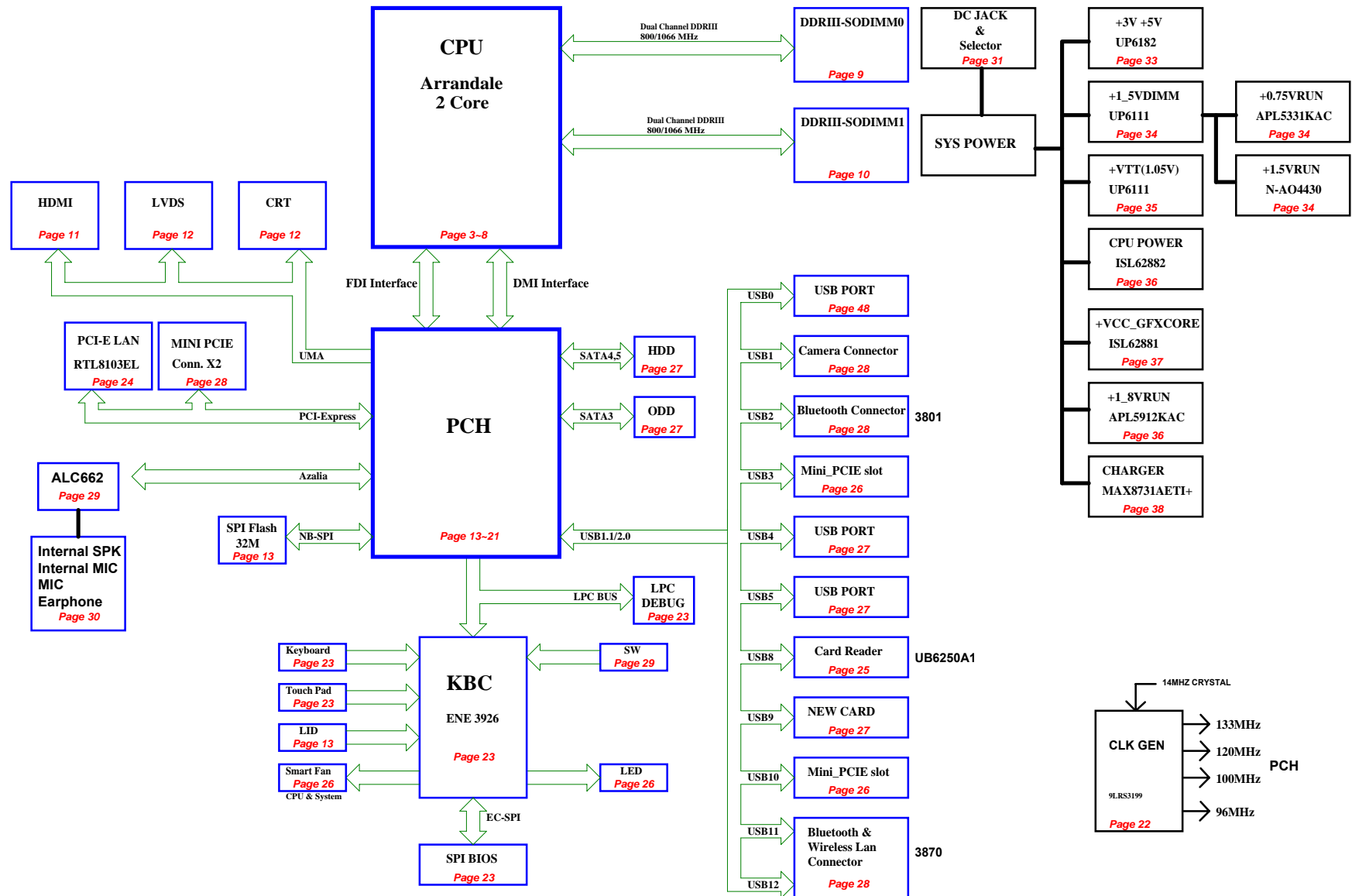


## Calpella Platform

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# SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

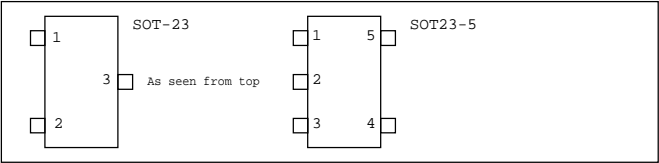
## Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
PWR_SRC	19V	S0,(S3-S5)	LAN
+5VALW	5V	S0,(S3-S5)	
+5VRUN	5V	S0	
+5VSUS	5V	S0	
+3VALW	3.3V	S0,(S3-S5)	
+3VSUS	3.3V	S0,(S3-S5)	
+3VRUN	3.3V	S0	DDRIII core
+1_5VDIMM	1.5V	S0,S3	
+1_5VRUN	1.5V	S0	
VTT	1.05V	S0	PCH
+0_75VRUN	0.75V	S0	DDRIII command & control pull up.
+VCC_CORE	1.05V~1.1V	S0	CPU core rail
+VCC_GFXCORE	1.1V	S0	Graphics core rail ( Dual Core only )

## Net Naming Conventions

<b>Suffix</b>
# = Active Low Signal
<b>Prefix</b>
H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)

## PCB Footprints



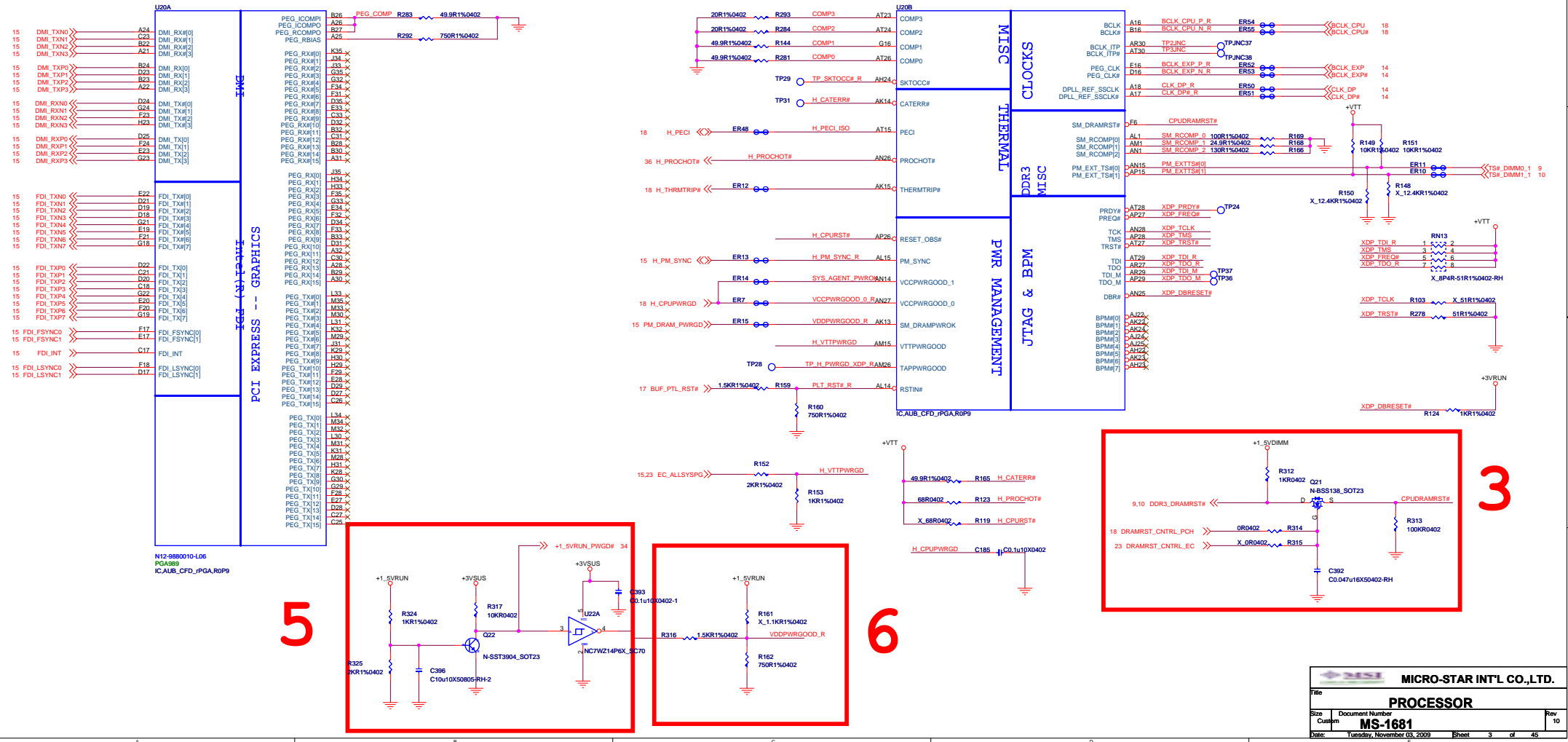
## AC Mode

Power States	SLP_S3#	SLP_S4#	SLP_S5#	SLP_LAN#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF

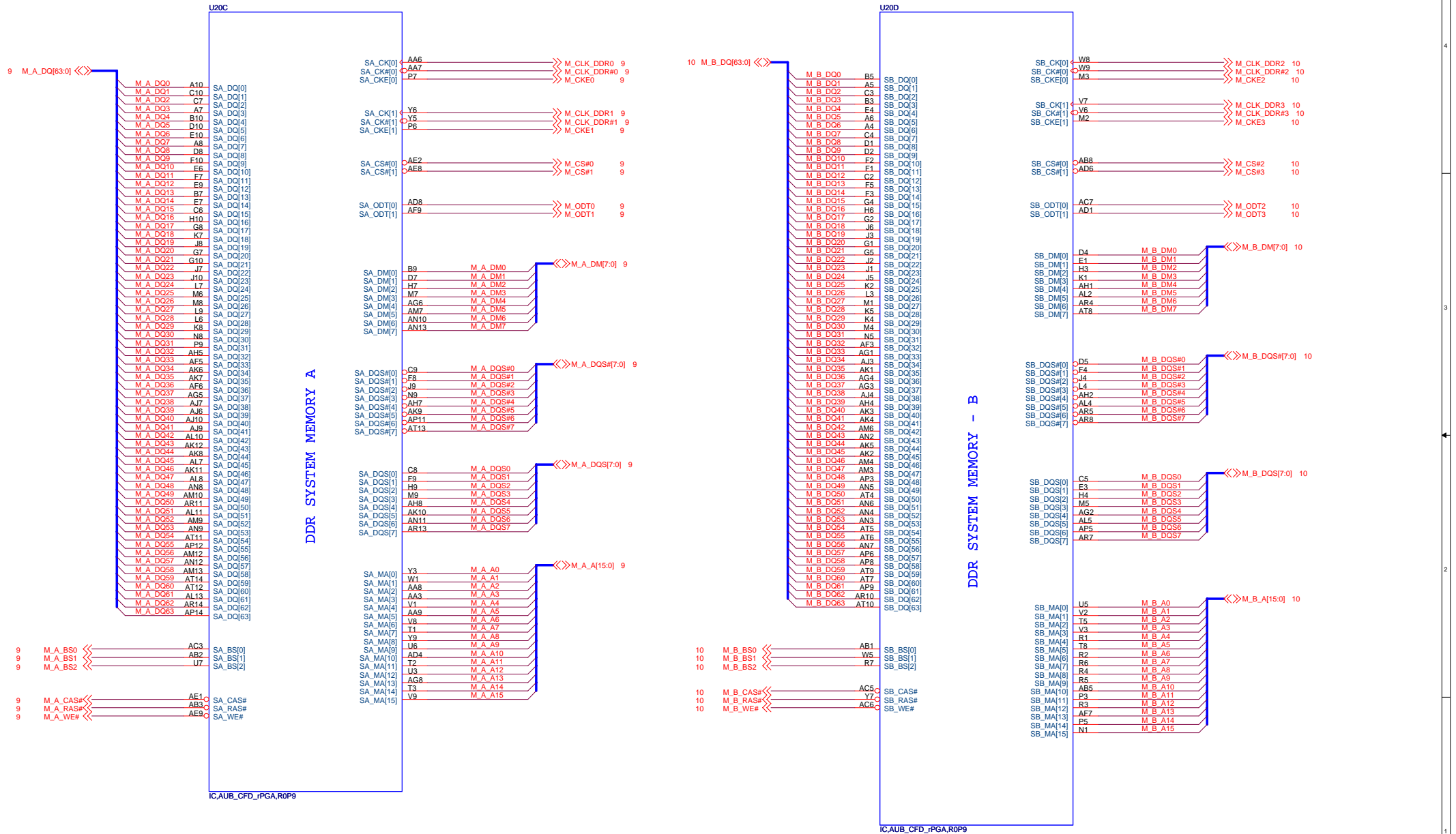
## Battery Mode

Power States	SLP_S3#	SLP_S4#	SLP_S5#	SLP_LAN#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	HIGH	ON	OFF	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF

# ARRANDALE PROCESSOR (CLK,MISC,JTAG)



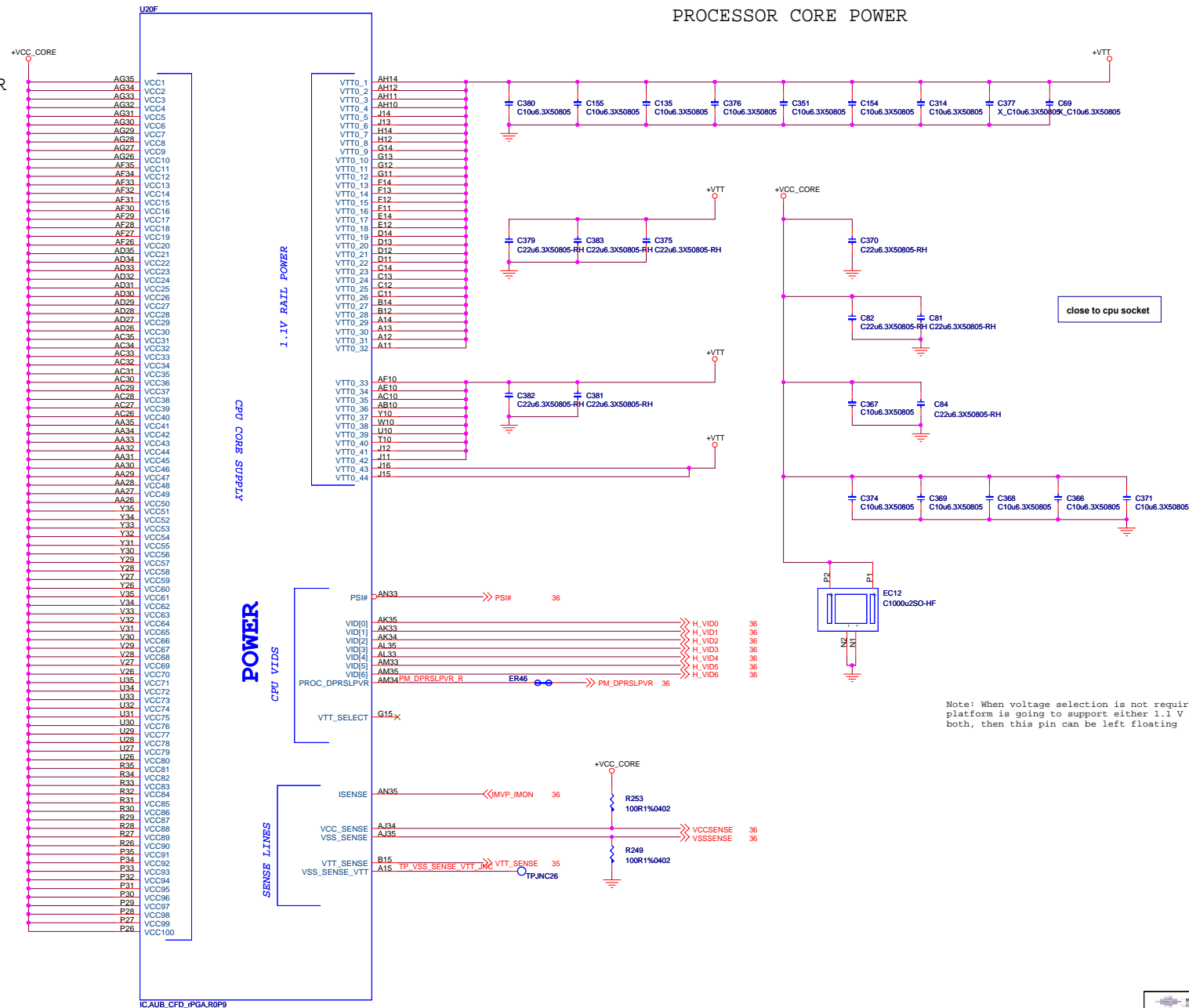
# ARRANDALE PROCESSOR (DDR3)



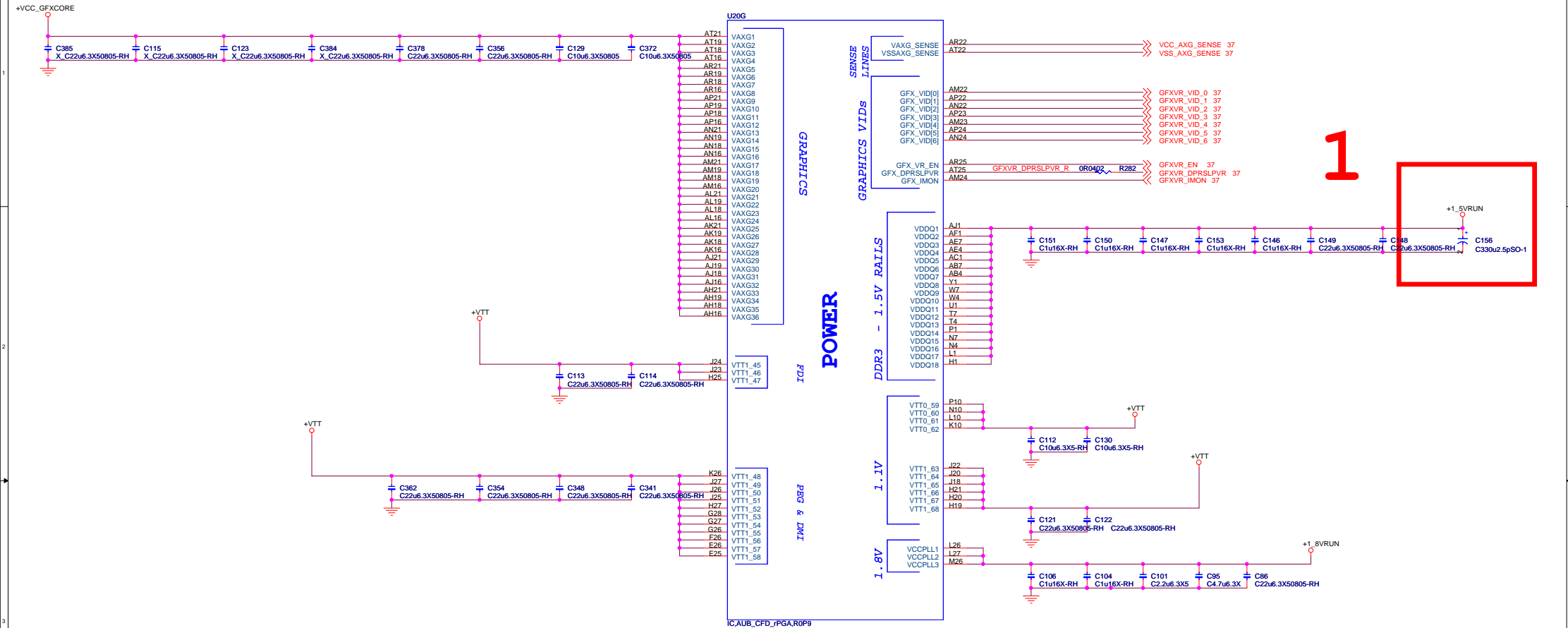
# ARRANDALE PROCESSOR (POWER)

## PROCESSOR CORE POWER

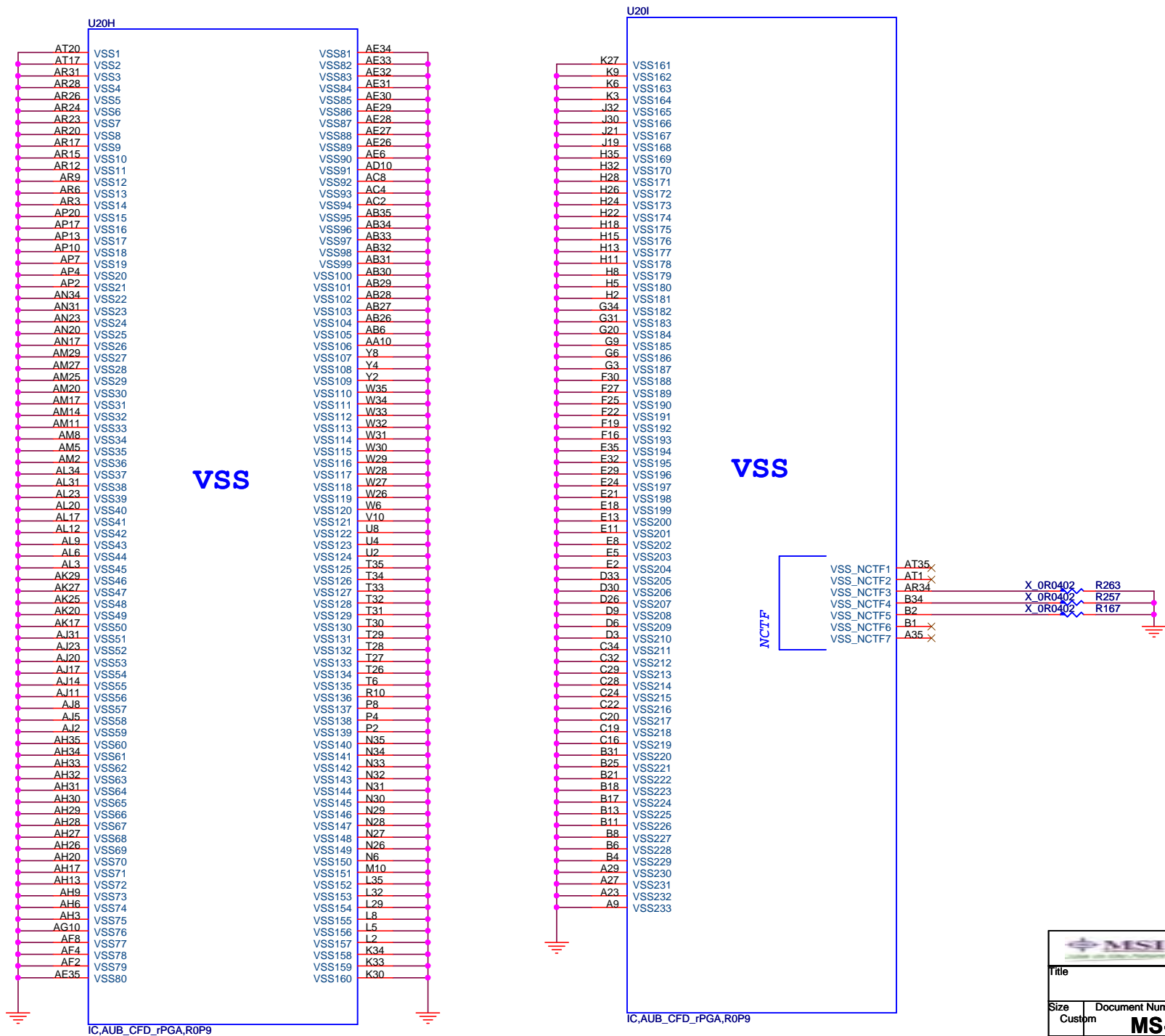
## PROCESSOR CORE POWER



ARRANDALE PROCESSOR (GRAPHICS POWER)



# ARRANDALE PROCESSOR (GND)



# ARRANDALE PROCESSOR (RESERVED)

U20E

AP25  
AL25  
AL24  
AL22  
AJ33  
AG9  
M27  
L28  
J17  
H17  
G25  
G17  
E31  
E30

RSVD1  
RSVD2  
RSVD3  
RSVD4  
RSVD5  
RSVD6  
RSVD7  
RSVD8  
RSVD9  
RSVD10  
RSVD11  
RSVD12  
RSVD13  
RSVD14

TP25  
TP17  
TP21  
TP22  
TP8  
TP7  
TP15  
TP26  
TP27  
TP19  
TP13  
TP9  
TP23  
TP20  
TP18  
TP30

CFG0  
CFG1  
CFG2  
CFG3  
CFG4  
CFG5  
CFG6  
CFG7  
CFG8  
CFG9  
CFG10  
CFG11  
CFG12  
CFG13  
CFG14  
CFG15  
CFG16  
CFG17  
CFG18

B19  
A19  
A20  
B20  
U9  
T9  
AC9  
AB9  
C1  
A3  
J29  
J28  
A34  
A33  
C35  
B35

RSVD15  
RSVD16  
RSVD17  
RSVD18  
RSVD19  
RSVD20  
RSVD21  
RSVD22  
RSVD\_NCTF\_23  
RSVD\_NCTF\_24  
RSVD26  
RSVD27  
RSVD\_NCTF\_28  
RSVD\_NCTF\_29  
RSVD\_NCTF\_30  
RSVD\_NCTF\_31

IC\_AUB\_CFD\_rPGA,R0P9

RESERVED

RSVD32  
RSVD33  
RSVD34  
RSVD35  
RSVD36  
RSVD\_NCTF\_37  
RSVD38  
RSVD39  
RSVD\_NCTF\_40  
RSVD\_NCTF\_41  
RSVD\_NCTF\_42  
RSVD\_NCTF\_43

RSVD45  
RSVD46  
RSVD47  
RSVD48  
RSVD49  
RSVD50  
RSVD51  
RSVD52  
RSVD53  
RSVD\_NCTF\_54  
RSVD\_NCTF\_55  
RSVD\_NCTF\_56  
RSVD\_NCTF\_57  
RSVD58

RSVD\_TP\_59  
RSVD\_TP\_60  
KEY  
RSVD62  
RSVD63  
RSVD64  
RSVD65

RSVD\_TP\_66  
RSVD\_TP\_67  
RSVD\_TP\_68  
RSVD\_TP\_69  
RSVD\_TP\_70  
RSVD\_TP\_71  
RSVD\_TP\_72  
RSVD\_TP\_73  
RSVD\_TP\_74  
RSVD\_TP\_75

RSVD\_TP\_76  
RSVD\_TP\_77  
RSVD\_TP\_78  
RSVD\_TP\_79  
RSVD\_TP\_80  
RSVD\_TP\_81  
RSVD\_TP\_82  
RSVD\_TP\_83  
RSVD\_TP\_84  
RSVD\_TP\_85

VSS

AJ13  
AJ12

H RSVD32  
H RSVD33

TP38  
TP39

AH25  
AK26

H RSVD35

TP40

AL26  
AR2

H RSVD36

TP41

AJ26  
AJ27

H RSVD40

TP42

AT3  
AR1

H RSVD40

TP42

AT3  
AR1

H RSVD40

TP42

AT3  
AR1

H RSVD40

TP42

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H RSVD40

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H RSVD40

TP42

AT3  
AR1

H RSVD40

TP42

AT3  
AR1

H RSVD40

TP42

AT3  
AR1

H RSVD40

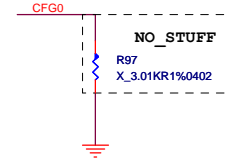
TP42

AT3  
AR1

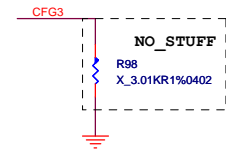
H RSVD40

TP42

PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

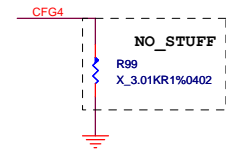


CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...



CFG[3] - PCI Express\* Static Lane  
Numbering Reversal. Lane Reversal will be  
applied across all 16 Lanes.  
1: No lane reversal  
0: Reversal

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

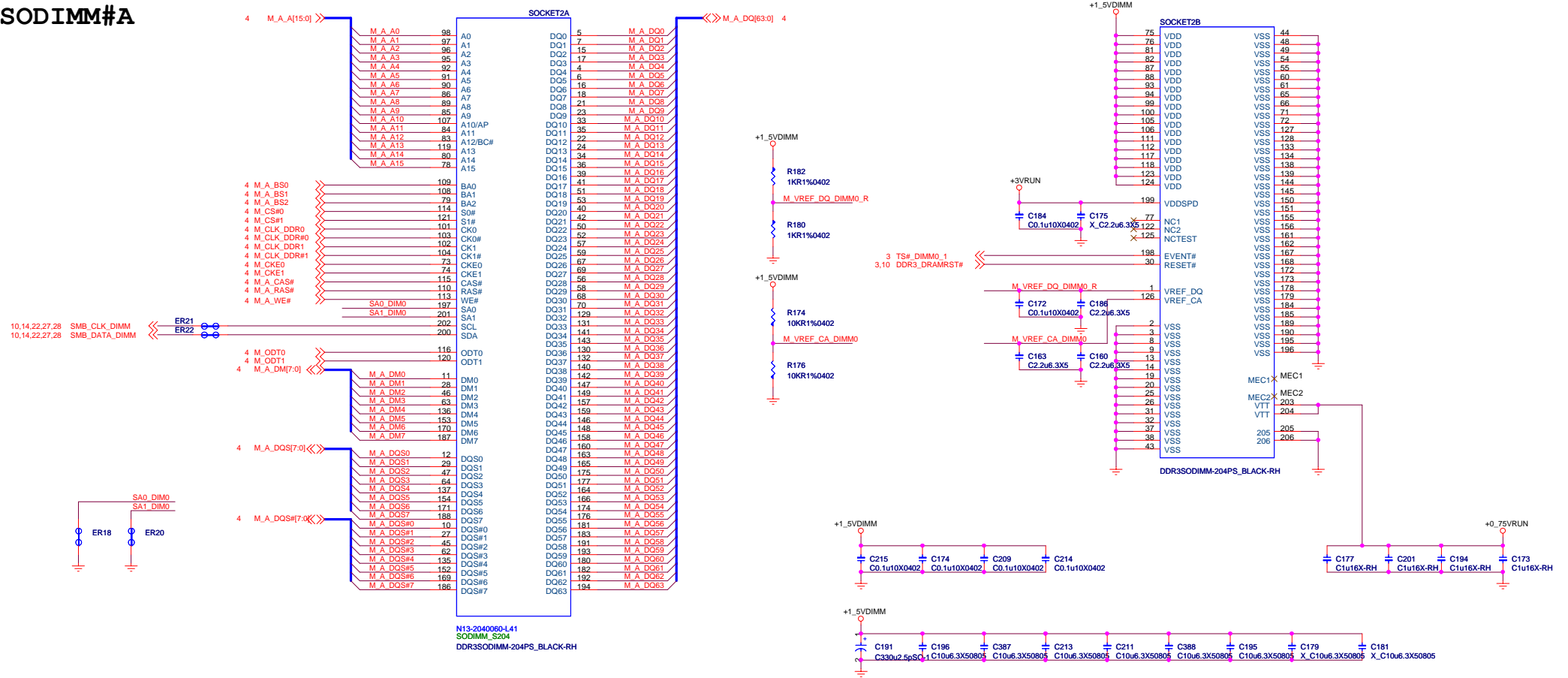


Layout Note:  
Location of all CFG strap resistors needs  
to be close to trace to minimize stub

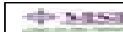
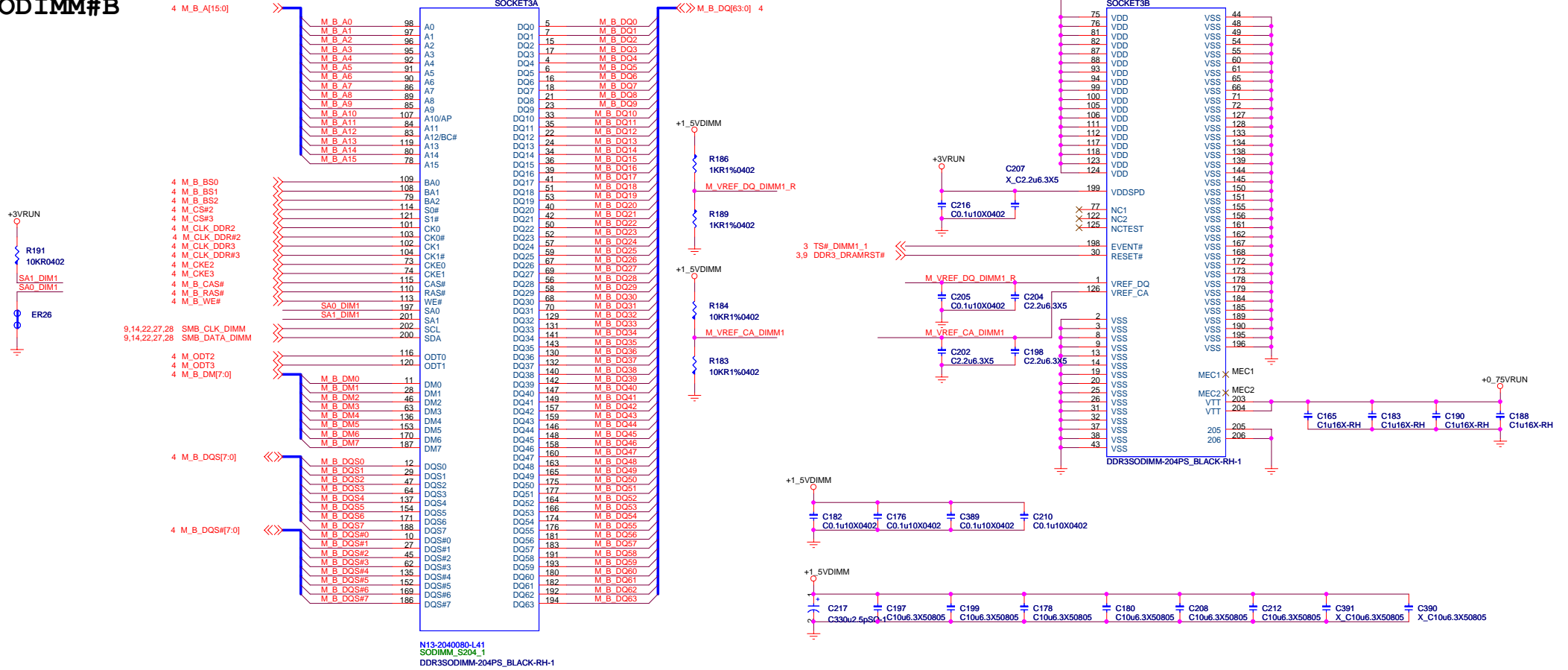
Vss (AP34) can be left NC  
is CRB implementation;  
EDS/DG recommendation to GND



SODIMM#A



**SODIMM#B**



**MICRO-STAR INT'L CO.,LTD.**

Title
-------

## DDR3 SODIMM1

Size	
Custom	

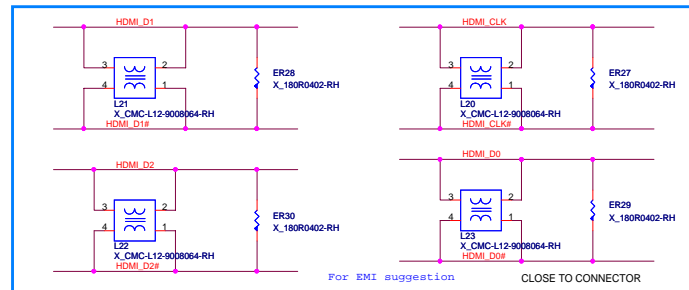
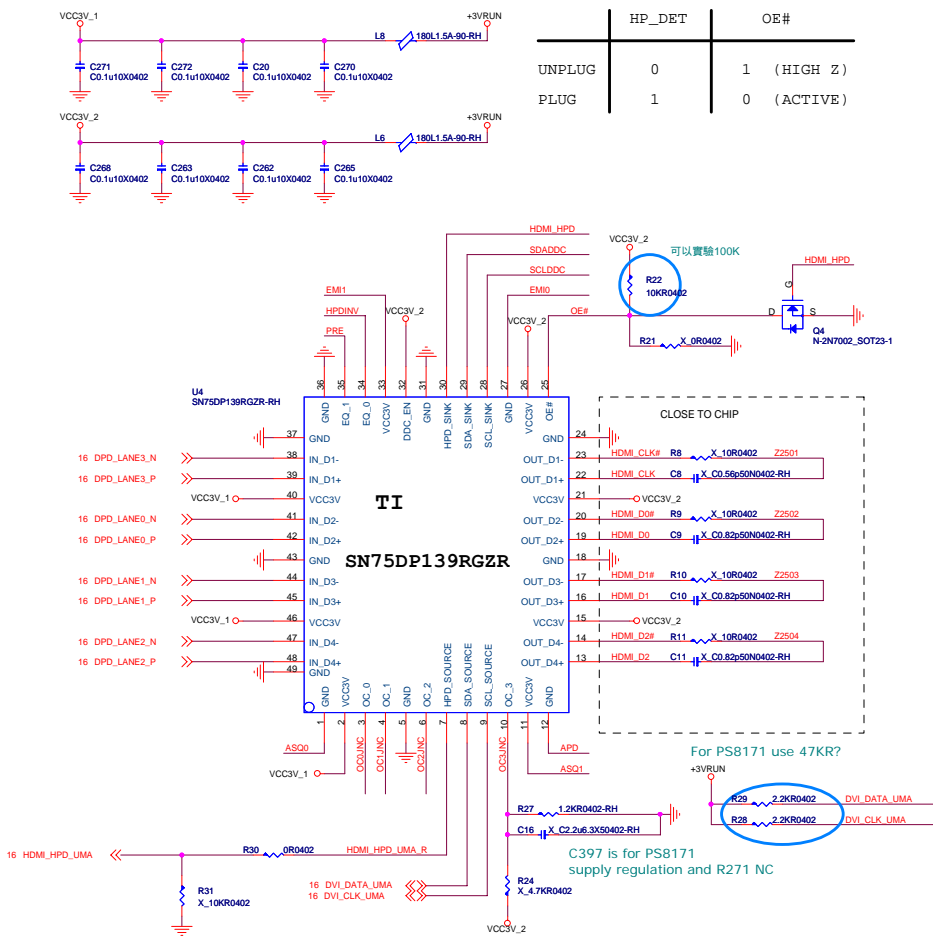
MS-1681

Date: \_\_\_\_\_

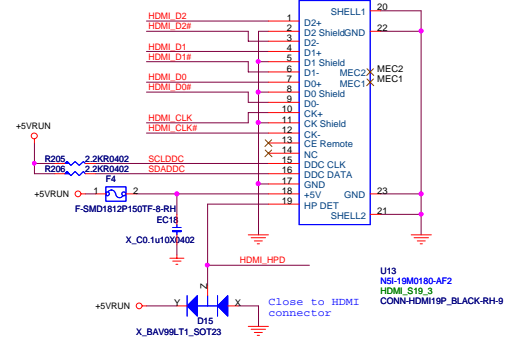
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10

## HDMI Switch

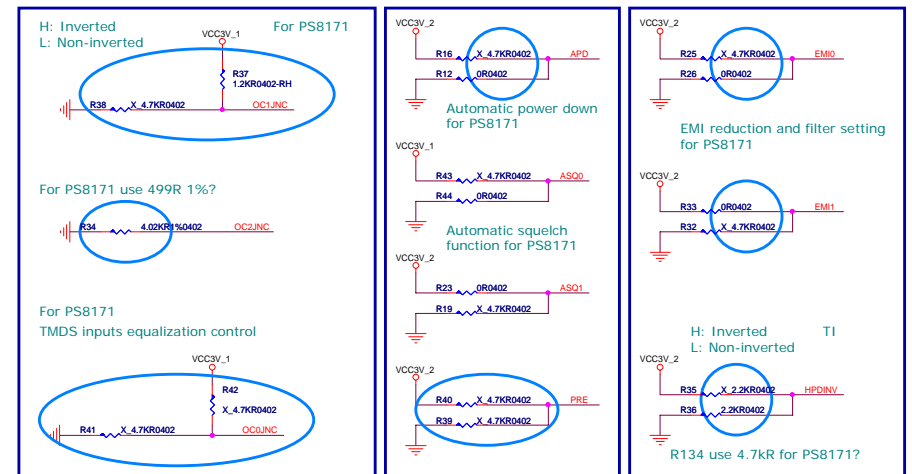


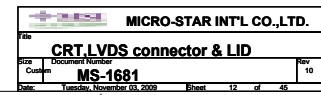
## HDMI connector

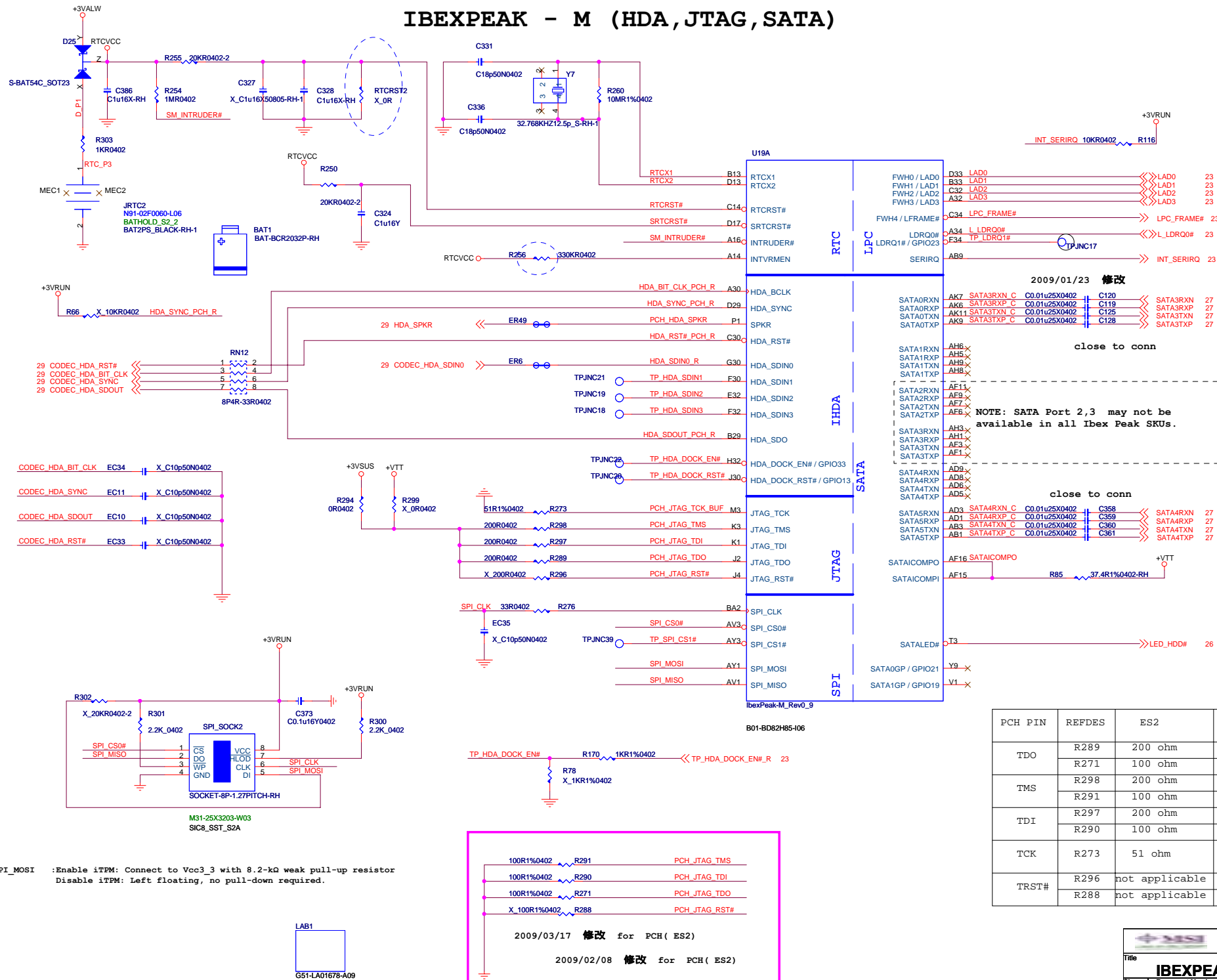


SN75DP139	PS8171	Pin no.
Floating	<p>TMDS inputs equalization control (internal pull-down~500KΩ)</p> <p>PEQ = LOW: Mid level EQ (Default)</p> <p>PEQ = HIGH: High level EQ</p> <p>PEQ = MID: Low level EQ</p>	Pin 3
High	<p>(Internal pull down~500KΩ)</p> <p>P10 = LOW: HPD = HPD_SINK @ 3.3V CMOS output</p> <p>P10 = High: HPD= HPD_SINK# (inverted HPD) @ 0.5V</p>	Pin 4
GND	<p>[ASQ1,ASQ0] = HL: No automatic squelch (internal pull down~500kΩ)</p> <p>LI: Automatic squelch enable, Level = 120mVpp, default timer</p> <p>LH: Automatic squelch enable, Level = 100mVpp, default timer</p> <p>HH: Automatic squelch enable, Level = 80mVpp, default timer</p> <p>ML: Automatic squelch enable, Level = 120mVpp, extended timer</p> <p>MH: Automatic squelch enable, Level = 100mVpp, extended timer</p> <p>LH: Automatic squelch enable, Level = 80mVpp, extended timer</p> <p>HM: Reserved</p> <p>MM: Reserved</p>	Pin 1
VCC		Pin 11
4.65K to GND	499R to GND	Pin 6
GND	<p>Automatic power down management (Internal pull up~500KΩ)</p> <p>APD = LOW: Automatic power down disable</p> <p>APD = HIGH: Automatic power down enable</p> <p>APD = MID: Reserved</p>	Pin 12
1.2K to GND	2.2uF to GND	Pin 10
GND	<p>EMI reduction and filter setting.</p> <p>(EMI1 internal pull up~500KΩ; EMI0 internal pull down~500KΩ)</p> <p>(EMI1,EMI0) = HL: No EMI reduction</p> <p>EMIO = HIGH: Reduced rise/fall time</p> <p>MID: Reduced rise/fall time, 2nd</p> <p>EMI1 = LOW: EMI filter setting 1</p> <p>MID: Reserved</p>	Pin 27
VCC		Pin 33
Note2	<p>DDC Active Buffer enable and setting (internal pull-down~500KΩ)</p> <p>DDCBUF = LOW: No DDC active buffer, passive DDC level shifting</p> <p>DDCBUF = HIGH: Active DDC buffer enable, setting 1</p> <p>DDCBUF = MID: Active DDC buffer enable, setting 2</p>	Pin 34
Floating	<p>TMDS output driver pre-emphasis level setting (internal pull down~500KΩ)</p> <p>PRE = LOW No pre-emphasis</p> <p>PRE = HIGH: Low level pre-emphasis is added</p> <p>PRE = MID: High level pre-emphasis is added</p>	Pin 35

**Note2: High is HPD logic inverted, Low is HPD logic non-inverted**

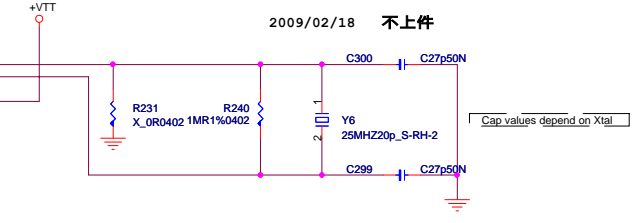
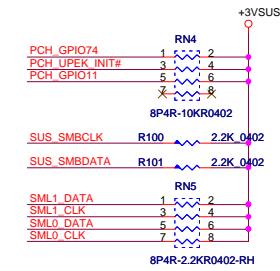
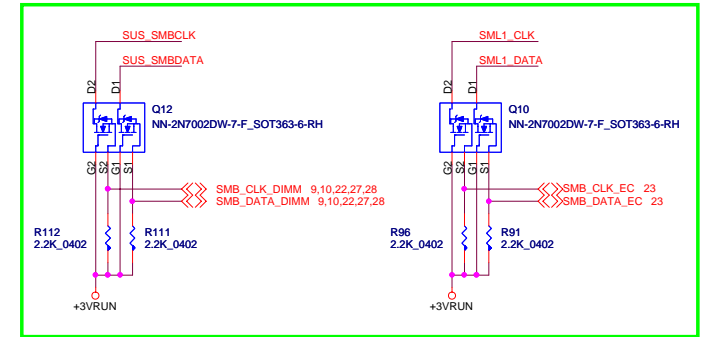
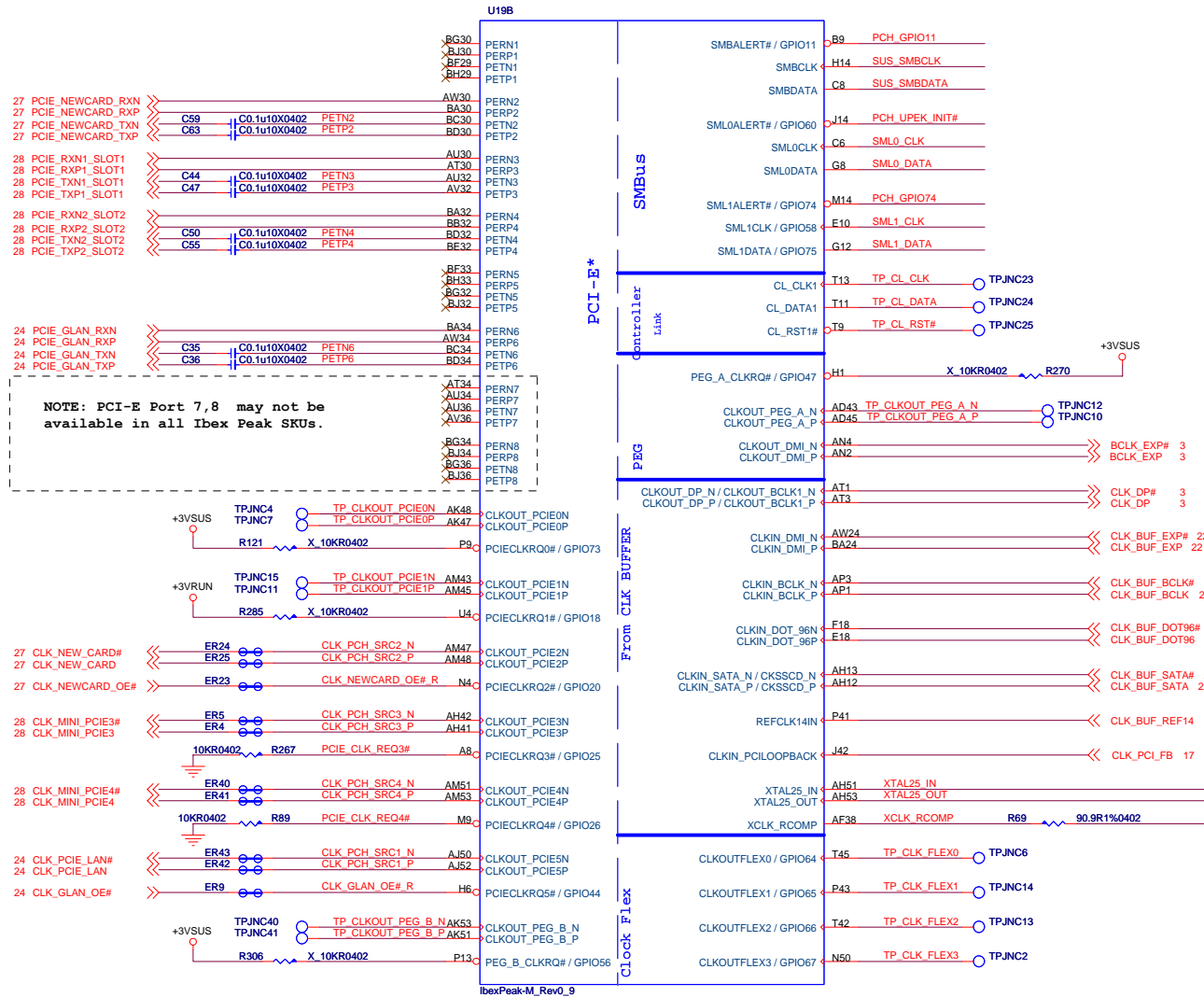




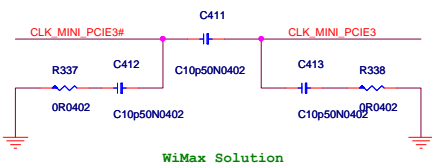
**IBEXPEAK - M (HDA, JTAG, SATA)**

PCH PIN	REFDES	ES2	STATE
TDO	R289	200 ohm	STUFF
	R271	100 ohm	STUFF
TMS	R298	200 ohm	STUFF
	R291	100 ohm	STUFF
TDI	R297	200 ohm	STUFF
	R290	100 ohm	STUFF
TCK	R273	51 ohm	STUFF
TRST#	R296	not applicable	NO STUFF
	R288	not applicable	NO STUFF

# IBEXPEAK - M (PCI-E, SMBUS, CLK)

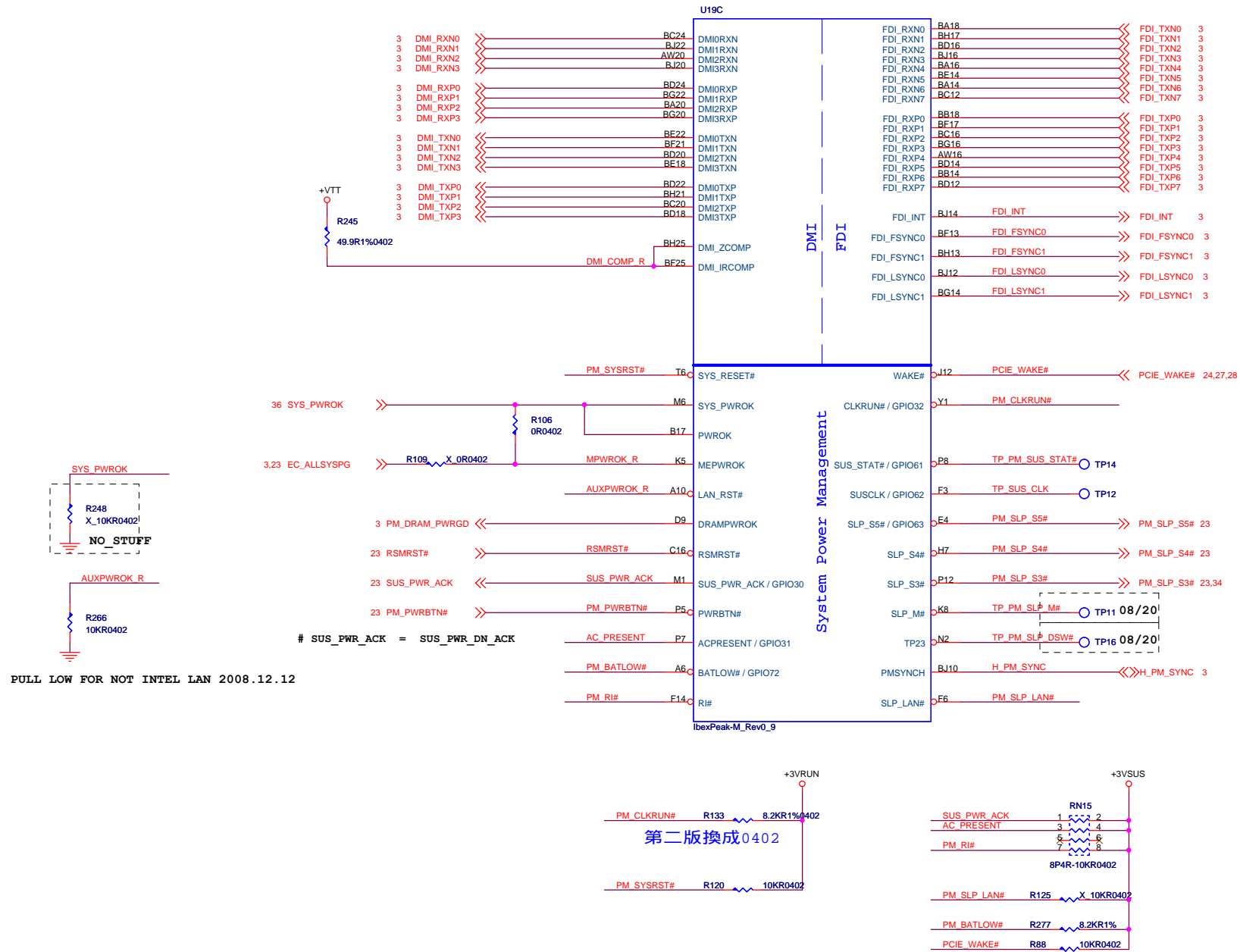


PCIECLKRQ1# / GPIO18	RUN Well
PCIECLKRQ1# / GPIO20	
PCIECLKRQ0# and PCIECLKRQ3# ~ PCIECLKRQ7#	
PEG_A_CLKRQ#	SUS Well
PEG_B_CLKRQ#	

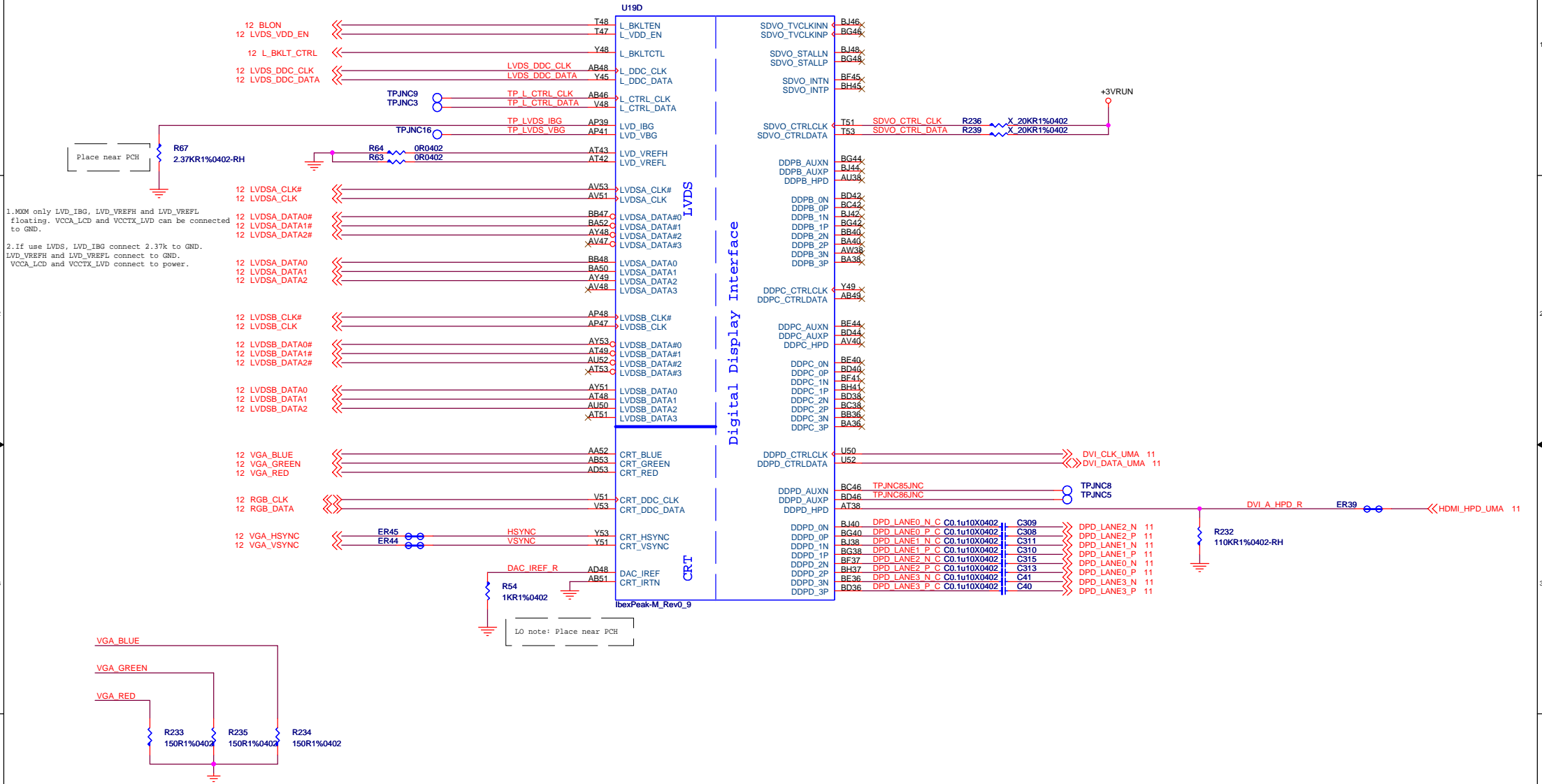


MICRO-STAR INT'L CO.,LTD.			
IBEXPEAK - M (PCI-E,SMBUS,CLK)			
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Custom	MS-1681	10	
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**IBEXPEAK - M (DMI,FDI,GPIO)**



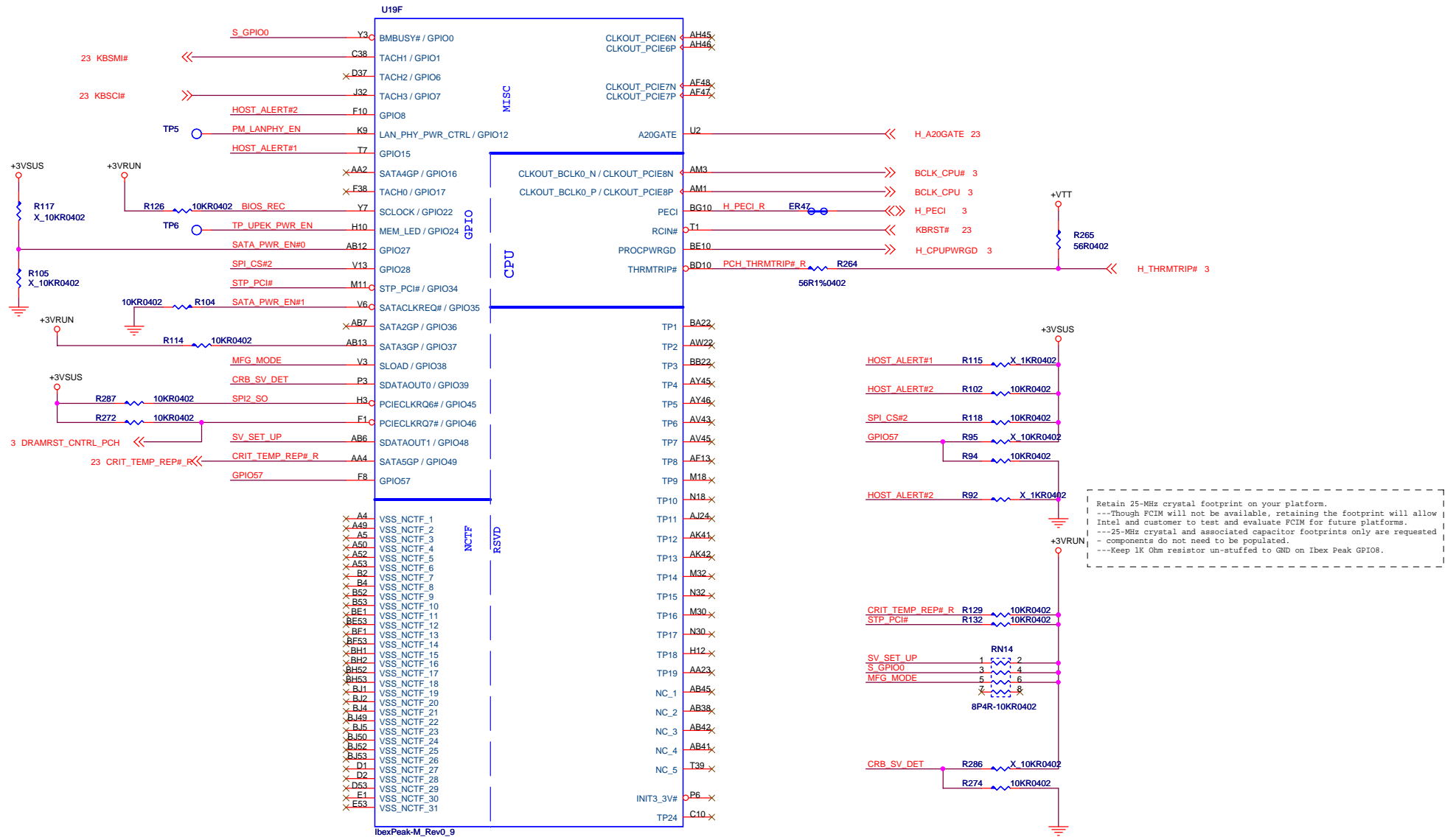
# IBEXPEAK - M (LVDS,DDI)



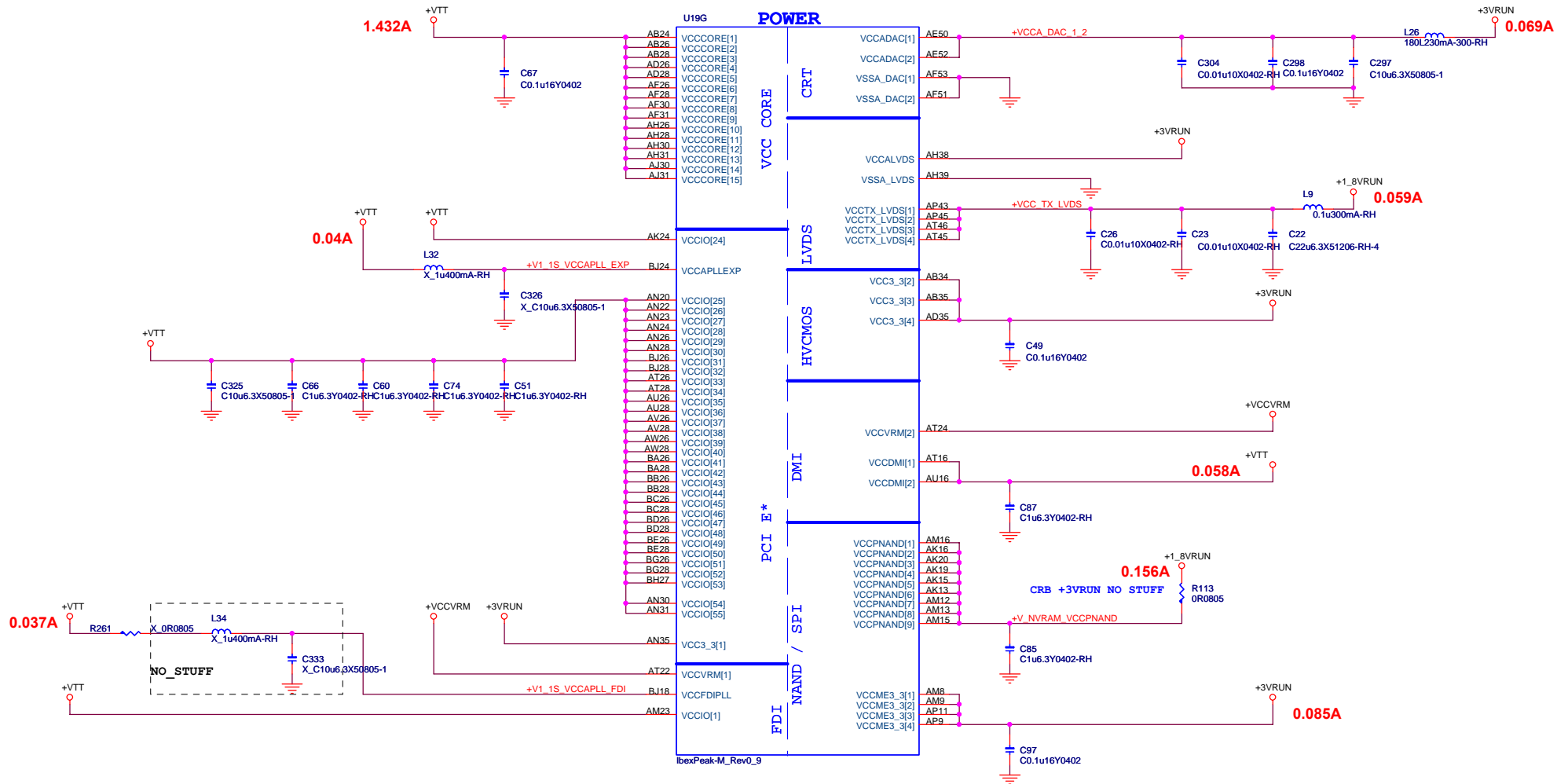




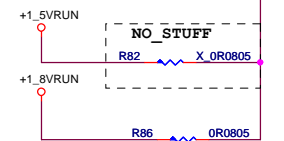
# IBEXPEAK - M (GPIO,VSS\_NCTF,RSVD)

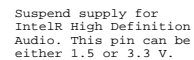


# IBEXPEAK - M (POWER)

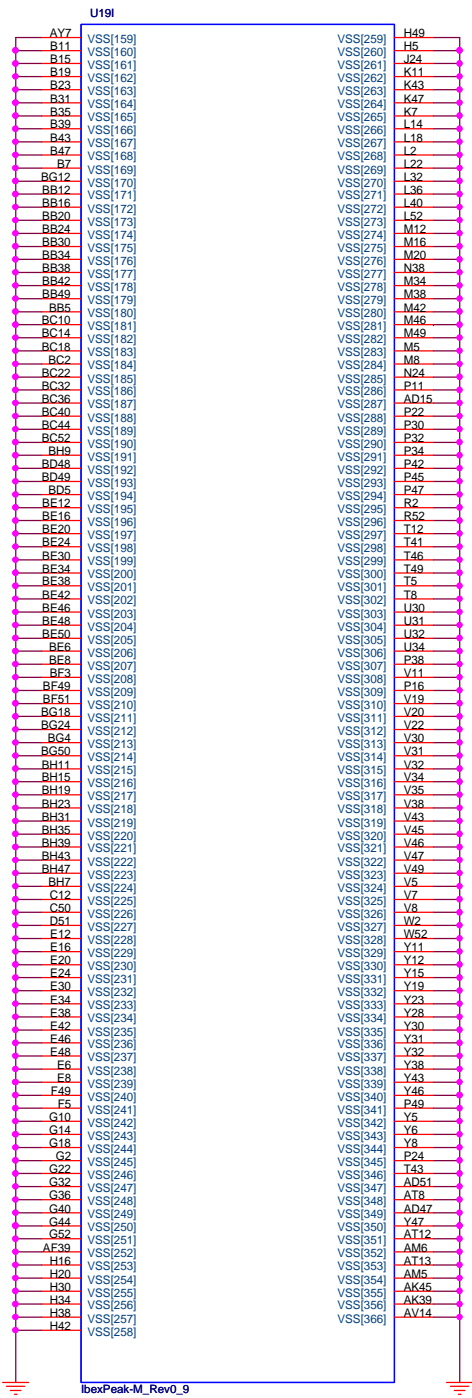
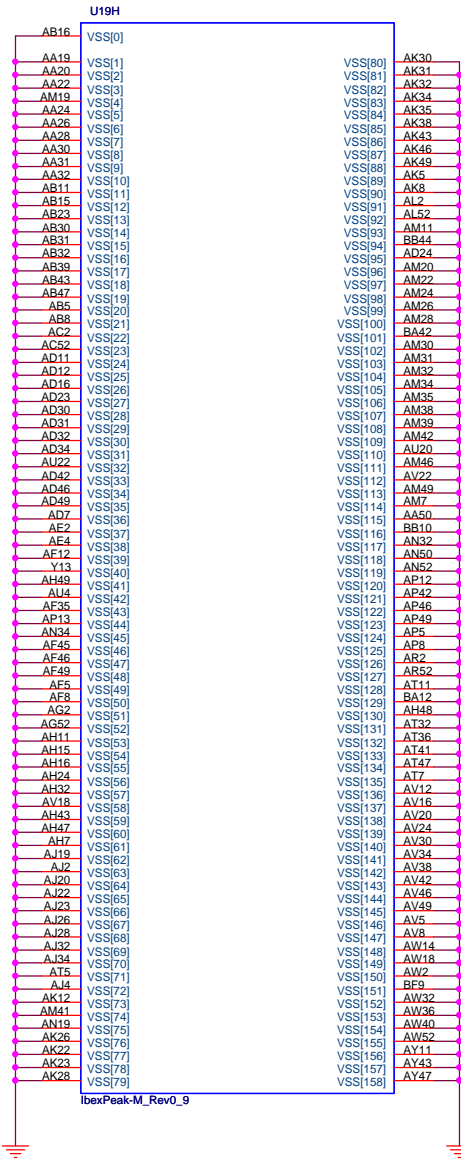


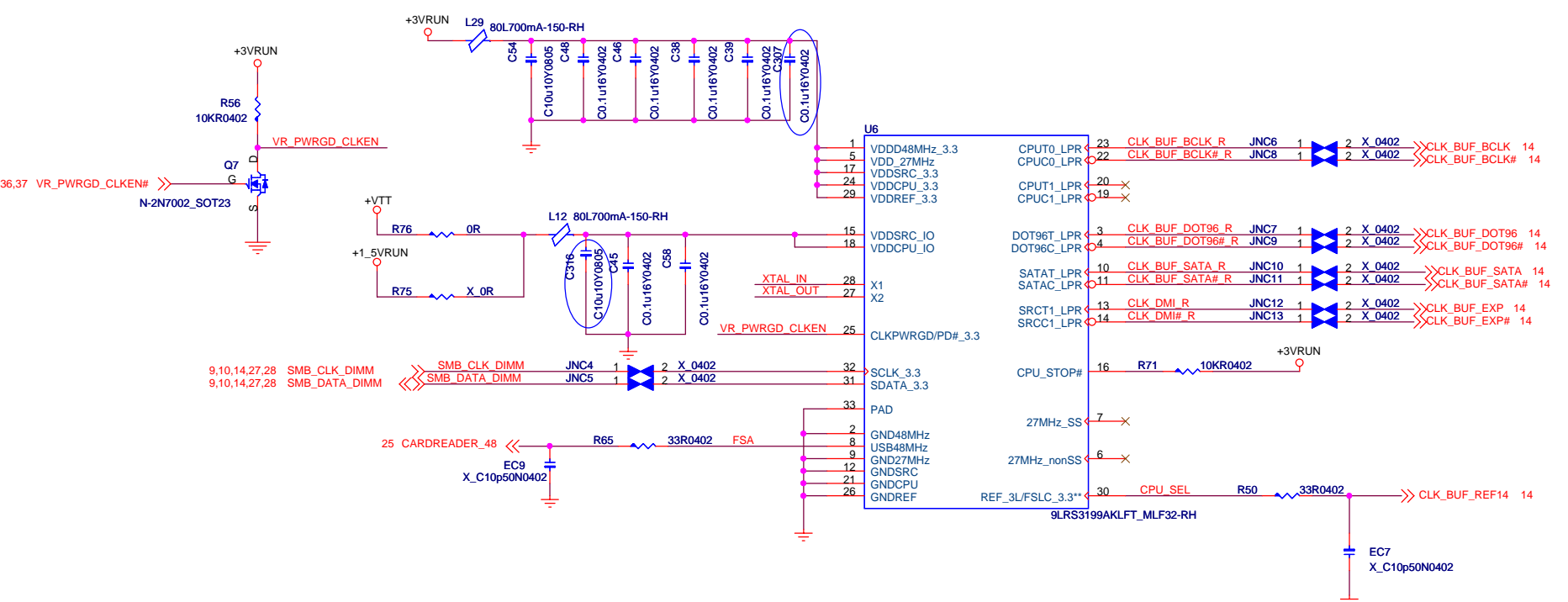
The VCCVPM rail (1.8 V/1.5 V) powers an internal voltage regulator module (VRM) that regulates clean 1.05-V voltage supply for analog rails (VCCAClk, VccapllEXP, VCCFDIPLL, and VCCSATAPLL). This solution will allow us to remove the LC filter requirements for those rails, thereby reducing platform BOM cost. VCCVPM is enabled by default via internal pull up to GPIO27, therefore GPIO27 should be left as No Connect. The following diagram shows implementation details on how to enable and disable VccVRM.



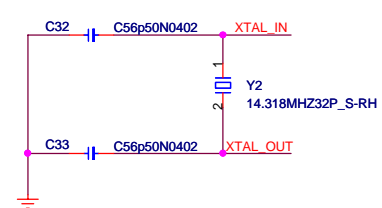
**IBEXPEAK - M (POWER)**

IBEXPEAK - M (GND)

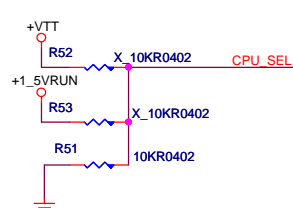




**Capacity select**  
If LC=20pf C708/C709=33pf  
If LC=32pf C708/C709=56pf



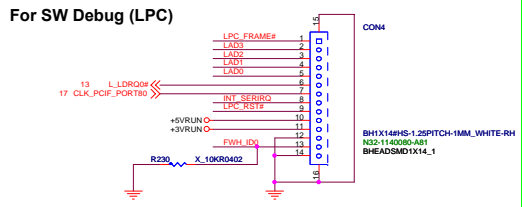
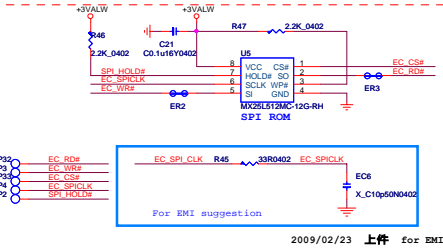
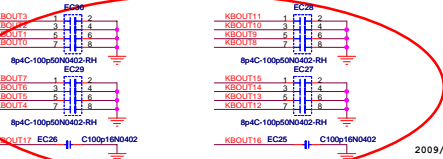
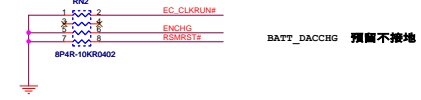
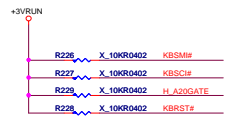
**For CPU frequency select (133MHz)**



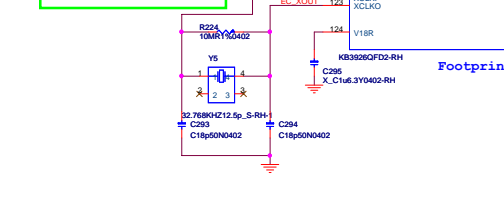
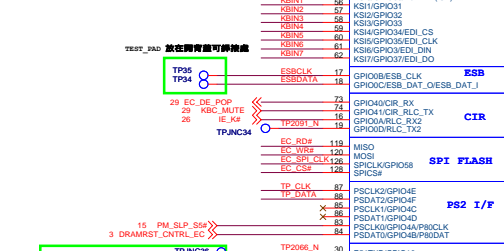
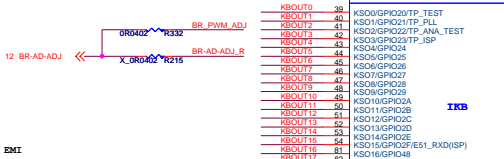
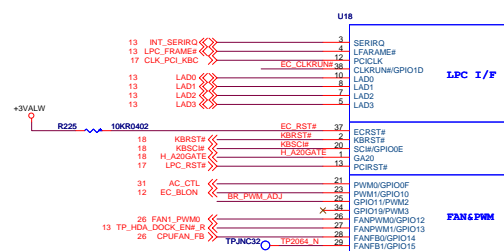
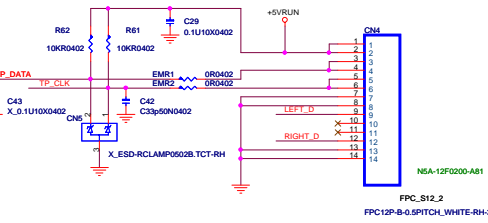
CPU_SEL	CPU0	CPU1
0(Default)	133MHz	133MHz
1(1.05~1.5V)	100MHz	100MHz

**Co-Lay Note:**

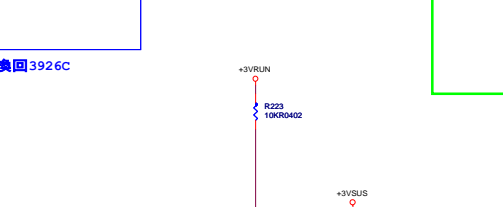
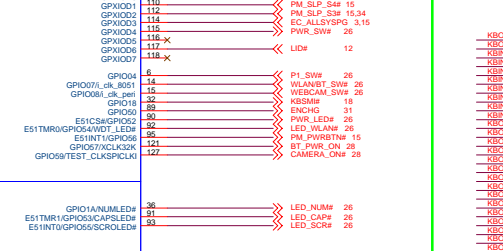
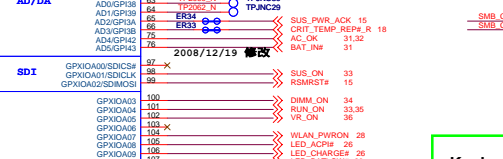
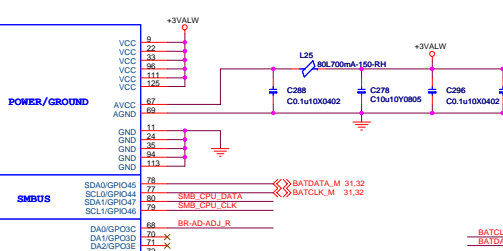
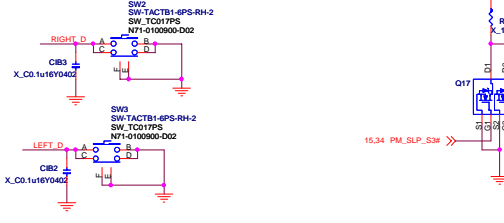
For IDT IC9IRS3199  
R598,R599,R600=10Kohm  
  
For Sillego SLG8SP587  
R598,R599,R600=4.7Kohm



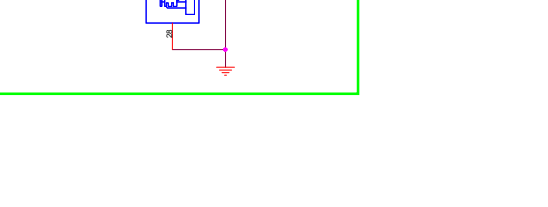
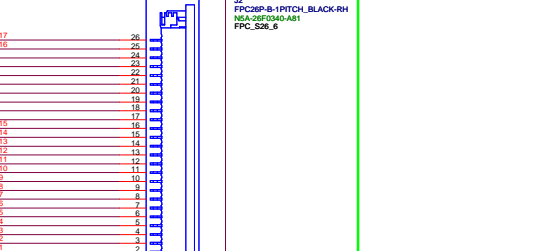
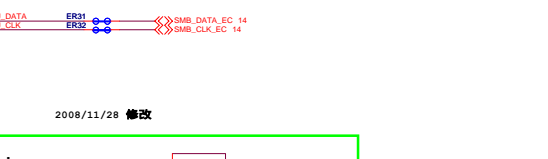
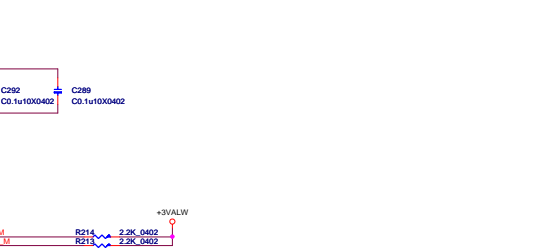
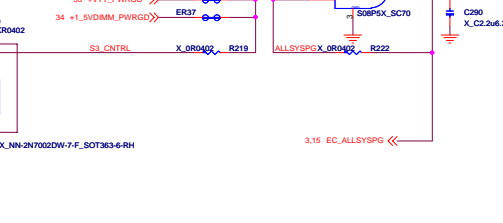
# Touch Pad



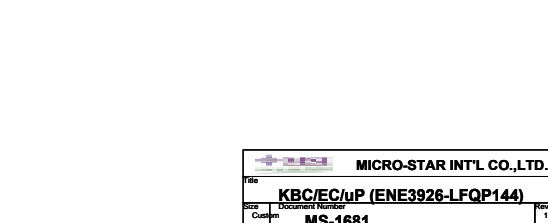
# Footprint:換回3926C



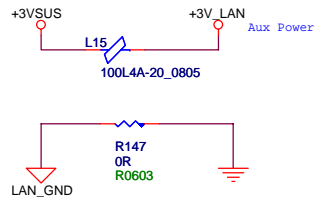
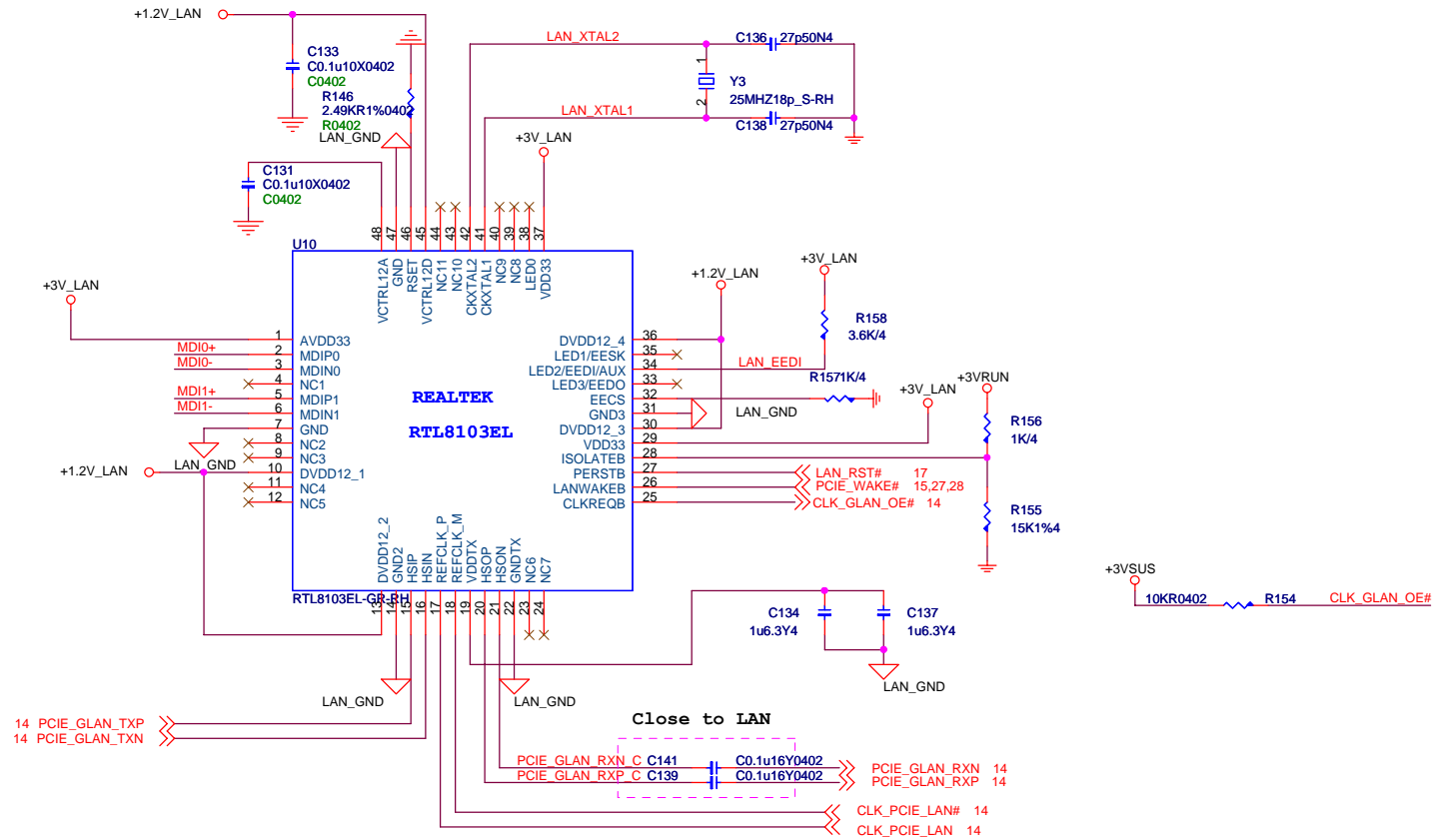
# LED



# Keyboard conn

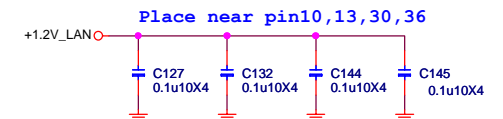
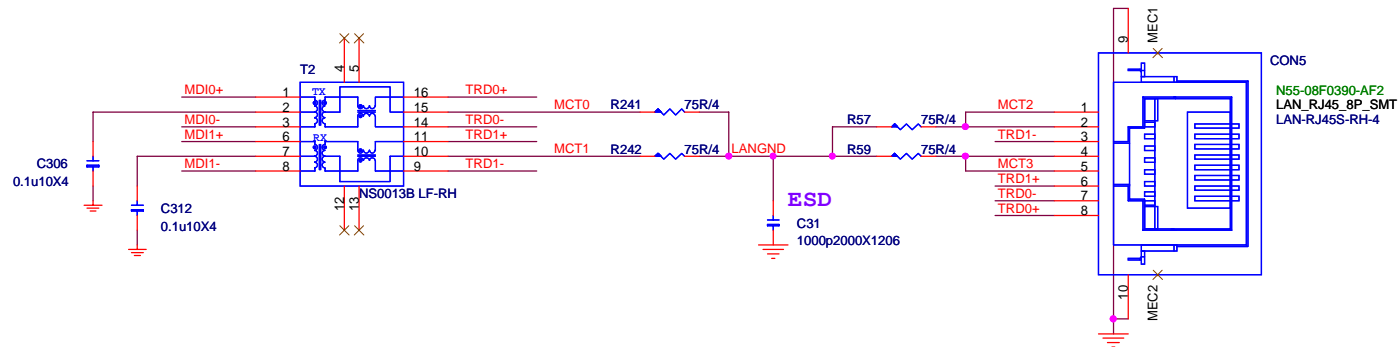
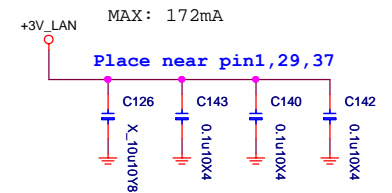


1. Pin 46 : RSET res should be close to LAN chip. Don't have power trace or high frequency trace beside it.
2. The trace of each Pair(MDIX+/-) should be equal in length and better have ground under.
3. Both EGND and GND can be connect together or use 0 Ohm res. to connect them.
4. 1.2V請留 power plane並且盡量大一點.
5. 1.2V Bypass 電容不能省. 在 LAN 的每一個 power pin 都加 0.1u 的電容, 不能省.
- 6.請參考RTL8111c EMI layout notice. Fine tune cap (0.1uF ~ 10pF) of center-tapped can improve EMI for single tone noise.
7. Please refer and follow our Layout Guidel.5 as attached file
8. RJ45 的部份,對應pin 請您在confirm一下.....一般都是接到 RJ45 pin 12/ 36



## POWER Comparison

	3.3V	mW
10 M Idle/TxRx	87/172	287/568
100 M Idle/TxRx	112/165	370/545
ALDPS	60	198
D3 cold with link10M /without link	32/18	106/59.4

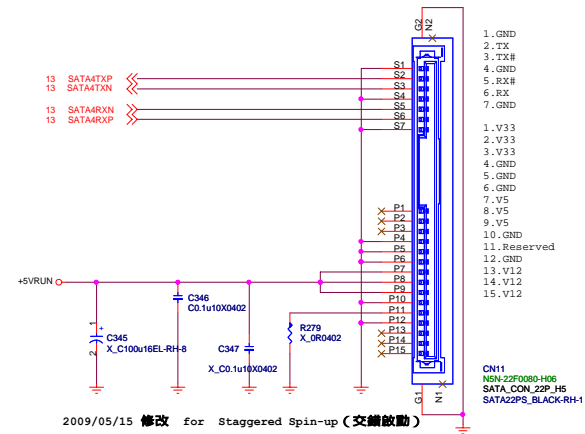




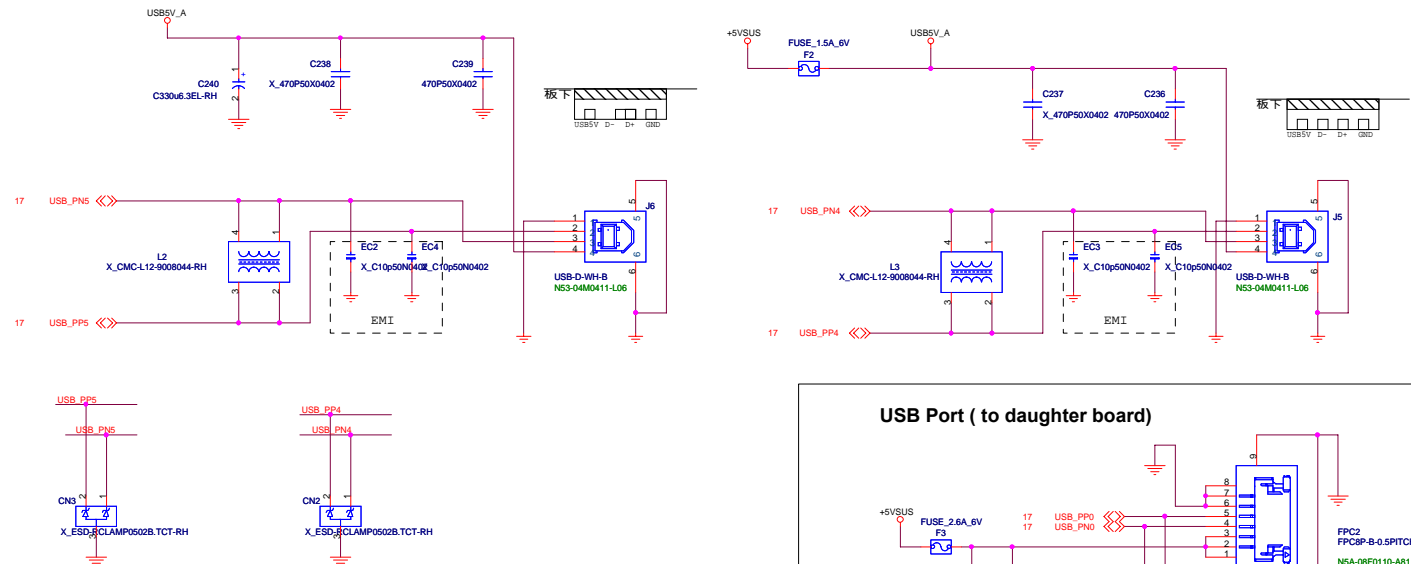




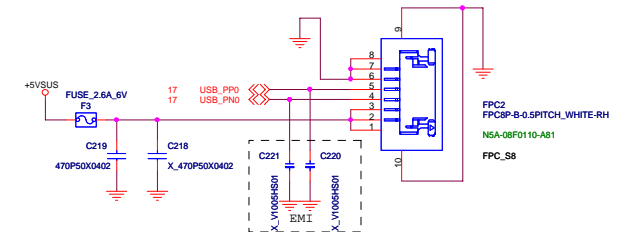
## SATA HDD



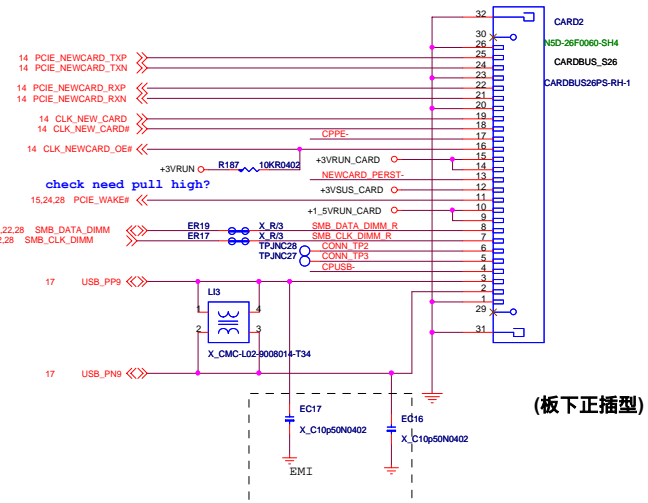
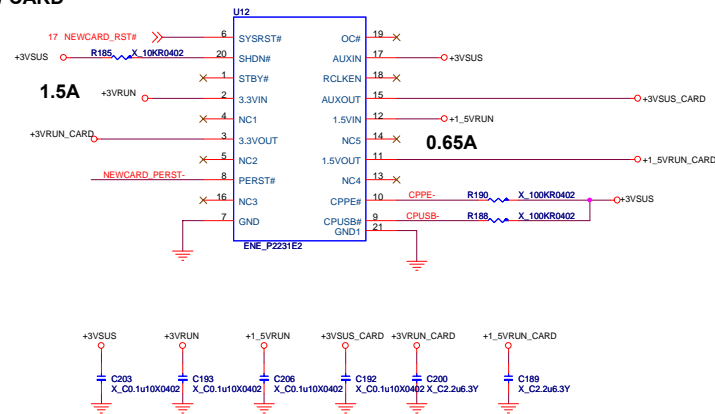
### USB Port



**USB Port ( to daughter board)**

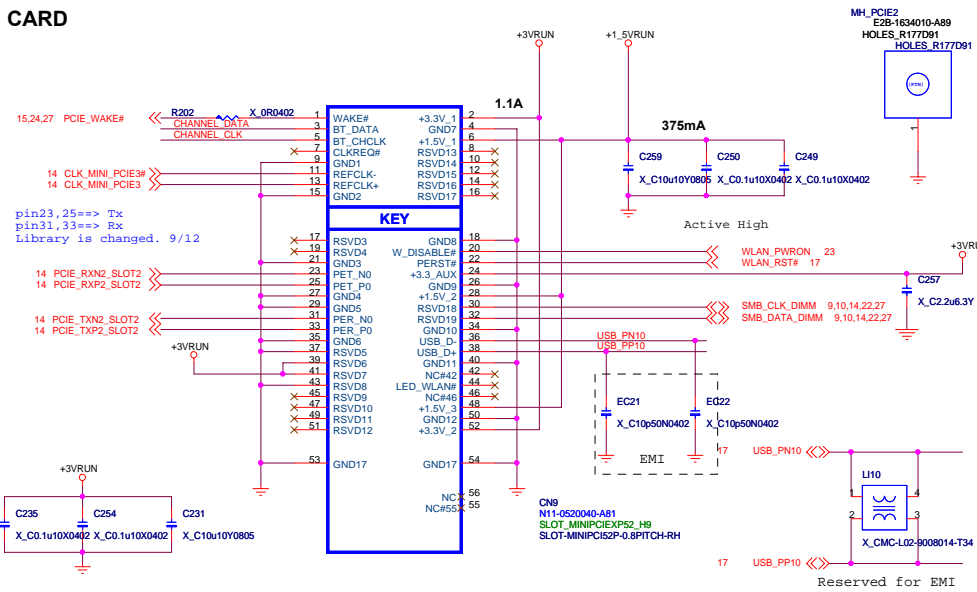


## NEW CARD

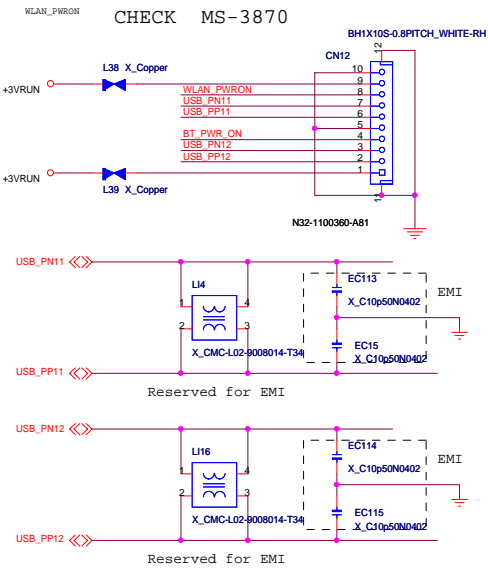
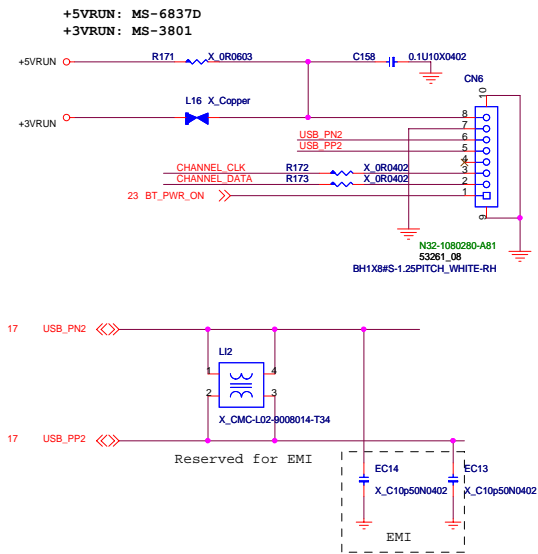


(板下正插型)

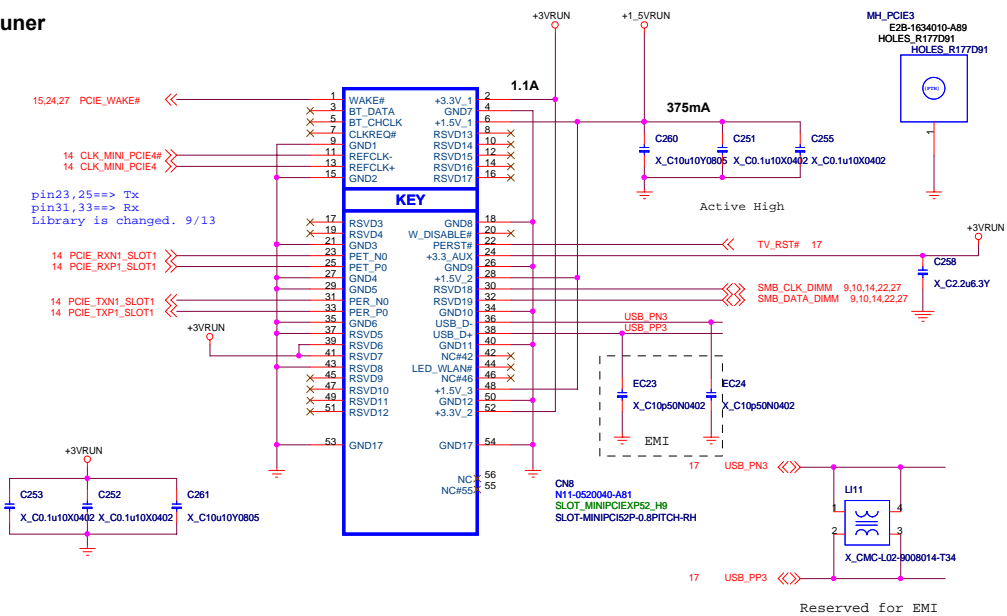
## WLAN CARD



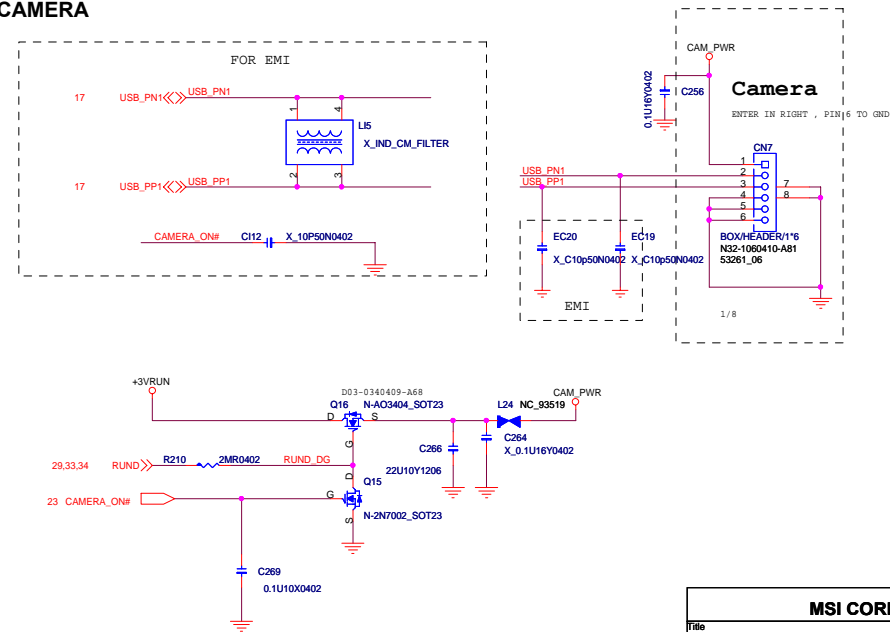
## BLUETOOTH

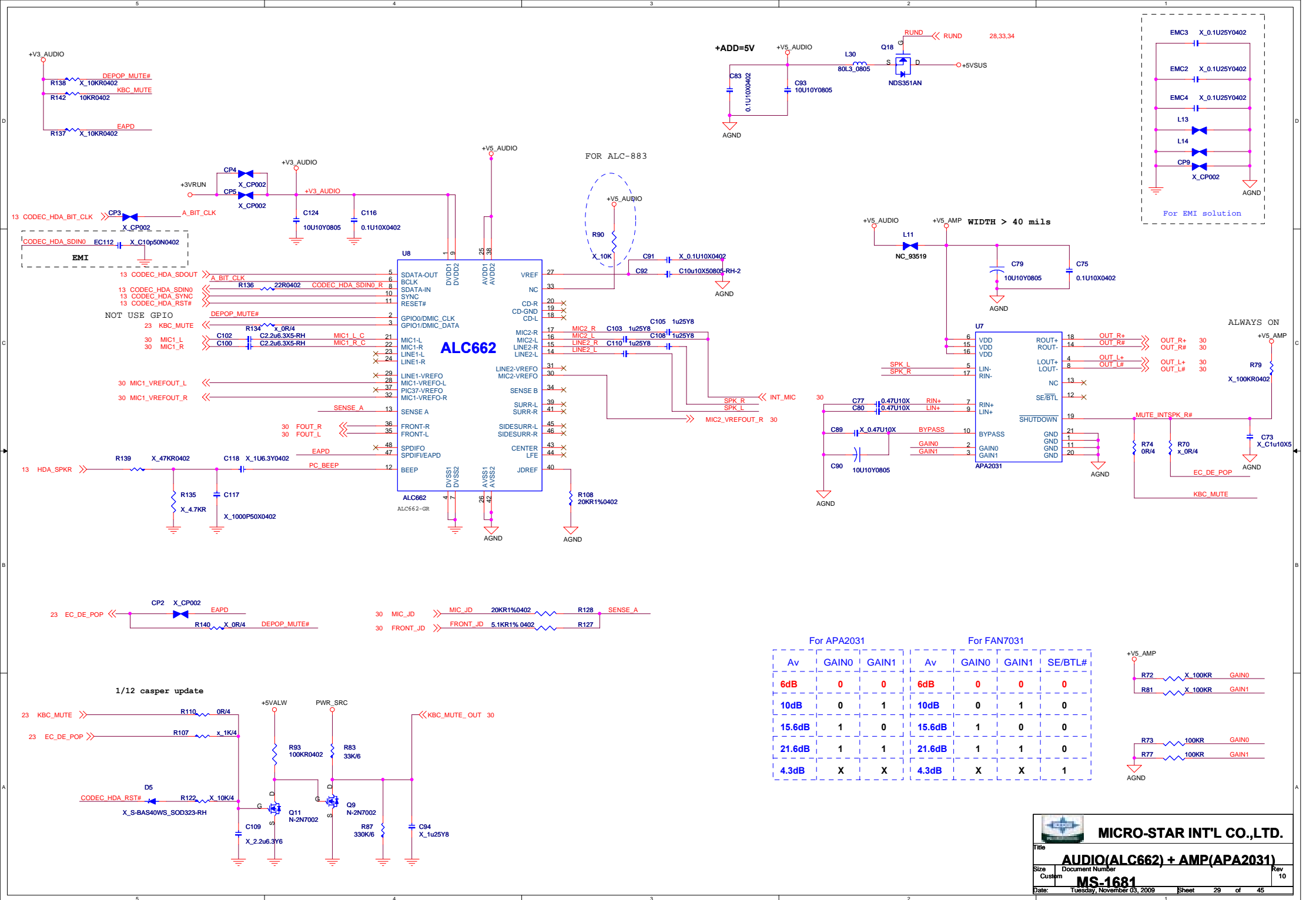


## TV Tuner



## CAMERA



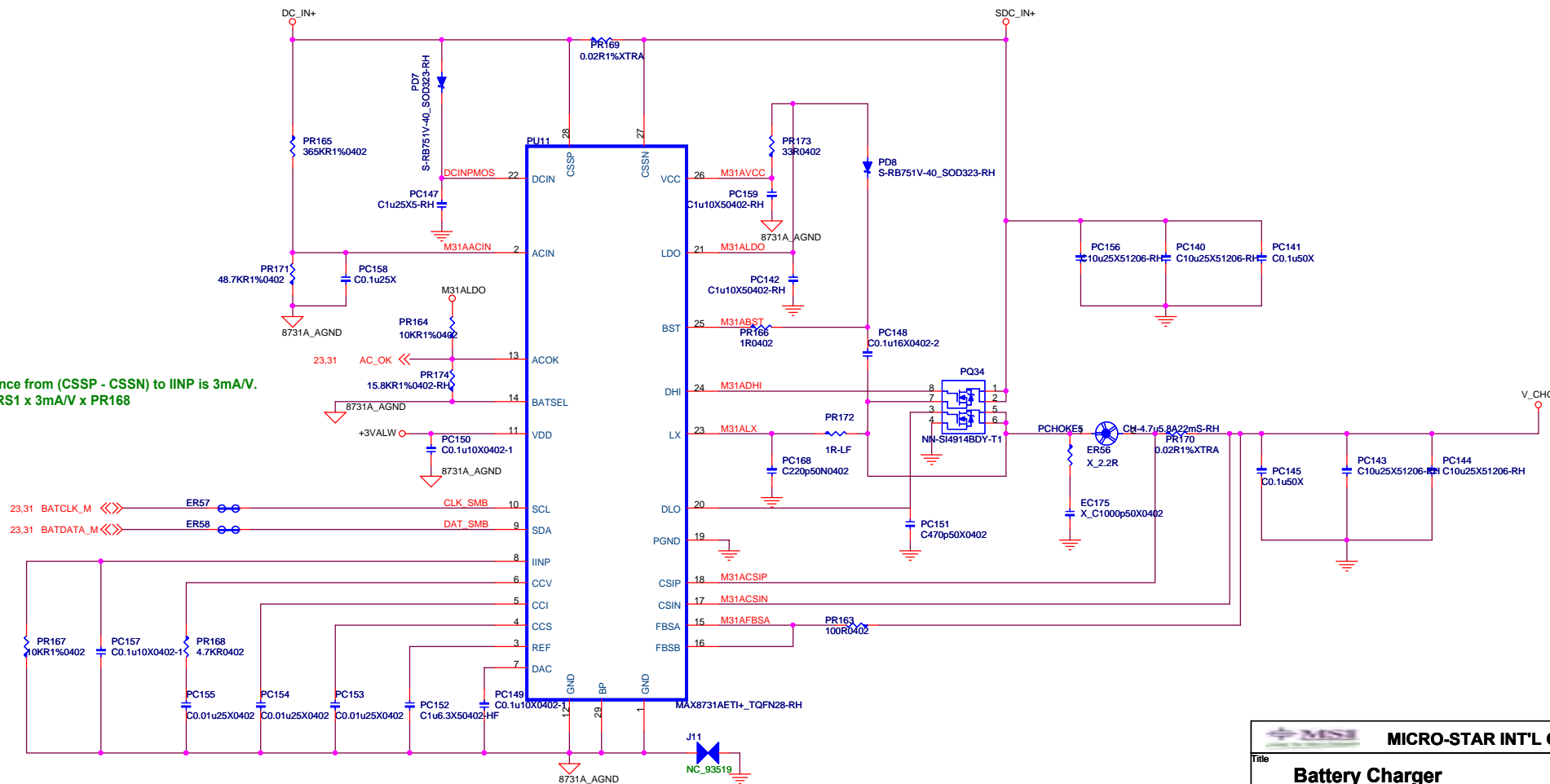






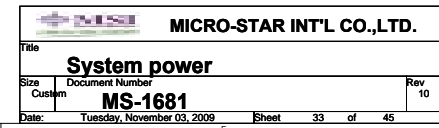
Adapter= 65W  
Adapter input voltage set 19 Voltage

IINP :  
1. The transconductance from (CSSP - CSSN) to IINP is 3mA/V.  
2.  $V_{IINP} = IINPUT \times RS1 \times 3mA/V \times PR168$



MICRO-STAR INT'L CO.,LTD.			
Title			
Battery Charger			
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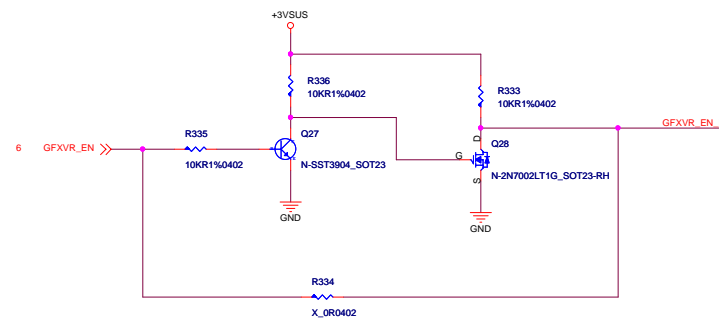
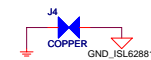




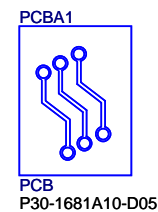
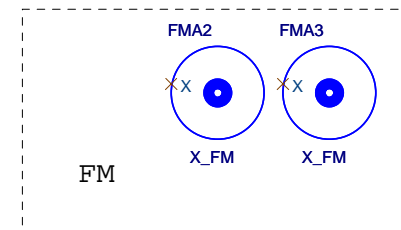
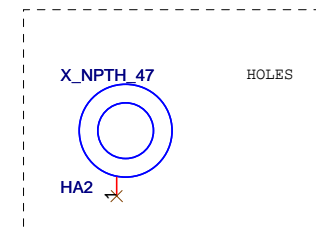
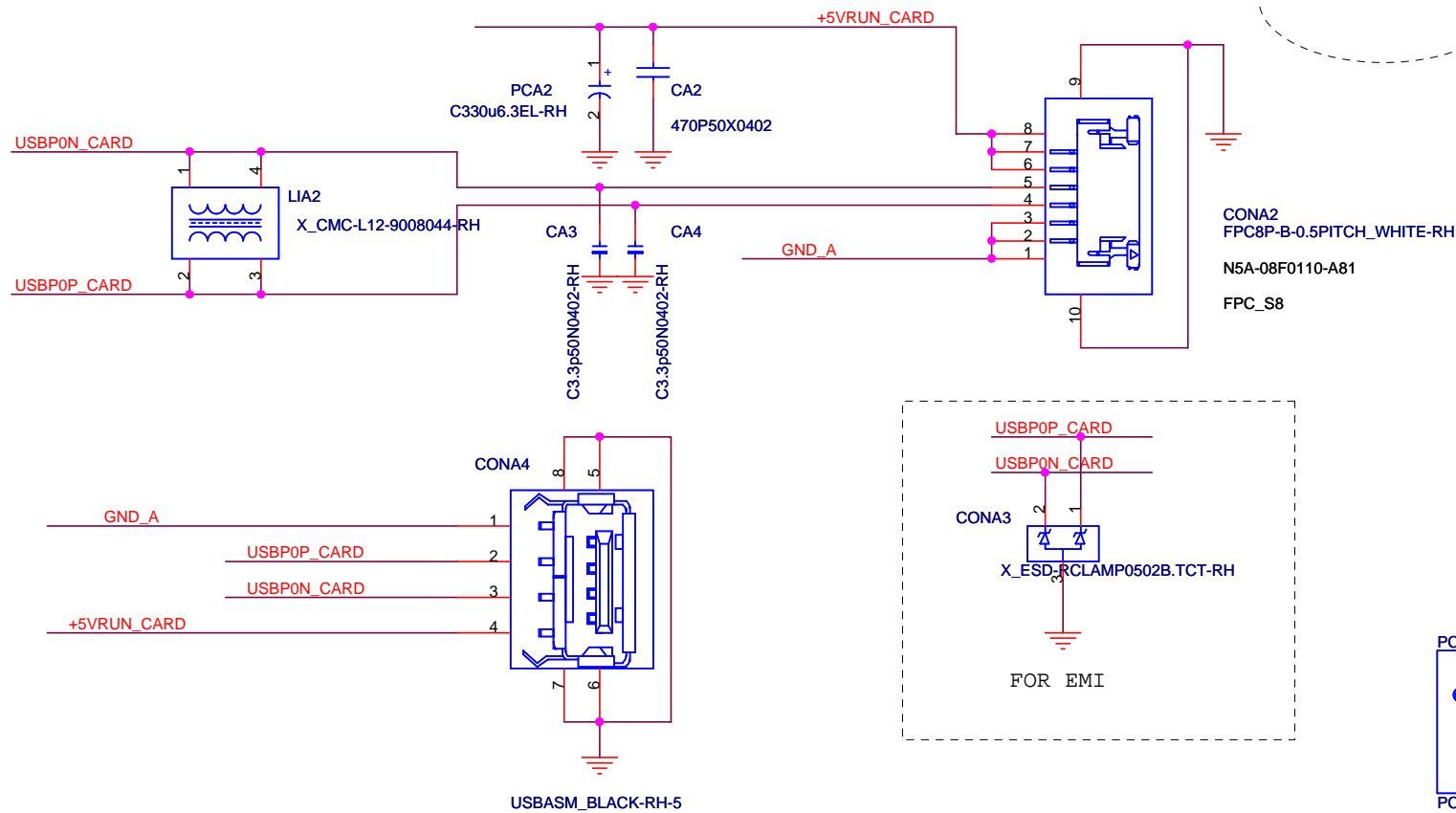







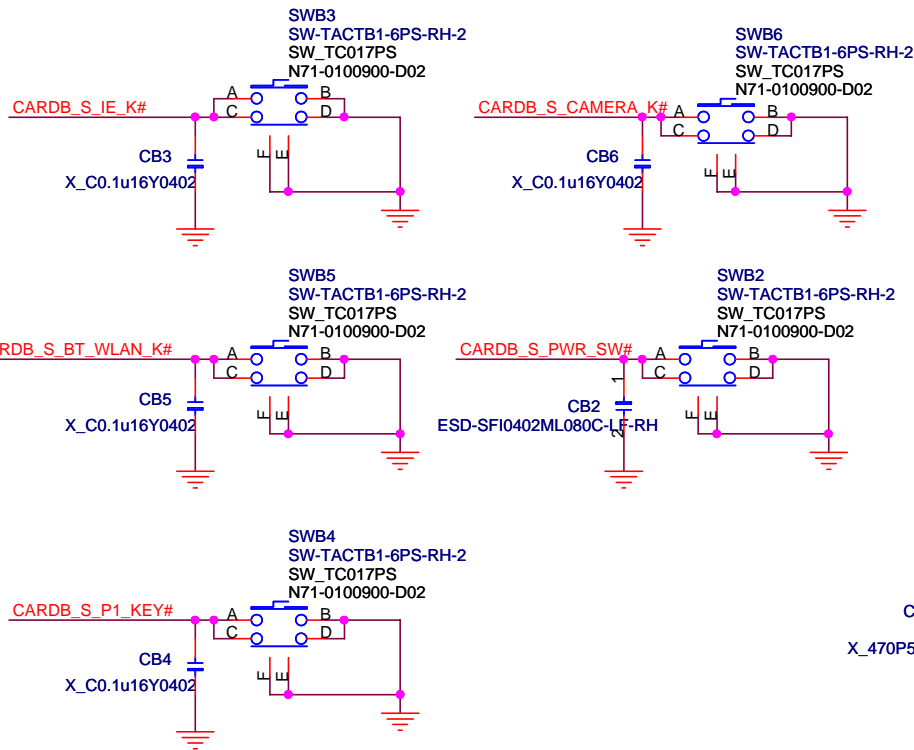






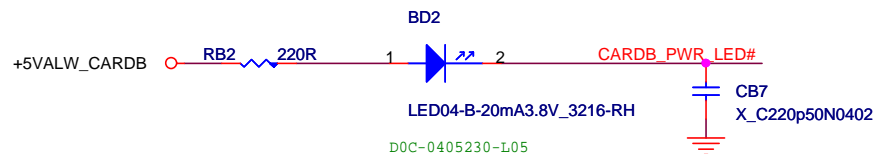
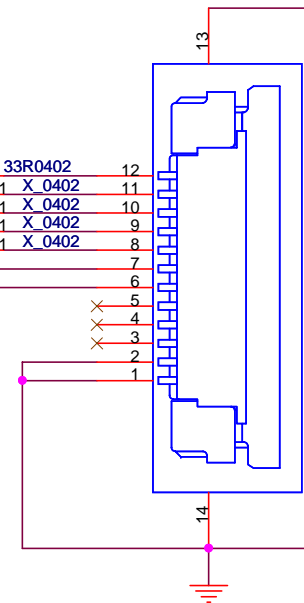
P30-1681A10-H73, 瀚宇博德 (薩摩亞)  
P30-1681A10-D05, 昆穎 (定穎大陸)

 <b>MICRO-STAR INT'L CO.,LTD.</b>		
Title		
<b>USB BOARD A</b>		
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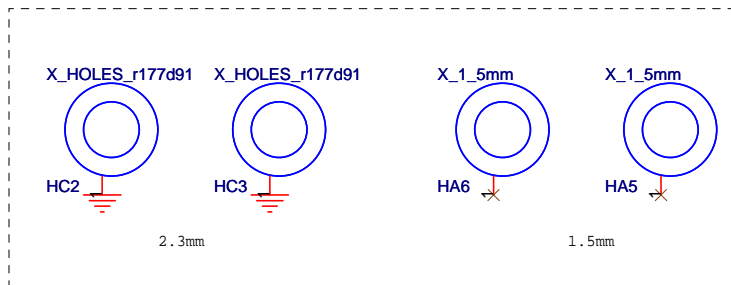
## CARD\_B\_ BOTTOM

CARDB_S_PWR_SW#	RB3	33R0402	12
CARDB_S_BT_WLAN_K#	JNCB5	2	1 X 0402
CARDB_S_CAMERA_K#	JNCB6	2	1 X 0402
CARDB_S_IE_K#	JNCB3	2	1 X 0402
CARDB_S_P1_KEY#	JNCB4	2	1 X 0402
CARDB_PWR_LED#			7
+5VALW_CARDB			6




MYLAR2  
MYLAR\_BOTTOM\_TOP  
E2M-6811111-G40

MYLAR3  
MYLAR\_BACK  
E2P-6811311-G40



PCBA2  
PCB  
P30-1681B10-D05

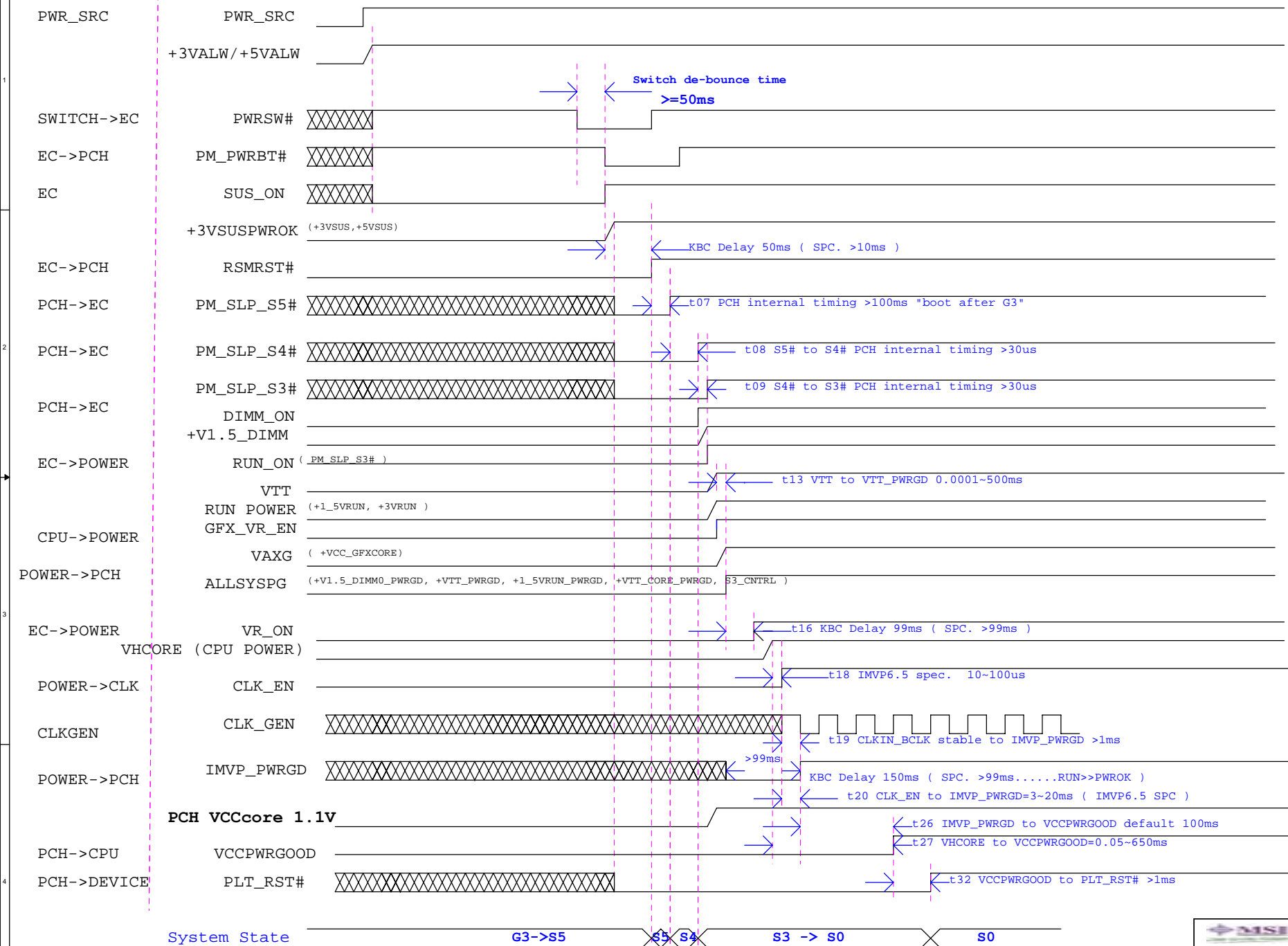
P30-1681B10-H73, 瀚宇博德 (薩摩亞)  
P30-1681B10-D05, 昆穎 (定穎大陸)

		<b>MICRO-STAR INT'L CO.,LTD.</b>		
Title				
<b>Lauch Board_B</b>				
Size	Document Number			Rev
Custom	<b>MS-1681</b>			10
Date:	Tuesday, November 03, 2009	Sheet	40	of 45

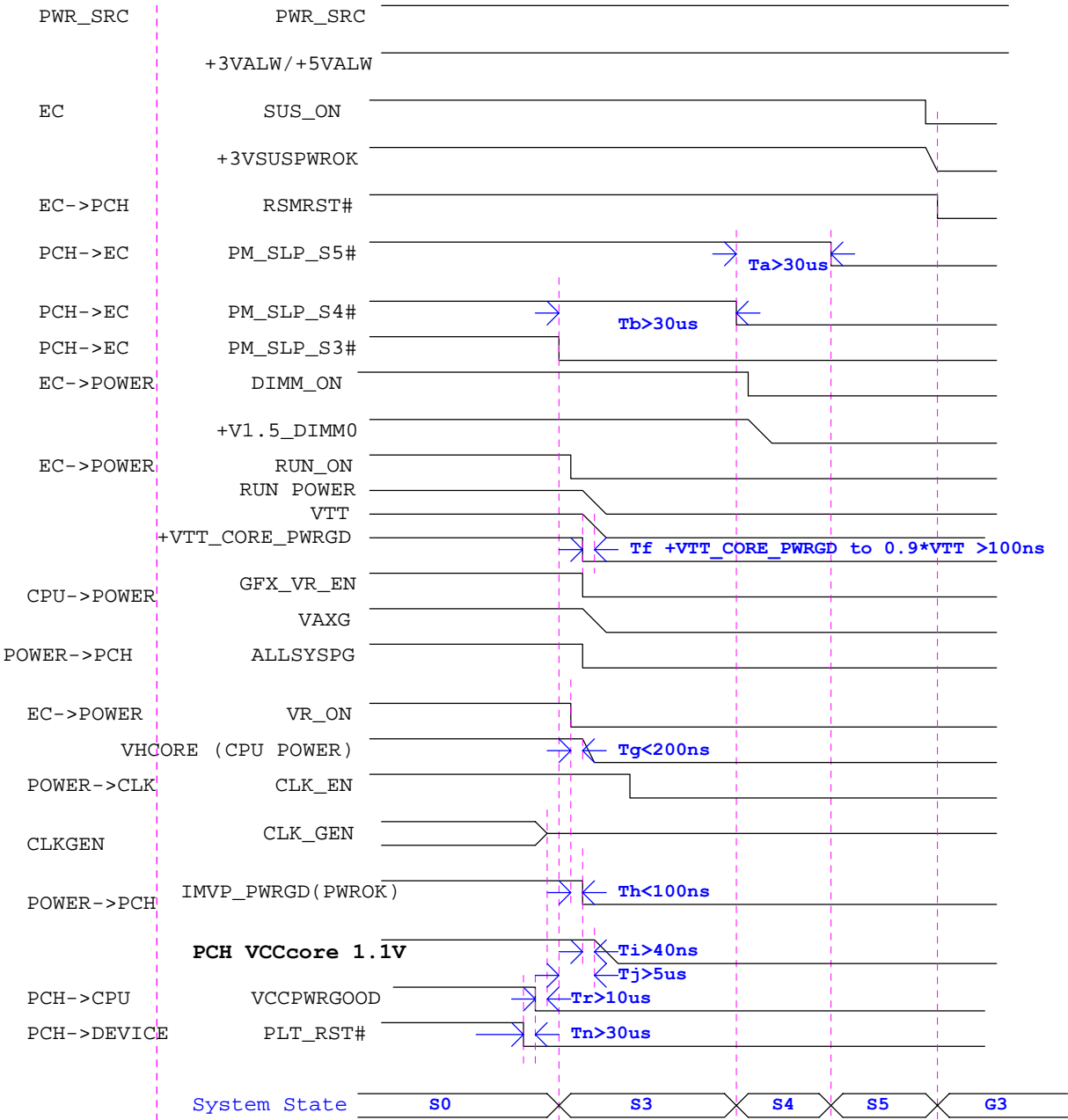


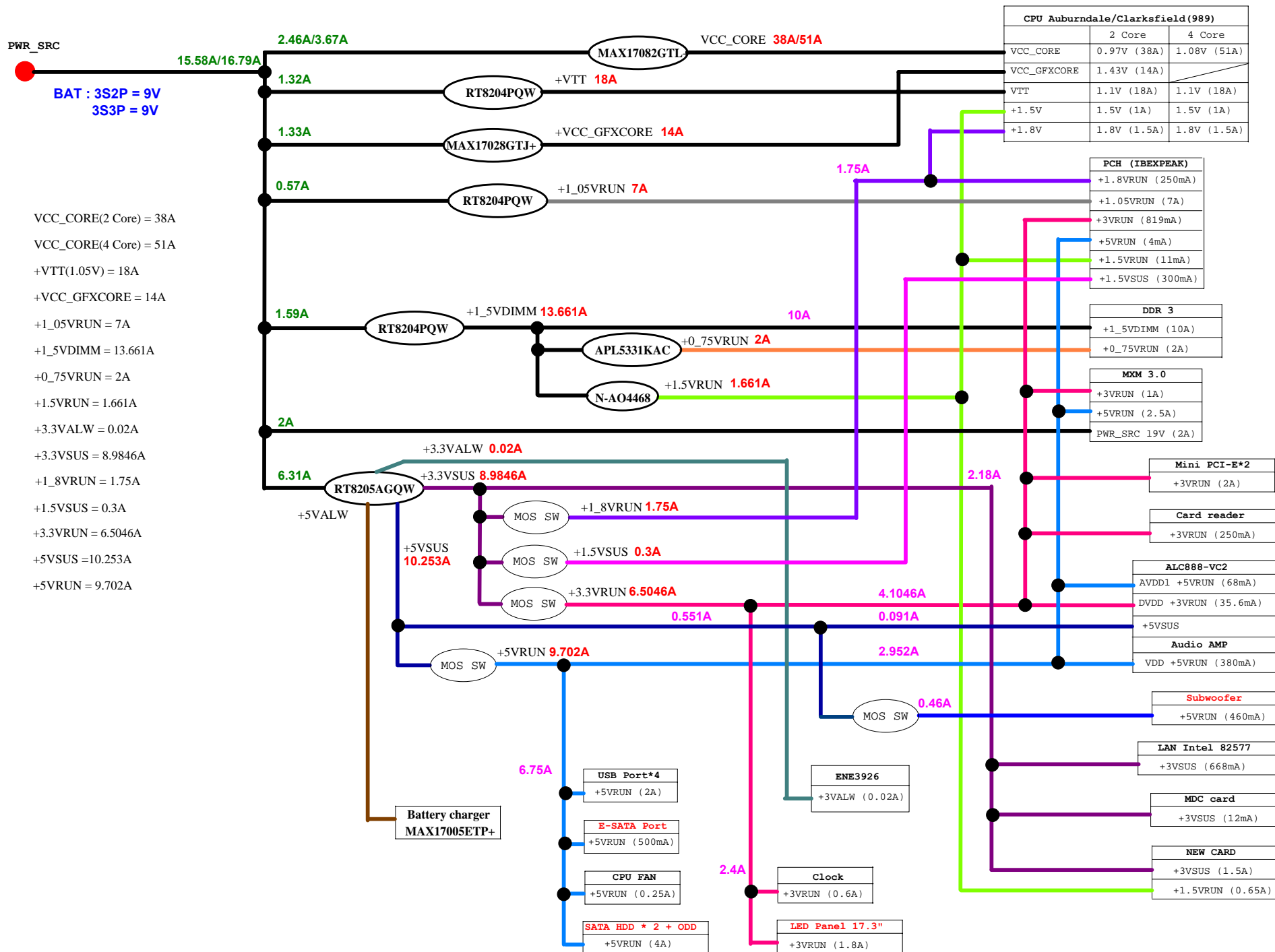


## Calpella System Power on Sequence DC mode



Power down Sequence DC mode S0 to G3





2008/11/13 修改


# Change Note :

## 0A-->0B

- 1.P19 stuff R113 & C85 for intel document about Braidwood
- 2.P23 add one PWM Pin for co-lay LED panel by EC
- 3.P25 Change CardReader to ENE
- 4.P26 Change "LED\_HDD#" PU +5VRUN to +3VRUN
- 5.P26 Fan conn footprint change back to "53398\_03"
- 6.P28 Add Wireless & Bluetooth combo(MS-3870)
- 7.P32 Change PR171 to 48.7K & PR172 to 1R0603
- 8.P33 Change PU2 from "UP6182AQAG" to "TPS51125" & PR18 to 30K
- 9.P34 Change PU9 from "UP6111AQDD" to "UP6128A" & PR156 to 3.48K & PR159 to 10.7K & PQ10 to "D03-0443033-V02"
- 10.P35 Change PU8 from "UP6111AQDD" to "UP6128A" & PR149 to 4.22K & remove C394
- 11.P36 Change PR95 to 1.82K & PR29 to 9.31K & PC90 to 47nf & PR99 to 931R & no stuff PC84 , PR94 , PEC4 , PEC5 , PEC6 , PEC8

## 0B-->10

- 1.P13 add net "TP\_HDA\_DOCK\_EN#\_R" for flash protect control.
- 2.P14 add wimax ac adepter schematic.
- 3.P23 add ENE GPIO13 for flash protect control.
- 4.P25 no stuff C399 & C400 for cardreader detect issus.
- 5.P26 change R307 from 0R to 33R for EMI.
- 6.P31 add 2 cap in +VBATA for EMI.
- 7.P34 change R329 from 0R to 1K for current limit.
- 8.P37 no stuff +VCC\_GFXCOPE PQ23 no cost down.
- 9.P40 change JNCB2 to RB3 , and 33R for EMI.
- 10.P40 change CB2 from 0.1u to 300p for EMI.

		<b>MICRO-STAR INT'L CO.,LTD.</b>	
Title			
<b>NOTE</b>			
Size	Document Number		Rev
Custom	<b>MS-1681</b>		10
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