S/M No:OSDMK42001

Service Manual

Model : DM-K42

Caution

: In this Manual, some parts can be changed for improving, their performance without notice in the parts list.

DAEWOO ELECTRONICS

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1. General Section

1.1. Cautions/Warnings

1.1.1. Product Safety Notice

Parts marked with the symbol ⚠ in the schematic diagram have critical characteristics.

Use ONLY replacement pares recommended by the manufacturer. It is recommended that the unit be operated from a suitable DC supply or batteries during initial check out procedures.

1.1.2. Leakage Current Check/Resistance Check

Before returning the unit to the customer, make sure you make either (1) a leakage current check or (2) a line to insulated resistance check.

If the leakage current exceeds 0.5 milliamps, or if the resistance from chassis to either side of the power cord is less than 240 K ohms, the unit is defective.

WARNING: DO NOT return the unit to the customer until the problem or located and corrected.

1.2. Safe Warnings

1.2.1. Protection of Eyes from Laser Beam

To protect eyes from invisible laser beam during servicing

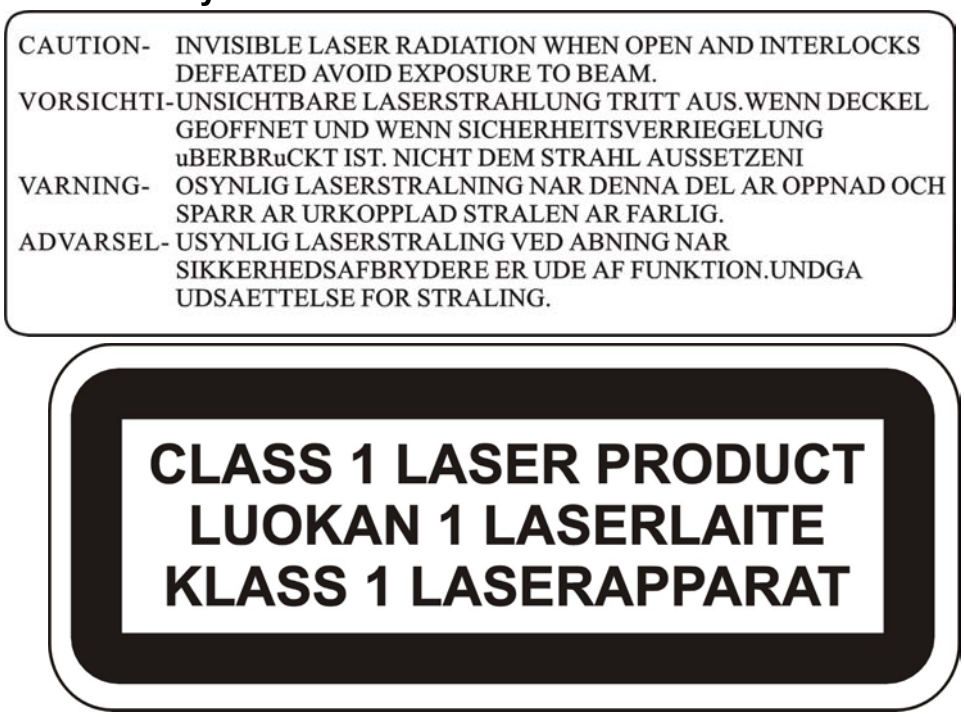
DO NOT LOOK AT THE LASER BEAM

1.2.2. Laser Caution

CAUTION

Adjusting the knobs, switches, and controls, etc. or taking actions not specified herein may result in a harmful emission of laser beams. This CD Changer must be adjusted and repaired only by qualified service personnel.

Laser symbol:



THIS IS COMPACT DISC PLAYER IS CLASSIFIED AS A CLASS 1 LASER PRODUCT.

THE LASS 1 LASER PRODUCT LABEL IS LOCATED ON THE REAR EXTERIOR.

1.3. Precautions

1.3.1. ESD Precautions in Repairing

1.3.1.1. Do not apply excessive pressure on the mechanical parts (moving pares), including the Pickup Block, as extremely high mechanical precision or required in these parts.

1.3.1.2. When soldering the microprocessor and signal processing IC's, use a ceramic soldering iron or a soldering iron whose metal part is grounded since they are not resistant to static electricity.

1.3.1.3. When removing the solder or soldering the laser shorting lands for the Pickup Block, use a ceramic soldering iron or a soldering iron whose metal part is grounded since the

laser diode or not resistant to static electricity.

1.3.2. DVD Loading Unit Precautions when handling the Mechanism Block

1.3.2.1. Do not loosen any screws in the Pickup Block.

1.3.2.2. Do not adjust any screws in the Mechanism Block except for “Tilt Adjust Screws”, as they are adjusted precisely at the factory.

1.3.2.3. Replacement of the Pickup Block is impossible. Always replace the Traverse Ass’y when the Pickup Block needed to be replaced. Do not touch the lens or lens holder of the Pickup Block.

1.3.2.4. The Guide Rails of the Pickup Block are greased. Take care when handing.

1.3.2.5. When you try to slide the Pickup Block, do not press or pull it directly. Always turn the dive gears with your fingers.

1.3.2.6. Be sure that the anti-slipping rubber on the turntable or clean. If there is dust or it is greasy, clean the part with the liquid that contains 50% each of alcohol and water.

1.3.2.7. When removing the Mechanism P.C.B. Ass’y, you need to short-circuit the laser diode shorting lands beforehand.

1.4. Software Upgrade

You can upgrade DVD Player using the software we provide as following step:

— Creating a software upgrade CD
— Use only a new CD-R/CD-RW(not an erased one).
— Give the CD a name of your choice(e.g. version and unit name).
— Burn the unpacked documents on the CD-R/CD-RW.
— The root directory(uppermost level) of the software upgrade CD

Attention: If a failure should occur during the software upgrade (e.g. a mains failure), it may happen that the units function and a restart of the upgrade function are no longer possible. If this should be the case, you must replace the intergraded FLASH ICs with preprogrammed ICs (see corresponding spare parts list).

─ Insert the upgrade CD (see corresponding spare parts list) and observe the hints on the display and on the screen of the TV set.
─ Carry out an initialization of the set.

Displaying the Software Version Number

— Press one after the other the “STOP” and “EJECT” buttons on the unit.
— Press the“OSD” with the remote control.
— Using the cursor buttons on the remote control, select the software version “MICRO Version” or “CUSTOMER VERSION” .The respective software version number then is displayed

2. Circuit Diagram and Component Layout

2.1. MPEG IC Block Diagrams

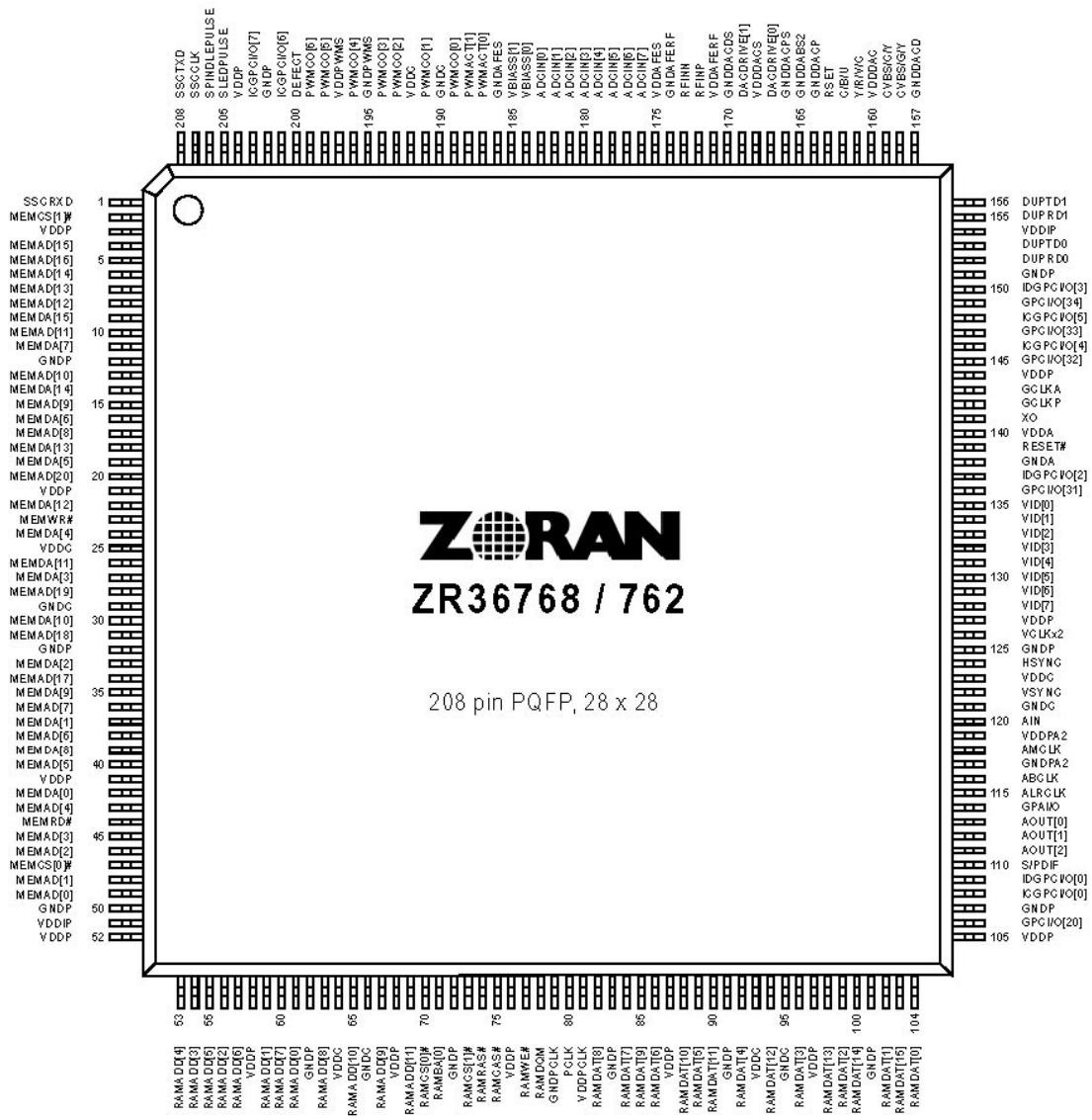


Fig. 2-1 ZR36768/762

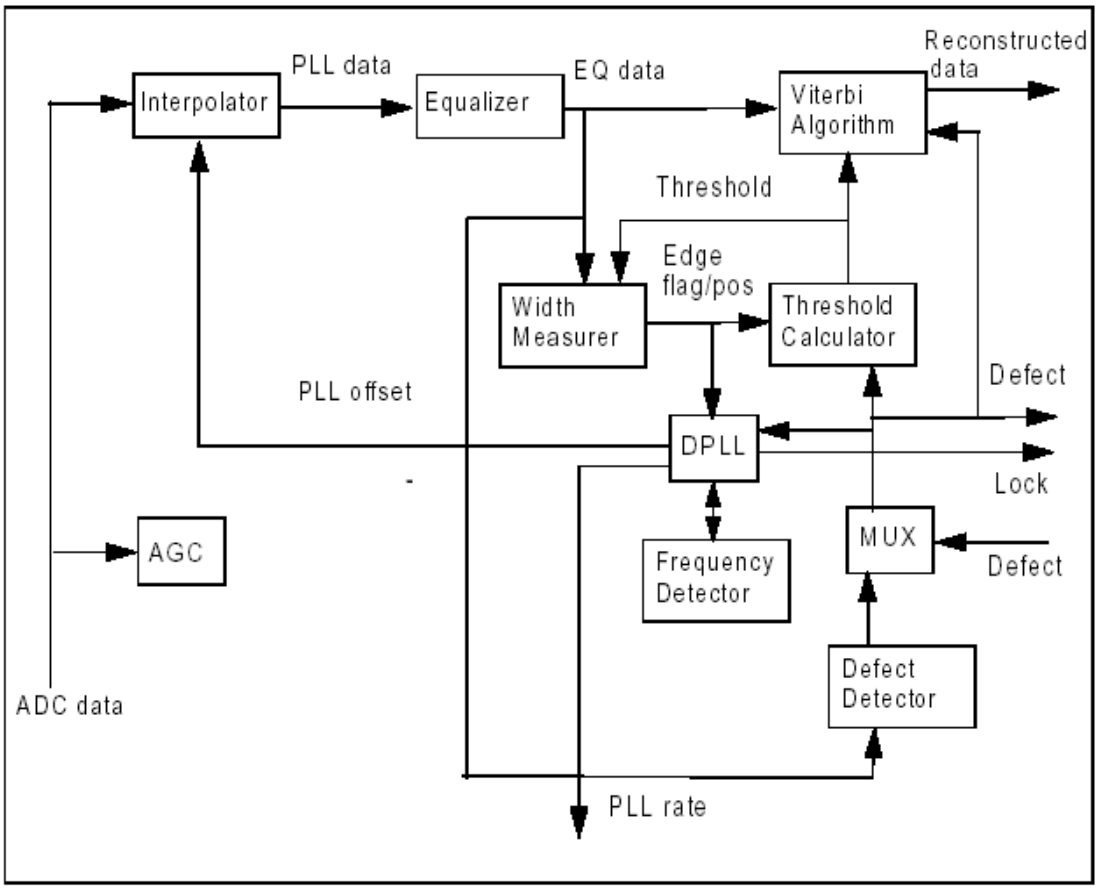


Fig. 2-2 DRC block diagram

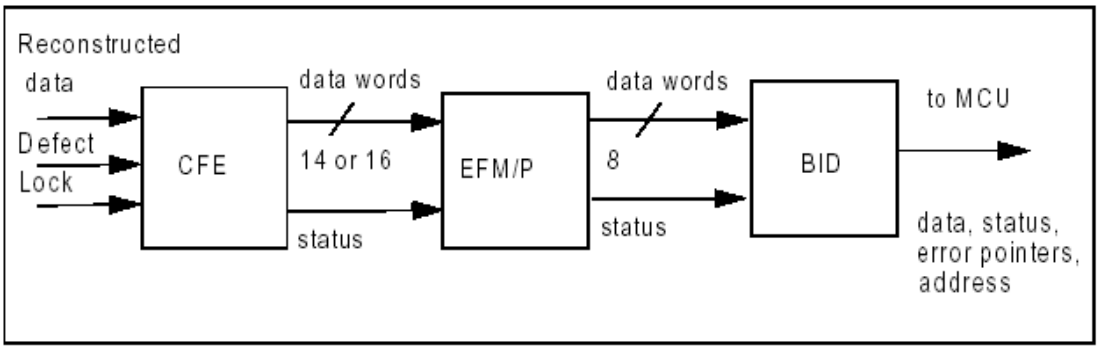


Fig.2-3 CSTP block diagram

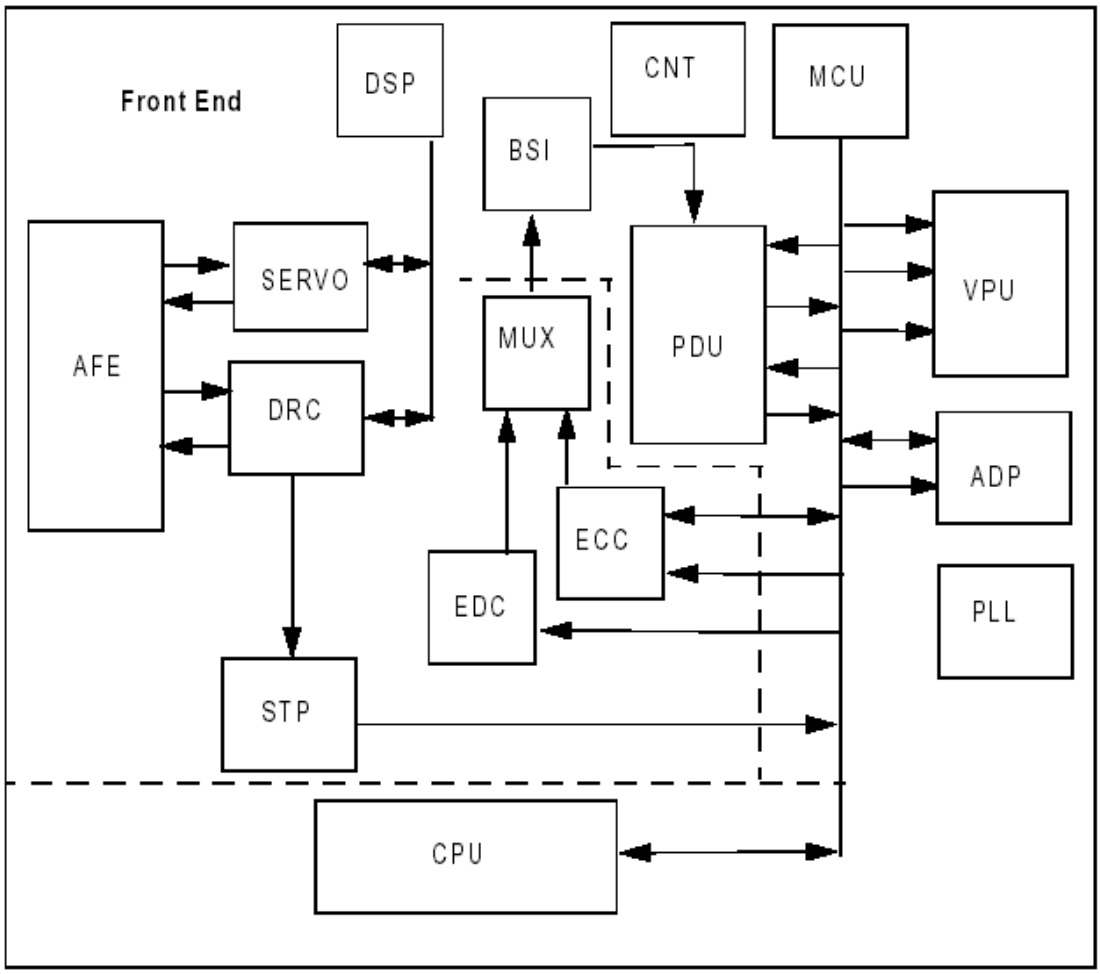


Fig.2-4 Vaddis ZR36768/762 block diagram

Table 1. Vaddis 6E Pin Description

Pin	Name	Direction	Status During/After RESET
	CPU Interface (15 pins)		
153	***DUPTD0*** ***GPCI/O[36]***	O I/O	During RESET: Output (high) After RESET: Input (r.t.)
	DUPTD0: First debug UART data output. GPCI/O[36]: General purpose input/output, monitored/controlled by CPU or DSP SW.		
152	***DUPRD0*** ***GPCI/O[35]***	I I/O	During RESET: Input (p.u.) After RESET: Input (r.t.)
	DUPRD0: First debug UART data input. GPCI/O[35]: General purpose input/output, monitored/controlled by CPU or DSP SW.		
156	***DUPTD1*** ***GPCI/O[38]***	O I/O	During RESET: Input (p.u.) After RESET: Input (r.t.)
	DUPTD1: Second debug UART data output. GPCi/O[38]: General purpose input/output, monitored/controlled by CPU or DSP SW.		
155	***DUPRD1*** ***GPCI/O[37]***	I I/O	During RESET: Input (p.u.) After RESET: Input (r.t.)
	DUPRD1: Second debug UART data input. GPCI/O[37]: General purpose input/output, monitored/controlled by CPU or DSP SW.		
106	***GPCI/O[20]*** ***CPUNMI*** ***SDATA[0]*** ***PM[0]***	I/O I I O	During RESET: Input (p.d.) After RESET: Input (r.t.)
	GPCI/O[20]: General purpose input/output, monitored/controlled by CPU or DSP SW. CPUNMI: CPU non-maskable interrupt input. SDATA[0]: SERVO channel sample data input for analog front-end bypass. PM[0]: Probe mux data output.		

Table 1. Vaddis 6E Pin Description (Continued)

Pin	Name	Direction	Status During/After RESET
	CPU Interface (15 pins) - continued		
108	*ICGPCI/O[0]* *AOUT[3]* *SDATA[1]* *PM[1]*	I/O O I O	During RESET: Input (p.d.) After RESET: Input (r.t.)
	ICGPCI/O[0]: General purpose input/output, monitored/controlled by CPU or DSP SW. Can be used as a general purpose external interrupt to the CPU. AOUT[3]: Serial output of digital stereo audio. SDATA[1]: SERVO channel sample data input for analog front-end bypass. PM[1]: Probe mux data output.		
109	*IDGPCI/O[0]* *SDATA[2]* *PM[2]*	I/O I O	During RESET: Input (p.d.) After RESET: Input (r.t.)
	IDGPCI/O[0]: General purpose input/output, monitored/controlled by CPU or DSP SW. Can be used as a general purpose external interrupt to the DSP. SDATA[2]: SERVO channel sample data input for analog front-end bypass. PM[2]: Probe mux data output.		
149 147 145 136	*GPCI/O[34]* *GPCI/O[33]* *GPCI/O[32]* *GPCI/O[31]*	I/O I/O I/O I/O	During RESET: Input (p.d.) After RESET: Input (r.t.)
	General purpose inputs/outputs, monitored/controlled by CPU or DSP SW.		
148 146	*ICGPCI/O[5]* *ICGPCI/O[4]*	I/O I/O	During RESET: Input (p.d.) After RESET: Input (r.t.)
	General purpose input/outputs, monitored/controlled by CPU and DSP SW. Can be used as general purpose external interrupts to the CPU.		
150 137	*IDGPCI/O[3]* *IDGPCI/O[2]*	I/O I/O	During RESET: Input (p.d.) After RESET: Input (r.t.)
	General purpose input/outpust, monitored/controlled by CPU and DSP SW. Can be used as general purpose external interrupts to the DSP.		
	PLL Signals (4 pins)		
139	*RESET#*	ID	Input
	Reset input. After this signal is deasserted, the Vaddis 6E starts the initialization process.		
142	*GCLKP*	ID	Input
	27.000MHz clock or crystal input for main processing clock generation.		
141	*XO*	AO	Output
	Output to a crystal that is connected to *GCLKP*. If a crystal is not used at *GCLKP*, *XO* must be left unconnected.		
143	*GCLKA*	ID	Input
	27.000MHz clock input for audio master clock generation. Must be connected to *GCLKP* in normal operation.		
	Analog Video Port (5 pins)		
158	*CVBS/G/Y* *(DAC A)*	AO	
	When the Vaddis 6E outputs composite video, this signal is CVBS. When the Vaddis 6E outputs RGB, this signal is green. When the Vaddis 6E outputs YUV, this signal is Y.		

Table 1. Vaddis 6E Pin Description (Continued)

Pin	Name	Direction	Status During/After RESET
	Analog Video Port (5 pins) - continued		
161	*Y/R/V/C* *(DAC B)*	AO	
	When the Vaddis 6E outputs composite video, this signal is Y. When the Vaddis 6E outputs RGB, this signal is red. When the Vaddis 6E outputs YUV, this signal is V. When the Vaddis 6E outputs SCART, this signal is C.		
162	*C/B/U* *(DAC C)*	AO	
	When the Vaddis 6E outputs composite video, this signal is C. When the Vaddis 6E outputs RGB, this signal is blue. When the Vaddis 6E outputs YUV, this signal is U.		
159	*CVBS/C/Y* *(DAC D)*	AO	
	The output on this line can be either CVBS, C or Y. The selection is independent of the selection on the other three DAC's.		
163	*RSET*	AI	
	Resistive load for gain adjustment of the DAC's.		
	Digital Video Port, CPU, DSP and ADP Debug (11 pins)		
128	*VID[7]* *ICETMS* *DJTMS* *GPCI/O[26]* *DACTEST[7]*	O I I I/O I	During RESET: Input (p.d.) After RESET: Input (r.t.)
	VID[7]: Digital video luma/chroma output, multiplexed in time according to the CCIR656 standard. ICETMS: ADPdebug interface. DJTMS: DSP debug interface. GPCI/O[26]: General purpose input/output, monitored/controlled by CPU or DSP SW. DACTEST[7]: DAC's test input.		
129	*VID[6]* *ICETDI* *DJTDI* *ICGPCI/O[2]* *DACTEST[6]*	O I I I/O I	During RESET: Input (p.d.) After RESET: Input (r.t.)
	VID[6]: Digital video luma/chroma output, multiplexed in time according to the CCIR656 standard. ICETDI: ADP debug interface. DJTDI: DSP debug interface. ICGPCI/O[2]: General purpose input/output, monitored/controlled by CPU or DSP SW. Can be used as a general purpose external interrupt to the CPU. DACTEST[6]: DAC's test input.		
130	*VID[5]* *ICETDO* *DJTDO* *IDGPCI/O[1]* *DACTEST[5]*	O O O I/O I	During RESET: Input (p.d.) After RESET: Input (r.t.)
	VID[5]: Digital video luma/chroma output, multiplexed in time according to the CCIR656 standard. ICETDO: ADP debug interface. DJTDO: DSP debug interface. IDGPCI/O[1]: General purpose input/output, monitored/controlled by CPU or DSP SW. Can be used as a general purpose external interrupt to the DSP. DACTEST[5]: DAC's test input.		

Table 1. Vaddis 6E Pin Description (Continued)

Pin	Name	Direction	Status During/After RESET
	Digital Video Port, CPU, DSP and ADP Debug (11 pins) - continued		
131	*VID[4]* *ICETCK* *DJTCK* *GPCI/O[27]* *DACTEST[4]*	O I I I/O I	During RESET: Input (p.d.) After RESET: Input (r.t.)
	VID[4]: Digital video luma/chroma output, multiplexed in time according to the CCIR656 standard. ICETCK: ADPdebug interface. DJTCK: DSP debug interface. GPCI/O[27]: General purpose input/output, monitored/controlled by CPU or DSP SW. DACTEST[4]: DAC's test input.		
132	*VID[3]* *DJTMS* *GPCI/O[28]* *DACTEST[3]* *SERVOCLK*	O I I/O I O	During RESET: Input (p.d.) After RESET: Input (r.t.)
	VID[3]: Digital video luma/chroma output, multiplexed in time according to the CCIR656 standard. DJTMS: DSP debug interface. GPCI/O[28]: General purpose input/output, monitored/controlled by CPU or DSP SW. DACTEST[3]: DAC's test input. SERVOCLK: SERVO channel clock output for analog front-end bypass.		
133	*VID[2]* *DJTDI* *GPCI/O[29]* *DACTEST[2]* *SSEL[0]*	O I I/O I O	During RESET: Input (p.d.) After RESET: Input (r.t.)
	VID[2]: Digital video luma/chroma output, multiplexed in time according to the CCIR656 standard. DJTDI: DSP debug interface. GPCI/O[29]: General purpose input/output, monitored/controlled by CPU or DSP SW. DACTEST[2]: DAC's test input. SSEL[0]: SERVO channel select output for analog front-end bypass.		
134	*VID[1]* *DJTDO* *GPCI/O[30]* *DACTEST[1]* *SSEL[1]*	O O I/O I O	During RESET: Input (p.d.) After RESET: Input (r.t.)
	VID[1]: Digital video luma/chroma output, multiplexed in time according to the CCIR656 standard. DJTDO: DSP debug interface. GPCI/O[30]: General purpose input/output, monitored/controlled by CPU or DSP SW. DACTEST[1]: DAC's test input. SSEL[1]: SERVO channel select output for analog front-end bypass.		
135	*VID[0]* *DJTCK* *ICGPCI/O[3]* *DACTEST[0]* *SSEL[2]*	O I I/O I O	During RESET: Input (p.d.) After RESET: Input (r.t.)
	VID[0]: Digital video luma/chroma output, multiplexed in time according to the CCIR656 standard. DJTCK: DSP debug interface. ICGPCI/O[3]: General purpose input/output, monitored/controlled by CPU or DSP SW. Can be used as a general purpose external interrupt to the CPU. DACTEST[0]: DAC's test input. SSEL[2]: SERVO channel select output for analog front-end bypass.		

Table 1. Vaddis 6E Pin Description (Continued)

Pin	Name	Direction	Status During/After RESET
	Digital Video Port, CPU, DSP and ADP Debug (11 pins) - continued		
126	*VCLKx2* *COSYNC* *ICGPCI/O[1]* *CJTMS* *DACTEST[10]* *PM[11]*	O O I/O I I O	During RESET: Input (p.d.) After RESET: Input (r.t.)
	VCLKx2: Digital video clock output. 27.000MHz. COSYNC: Composite sync output. Active only when component analog output is selected. ICGPCI/O[1]: General purpose input/output, monitored/controlled by CPU or DSP SW. Can be used as a general purpose external interrupt to the CPU. CJTMS: CPU debug interface. DACTEST[10]: DAC's test input. PM[11]: Probe mux data output.		
124	*HSYNC#* *GPCI/O[25]* *CJTDO* *DACTEST[8]* *PM[10]*	O I/O O I O	During RESET: Output (low) After RESET: Output (low)
	HSYNC#: Digital video horizontal sync signal. GPCI/O[25]: General purpose input/output, monitored/controlled by CPU or DSP SW. CJTDO: CPU debug interface. DACTEST[8]: DAC's test input. PM[10]: Probe mux data output.		
122	*VSYNC#* *GPCI/O[24]* *CJTDI* *DACTEST[9]* *PM[9]*	O I/O I I O	During RESET: Input (p.d.) After RESET: Input (r.t.)
	VSYNC#: Digital video vertical sync signal. GPCI/O[24]: General purpose input/output, monitored/controlled by CPU or DSP SW. CJTDI: CPU debug interface. DACTEST[9]: DAC's test input. PM[9]: Probe mux data output.		
	Digital Audio Port and CPU Debug (9 pins)		
120	*AIN* *GPCI/O[23]* *CJTCK* *PM[8]*	I I/O I O	During RESET: Input (p.d.) After RESET: Input (r.t.)
	AIN: Serial input of digital stereo audio. GPCI/O[23]: General purpose input/output, monitored/controlled by CPU or DSP SW. CJTCK: CPU debug interface. PM[8]: Probe mux data output.		
118	*AMCLK*	I/O	During RESET: Input (p.d.) After RESET: Input (r.t.)
	Audio master clock input/output. 128, 192, 256 or 384 times the sampling frequency.		
110	*S/PDIF* *SDATA[3]* *PM[3]*	O I O	During RESET: Input (p.d.) After RESET: Output (low)
	S/PDIF: S/PDIF transmitter output for digital coded or reconstructed audio data. SDATA[3]: SERVO channel sample data input for analog front-end bypass. PM[3]: Probe mux data output.		

Table 1. Vaddis 6E Pin Description (Continued)

Pin	Name	Direction	Status During/After RESET
	Digital Audio Port and CPU Debug (9 pins) - continued		
111	*AOUT[2]* *GPCI/O[21]* *SDTATA[4]* *PM[4]*	O I/O I O	During RESET: Input (p.d.) After RESET: Output (low)
	AOUT[2]: Serial output of digital stereo audio. GPCI/O[21]: General purpose input/output, monitored/controlled by CPU or DSP SW. SDATA[4]: SERVO channel sample data input for analog front-end bypass. PM[4]: Probe mux data output.		
112	*AOUT[1]* *GPCI/O[22]* *SDTATA[5]* *PM[5]*	O I/O I O	During RESET: Input (p.d.) After RESET: Output (low)
	AOUT[1]: Serial output of digital stereo audio. GPCI/O[22]: General purpose input/output, monitored/controlled by CPU or DSP SW. SDATA[5]: SERVO channel sample data input for analog front-end bypass. PM[5]: Probe mux data output.		
113	*AOUT[0]* *SDATA[6]* *PM[6]*	O I O	During RESET: Input (p.d.) After RESET: Output (low)
	AOUT[0]: Serial output of digital stereo audio. SDATA[6]: SERVO channel sample data input for analog front-end bypass. PM[6]: Probe mux data output.		
115	*ALRCLK*	O	During RESET: Input (p.d.) After RESET: Output (low)
	Digital audio left/right select output for the audio port. Square wave, at the sampling frequency.		
116	*ABCLK*	O	During RESET: Input (p.d.) After RESET: Output (low)
	Digital audio bit-clock output. Data on *AOUT* and *AIN* is output or latched, respectively, with the edge of this clock.		
114	*GPAI/O* *AOUT[3]* *SDATA[7]* *PM[7]*	I/O O I O	During RESET: Input (p.d.) After RESET: Input (r.t.)
	GPAI/O: General purpose input/output, monitored/controlled by the ADP SW. AOUT[3]: Serial output of digital stereo audio. SDATA[7]: SERVO channel sample data input for analog front-end bypass. PM[7]: Probe mux data output.		
	Loader Interface, RF Amplifier Interface, AV Bitstream Interface (28 pins)		
185 184	*VBIASS[1]* *VBIASS[0]*	AI AI	
	Servo analog signal reference voltage inputs.		
169 167	*DACDRIVE[1]* *DACDRIVE[0]*	AO AO	
	Drive DAC's output signals.		

Table 1. Vaddis 6E Pin Description (Continued)

Pin	Name	Direction	Status During/After RESET
Loader Interface, RF Amplifier Interface, AV Bitstream Interface (28 pins) - continued			
187	*PWMACT[0]* *GPCI/O[39]* *DVDDAT[0]* *NRZDATA*	O I/O I I	During RESET: Input (p.d.) After RESET: Input (r.t.)
	PWMACT[0]: PWM0 output signal. GPCI/O[39]: General purpose input/output, monitored/controlled by CPU or DSP SW. DVDDAT[0]: AV data input line for front-end bypass. NRZDATA: NRZ data input for analog front-end and data read channel bypass.		
188	*PWMACT[1]* *GPCI/O[40]* *DVDDAT[1]* *NRZCLK*	O I/O I I	During RESET: Input (p.d.) After RESET: Input (r.t.)
	PWMACT[1]: PWM1 output signal. GPCI/O[40]: General purpose input/output, monitored/controlled by CPU or DSP SW. DVDDAT[1]: AV data input line for front-end bypass. NRZCLK: NRZ clock input for analog front-end and data read channel bypass.		
205	*SLEDPULSE* *IDGPCI/O[6]* *DVDSOS*	I I/O I	During RESET: Input (p.d.) After RESET: Input (r.t.)
	SLEDPULSE: Sled optical encoder input. IDGPCI/O[6]: General purpose input/output, monitored/controlled by CPU or DSP SW. Can be used as a general purpose external interrupt to the DSP. DVDSOS: AV start of sector indication input for front-end bypass.		
206	*SPINDLEPULSE* *IDGPCI/O[7]*	I I/O	During RESET: Input (p.d.) After RESET: Input (r.t.)
	SPINDLEPULSE: Spindle optical encoder input. IDGPCI/O[7]: : General purpose input/output, monitored/controlled by CPU or DSP SW. Can be used as a general purpose external interrupt to the DSP.		
172	*RFINP*	AI	
	RF positive input signal (differential input) or RF input signal (single ended).		
173	*RFINN*	AI	
	RF negative input signal (differential input) or RF reference input signal.		
176	*ADCIN[7]* *AFETESTN*	AI AI/O	
	ADCIN[7]: SERVO ADC input signal from RF amplifier. AFETESTN: Analog front-end test differential signal (negative), input or output.		
177	*ADCIN[6]* *AFETESTP*	AI AI/O	
	ADCIN[6]: SERVO ADC input signal from RF amplifier. AFETESTP: Analog front-end test differential signal (positive), input or output.		
178 179 180 181 182 183	*ADCIN[5]* *ADCIN[4]* *ADCIN[3]* *ADCIN[2]* *ADCIN[1]* *ADCIN[0]*	AI AI AI AI AI AI	
	SERVO ADC input signals from RF amplifier.		

Table 1. Vaddis 6E Pin Description (Continued)

Pin	Name	Direction	Status During/After RESET
Loader Interface, RF Amplifier Interface, AV Bitstream Interface (28 pins) - continued			
189	*PWMCO[0]* *GPCI/O[41]* *DVDDAT[2]* *NRZLOCK*	O I/O I I	During RESET: Input (p.d.) After RESET: Input (r.t.)
	PWMCO[0]: PWM2 output signal. GPCI/O[41]: General purpose input/output, monitored/controlled by CPU or DSP SW. DVDDAT[2]: AV data input for front-end bypass. NRZLOCK: NRZ lock input for analog front-end and data read channel bypass.		
191	*PWMCO[1]* *GPCI/O[42]* *DVDDAT[3]* *NRZDFCT*	O I/O I I	During RESET: Input (p.d.) After RESET: Input (r.t.)
	PWMCO[1]: PWM3 output signal. GPCI/O[42]: General purpose input/output, monitored/controlled by CPU or DSP SW. DVDDAT[3]: AV data input for front-end bypass. NRZDFCT: NRZ defect input for analog front-end and data read channel bypass.		
193	*PWMCO[2]* *GPCI/O[43]* *DVDDAT[4]* *RFDAT[0]*	O I/O I I	During RESET: Input (p.d.) After RESET: Input (r.t.)
	PWMCO[2]: PWM4 output signal. GPCI/O[43]: General purpose input/output, monitored/controlled by CPU or DSP SW. DVDDAT[4]: AV data input for front-end bypass. RFDAT[0]: RF channel sample data input for analog front-end bypass.		
194	*PWMCO[3]* *GPCI/O[44]* *DVDDAT[5]* *RFDAT[1]*	O I/O I I	During RESET: Input (p.d.) After RESET: Input (r.t.)
	PWMCO[3]: PWM5 output signal. GPCI/O[44]: General purpose input/output, monitored/controlled by CPU or DSP SW. DVDDAT[5]: AV data input for front-end bypass. RFDAT[1]: RF channel sample data input for analog front-end bypass.		
196	*PWMCO[4]* *GPCI/O[45]* *DVDDAT[6]* *RFDAT[2]*	O I/O I I	During RESET: Input (p.d.) After RESET: Input (r.t.)
	PWMCO[4]: PWM6 output signal. GPCI/O[45]: General purpose input/output, monitored/controlled by CPU or DSP SW. DVDDAT[6]: AV data input for front-end bypass. RFDAT[2]: RF channel sample data input for analog front-end bypass.		
198	*PWMCO[5]* *GPCI/O[46]* *DVDDAT[7]* *RFDAT[3]*	O I/O I I	During RESET: Input (p.d.) After RESET: Input (r.t.)
	PWMCO[5]: PWM7 output signal. GPCI/O[46]: General purpose input/output, monitored/controlled by CPU or DSP SW. DVDDAT[7]: AV data input for front-end bypass. RFDAT[3]: RF channel sample data input for analog front-end bypass.		

Table 1. Vaddis 6E Pin Description (Continued)

Pin	Name	Direction	Status During/After RESET
Loader Interface, RF Amplifier Interface, AV Bitstream Interface (28 pins) - continued			
199	***PWMCO[6]*** ***IDGPCI/O[4]*** ***DVDREQ*** ***RFDAT[4]***	O I/O O I	During RESET: Input (p.d.) After RESET: Input (r.t.)
	PWMCO[6]: PWM8 output signal. IDGPCI/O[4]: General purpose input/output, monitored/controlled by CPU or DSP SW. Can be used as a general purpose external interrupt to the DSP. DVDREQ: AV data request output for front-end bypass. RFDAT[4]: RF channel sample data input for analog front-end bypass.		
203	***ICGPCI/O[7]*** ***DVDERR*** ***RFCLK*** ***PM[12]***	I/O I O O	During RESET: Input (p.d.) After RESET: Input (r.t.)
	ICGPCI/O[7]: General purpose input/output, monitored/controlled by CPU or DSP SW. Can be used as a general purpose external interrupt to the CPU. DVDERR: AV error input for front-end bypass. RFCLK: RF channel sampling clock output for analog front-end bypass. PM[12]: Probe mux data output.		
200	***DEFECT*** ***IDGPCI/O[5]*** ***DVDSTRB*** ***RFDAT[5]***	I/O I/O O I	During RESET: Input (p.d.) After RESET: Input (r.t.)
	DEFECT: Disc defect input or output signal. IDGPCI/O[5]: General purpose input/output, monitored/controlled by CPU or DSP SW. Can be used as a general purpose external interrupt to the DSP. DVDSTRB: AV data bit strobe (clock) input for front-end bypass. RFDAT[5]: RF channel sample data inputs for analog front-end bypass.		
201	***ICGPCI/O[6]*** ***DVDVALID*** ***PM[16]***	I/O I O	During RESET: Input (p.d.) After RESET: Input (r.t.)
	ICGPCI/O[6]: General purpose input/output, monitored/controlled by CPU or DSP SW. Can be used as a general purpose external interrupt to the CPU. DVDVALID: AV data valid input for front-end bypass. RFCLK: RF channel sampling clock output for analog front-end bypass. PM[16]: Probe mux data output.		

Table 1. Vaddis 6E Pin Description (Continued)

Pin	Name	Direction	Status During/After RESET
	SDRAM Interface (36 pins)		
103 100 98 94 90 88 85 82 84 86 89 92 96 99 102 104	*RAMDAT[15]* *RAMDAT[14]* *RAMDAT[13]* *RAMDAT[12]* *RAMDAT[11]* *RAMDAT[10]* *RAMDAT[9]* *RAMAT[8]* *RAMDAT[7]* *RAMDAT[6]* *RAMDAT[5]* *RAMDAT[4]* *RAMAT[3]* *RAMDAT[2]* *RAMDAT[1]* *RAMDAT[0]*	I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O	During RESET: Input (r.t.) After RESET: Input (r.t.)
	SDRAM bi-directional data bus.		
69 65 67 63 60 57 55 53 54 56 59 61	*RAMADD[11]* *RAMADD[10]* *RAMADD[9]* *RAMADD[8]* *RAMADD[7]* *RAMADD[6]* *RAMADD[5]* *RAMADD[4]* *RAMADD[3]* *RAMADD[2]* *RAMADD[1]* *RAMADD[0]*	O O O O O O O O O O O O	During RESET: Output (low) After RESET: Output (low)
	SDRAM address bus output.		
74	*RAMRAS#*	O	During RESET: Output (high) After RESET: Output (high)
	SDRAM row select.		
75	*RAMCAS#*	O	During RESET: Output (high) After RESET: Output (high)
	SDRAM column select.		
80	*PCLK*	O	During RESET: Output After RESET: Output
	SDRAM clock output (same as internal processing clock).		
78	*RAMDQM*	O	During RESET: Output (high) After RESET: Output (high)
	SDRAM data masking.		
71	*RAMBA[0]*	O	During RESET: Output (high) After RESET: Output (low)
	SDRAM bank select.		
70	*RAMCS[0]#* *RAMBA[1]*	O O	During RESET: Output (high) After RESET: Output (high)
	RAMCS[0]#: SDRAM chip select. RAMBA[1]: SDRAM bank select.		
73	*RAMCS[1]#*	O	During RESET: Output (high) After RESET: Output (high)
	SDRAM chip select.		

Table 1. Vaddis 6E Pin Description (Continued)

Pin	Name	Direction	Status During/After RESET
	SDRAM Interface (36 pins) - continued		
77	*RAMWE#*	O	During RESET: Output (high) After RESET: Output (high)
	SDRAM write enable.		
	SSC Interface (3 pins)		
208	*SSCTXD* *GPCI/O[16]* *PM[14]*	O I/O O	During RESET: Input (p.d.) After RESET: Input (r.t.)
	SSCTXD: SSC data output signal. GPCI/O[16]: General purpose input/output, monitored/controlled by the CPU or DSP SW. PM[14]: Probe mux data output.		
1	*SSCRXD* *GPCI/O[17]* *PM[15]*	I I/O O	During RESET: Input (p.d.) After RESET: Input (r.t.)
	SSCRXD: SSC data input. GPCI/O[17]: General purpose input/output, monitored/controlled by CPU or DSP SW. PM[15]: Probe mux data output.		
207	*SSCCLK* *GPCI/O[47]* *PM[13]*	I/O I/O O	During RESET: Input (p.d.) After RESET: Input (r.t.)
	SSCLK: SSC clock signal, input or output. GPCI/O[47]: General purpose input/output, monitored/controlled by CPU or DSP SW. PM[13]: Probe mux data output.		
	PNVM/SRAM Interface (41 pins)		
9 14 18 22 26 30 35 39 11 16 19 24 27 33 37 42	*MEMDA[15]* *MEMDA[14]* *MEMDA[13]* *MEMDA[12]* *MEMDA[11]* *MEMDA[10]* *MEMDA[9]* *MEMDA[8]* *MEMDA[7]* *MEMDA[6]* *MEMDA[5]* *MEMDA[4]* *MEMDA[3]* *MEMDA[2]* *MEMDA[1]* *MEMDA[0]*	I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O	During RESET: Input (p.d.) After RESET: Input (r.t.)
	PNVM/SRAM bi-directional data bus.		
20	*MEMAD[20]* *MEMCS[2]#* *GPCI/O[19]*	O O I/O	During RESET: Input (p.u.) After RESET: Input (r.t.)
	MEMAD[20]: PNVM/SRAM address bus. MEMCS[2]#: PNVM/SRAM chip select. GPCI/O[19]: General purpose input/output, monitored/controlled by CPU or DSP SW.		
28	*MEMAD[19]* *PLLSEL*	O I	During RESET: Input (p.u.) After RESET: Output (high)
	MEMAD[19]: PNVM/SRAM address bus. PLLSEL: PLL frequency selection - 108MHz (low) or 135MHz (high), sampled during RESET.		

Table 1. Vaddis 6E Pin Description (Continued)

Pin	Name	Direction	Status During/After RESET
	PNVM/SRAM Interface (41 pins) - continued		
31 34 5 4 6	*MEMAD[18]* *MEMAD[17]* *MEMAD[16]* *MEMAD[15]* *MEMAD[14]*	O O O O O	During RESET: Output (low) After RESET: Output (low)
	PNVM/SRAM address bus.		
7	*MEMAD[13]* *AFETESTEN*	O I	During RESET: Input (p.d.) After RESET: Output (low)
	MEMAD[13]: PNVM/SRAM address bus. AFETESTEN: Analog front-end test mode enable input. Level sampled during RESET. In normal operation, this pin must be low during RESET.		
8	*MEMAD[12]* *PLLCFGA*	O I	During RESET: Input (p.d.) After RESET: Output (low)
	MEMAD[12]: PNVM/SRAM address bus. PLLCFGA: Audio PLL configuration input. Level sampled during RESET. In normal operation, this pin must be low during RESET.		
10	*MEMAD[11]* *PLLCFGP*	O I	During RESET: Input (p.d.) After RESET: Output (low)
	MEMAD[11]: PNVM/SRAM address bus. PLLCFGP: Process PLL configuration input. Level sampled during RESET. In normal operation, this pin must be low during RESET.		
13	*MEMAD[10]* *TESTMODE*	O I	During RESET: Input (p.d.) After RESET: Output (low)
	MEMAD[10]: PNVM/SRAM address bus. TESTMODE: Operational mode selection. Level sampled during RESET. In normal operation, this pin must be low during RESET.		
15 17 36 38 40 43 45 46	*MEMAD[9]* *MEMAD[8]* *MEMAD[7]* *MEMAD[6]* *MEMAD[5]* *MEMAD[4]* *MEMAD[3]* *MEMAD[2]*	O O O O O O O O	During RESET: Output (low) After RESET: Output (low)
	PNVM/SRAM address bus.		
48	*MEMAD[1]* *BOOTSEL[2]*	O I	During RESET: Input (p.d.) After RESET: Output (low)
	MEMAD[1]: PNVM/SRAM address bus. BOOTSEL[2]: CPU software boot (and execute) and execute source selection. See BOOTSEL[1] below.		
49	*MEMAD[0]* *BOOTSEL[1]*	O I	During RESET: Input (p.d.) After RESET: Output (low)
	MEMAD[0]: PNVM/SRAM address bus. BOOTSEL[1]: CPU software boot (and execute) and execute source selection: BOOTSEL[2:1] = 11b: Production testing. BOOTSEL[2:1] = 10b: Flash + SRAM (for debug/monitoring). BOOTSEL[2:1] = 01b: First debug UART. BOOTSEL[2:1] = 00b: Flash.		
23	*MEMWR#*	O	During RESET: Output (high) After RESET: Output (high)
	PNVM/SRAM write enable.		
44	*MEMRD#*	O	During RESET: Output (high) After RESET: Output (high)
	PNVM/SRAM read enable.		

Table 1. Vaddis 6E Pin Description (Continued)

Pin	Name	Direction	Status During/After RESET
	PNVM/SRAM Interface (41 pins) - continued		
47	*MEMCS[0]#*	O	During RESET: Output (high) After RESET: Output (high)
	PNVM/SRAM chip select.		
2	*MEMCS[1]#* *GPCI/O[18]*	O I/O	During RESET: Input (p.u.) After RESET: Input (r.t.)
	MEMCS[1]#: PNVM/SRAM chip select. GPCI/O[18]: General purpose input/output, monitored/controlled by CPU or DSP SW.		
	Power Signals (56 pins)		
*	*GNDP*		(* pins 12, 32, 50, 62, 72, 83, 91, 101, 107, 125, 151, 202)
	Digital periphery ground of 3.3V supply (12 pins).		
*	*VDDP*		(* pins 3, 21, 41, 52, 58, 68, 76, 87, 97, 105, 127, 144, 204)
	3.3V digital periphery power supply (13 pins).		
*	*VDDIP*		(* pins 51, 154)
	3.3V periphery reference voltage (2 pins).		
117	*GNDPA2*		
	Digital ground of filtered 3.3V supply for *AMCLK*.		
119	*VDDPA2*		
	3.3V filtered digital power supply for *AMCLK*.		
79	*GNDPCLK*		
	Digital ground of filtered 3.3V supply for *PCLK*.		
81	*VDDPCLK*		
	3.3V filtered digital power supply for *PCLK*.		
*	*GNDC*		(* pins 29, 66, 95, 121, 190)
	Digital core ground of 1.8V supply (5 pins).		
*	*VDDC*		(* pins 25, 64, 93, 123, 192)
	1.8V digital core power supply (5 pins).		
138	*GNDA*		
	Ground plane of internal PLL circuit.		
140	*VDDA*		
	1.8V power supply for internal PLL circuit.		
160	*VDDDAC*		
	3.3V analog power supply for the DAC's.		
164 157	*GNDDACP* *GNDDACD*		
	Grounds for the DAC's 3.3V analog power supply.		
165	*GNDDABS2*		
	Common ground for the video and SERVO DAC's		
166 170	*GNDDACPS* *GNDDACDS*		
	Grounds for the SERVO DAC 3.3V analog power supply.		
174	*GNDAFERF*		
	Analog RF ground of 3.3V supply.		
171	*VDDAFERF*		
	3.3V analog RF power supply.		
186	*GNDAFES*		
	Analog SERVO ground of 3.3V supply.		

Table 1. Vaddis 6E Pin Description (Continued)

Pin	Name	Direction	Status During/After RESET
Power Signals (56 pins) - continued			
175	*VDDAFES*		
	3.3V analog SERVO power supply.		
168	*VDDDACS*		
	3.3V SERVO DAC's power supply.		
195	*GNDPWMS*		
	SERVO PWM's ground of 3.3V supply.		
197	*VDDPWMS*		
	3.3V SERVO PWM power supply.		

2.2.Power supply Circuit Diagram and Component Layout

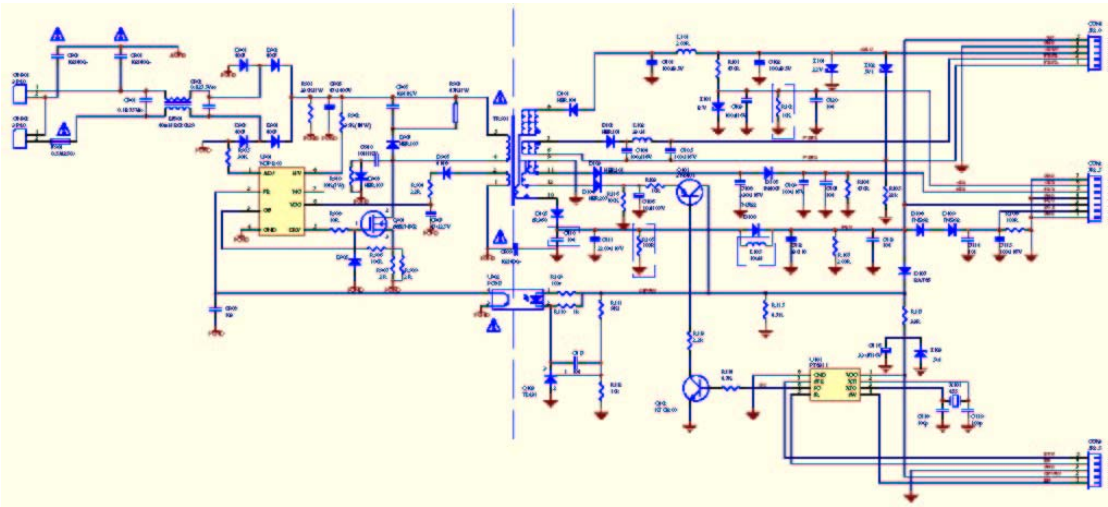


Fig 2-5 Power Supply Circuit Diagram

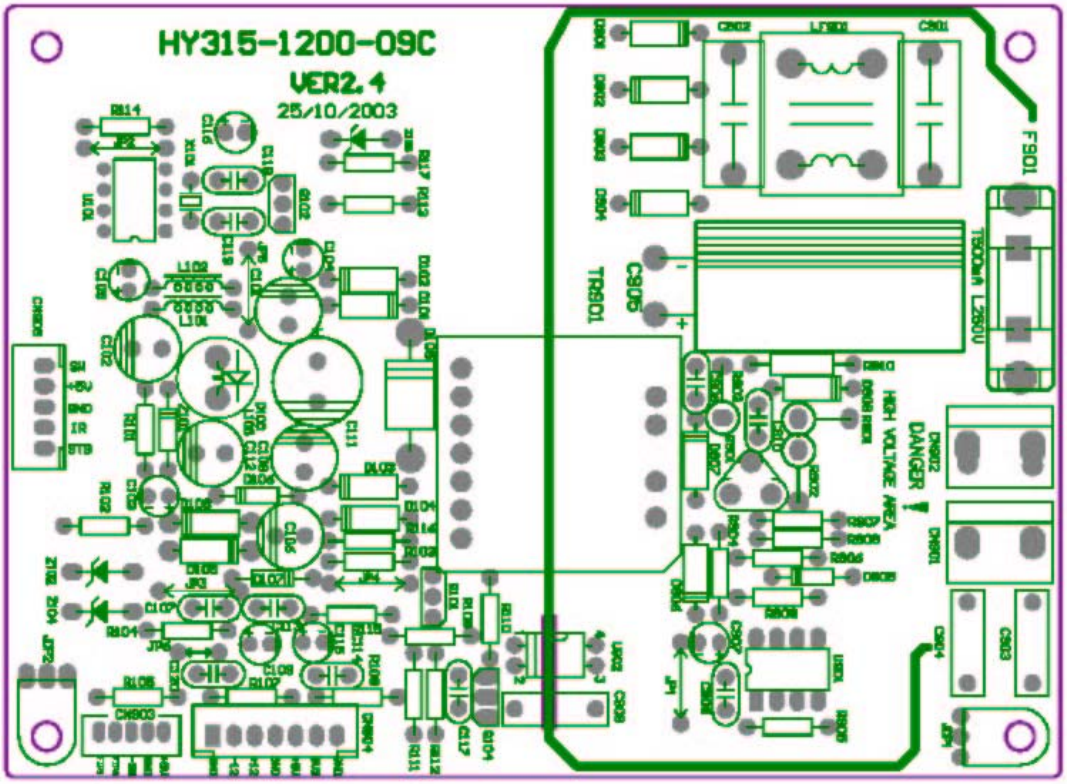


Fig 2-6 Power Supply Assembly Drawing

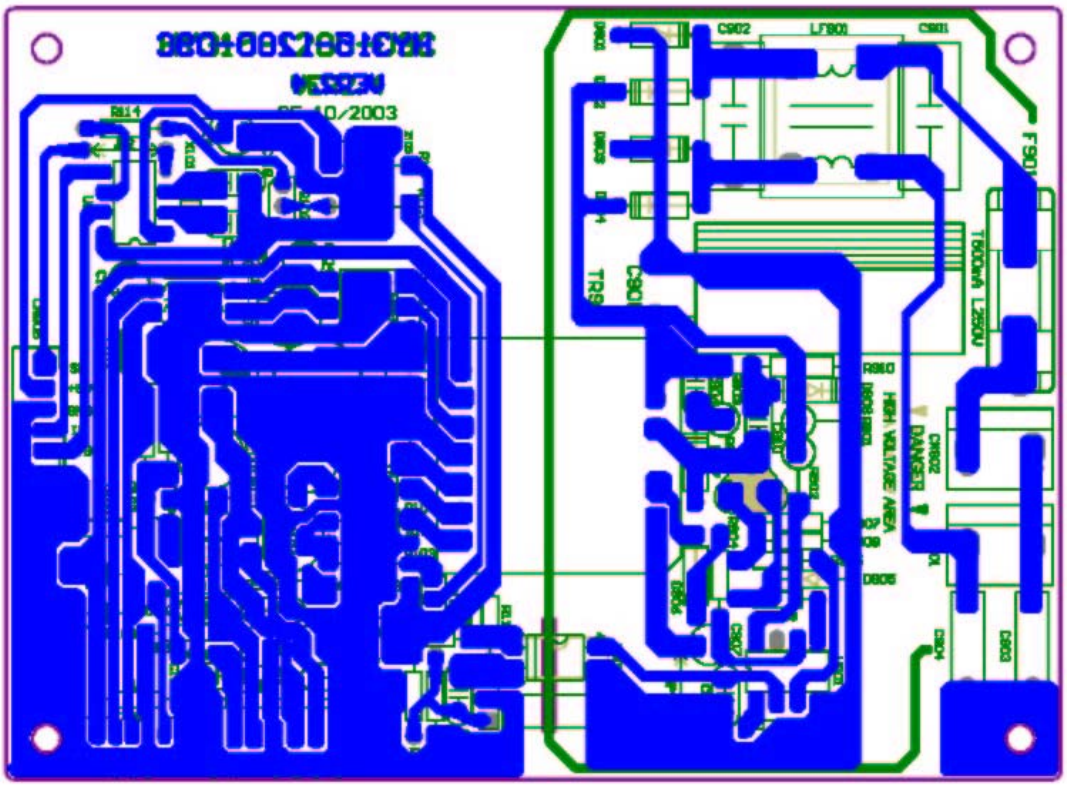


Fig 2-7 Power Supply Composite

2.3. MPEG Circuit Diagram and Component Layout

2.3.1. MPEG Circuit Diagram

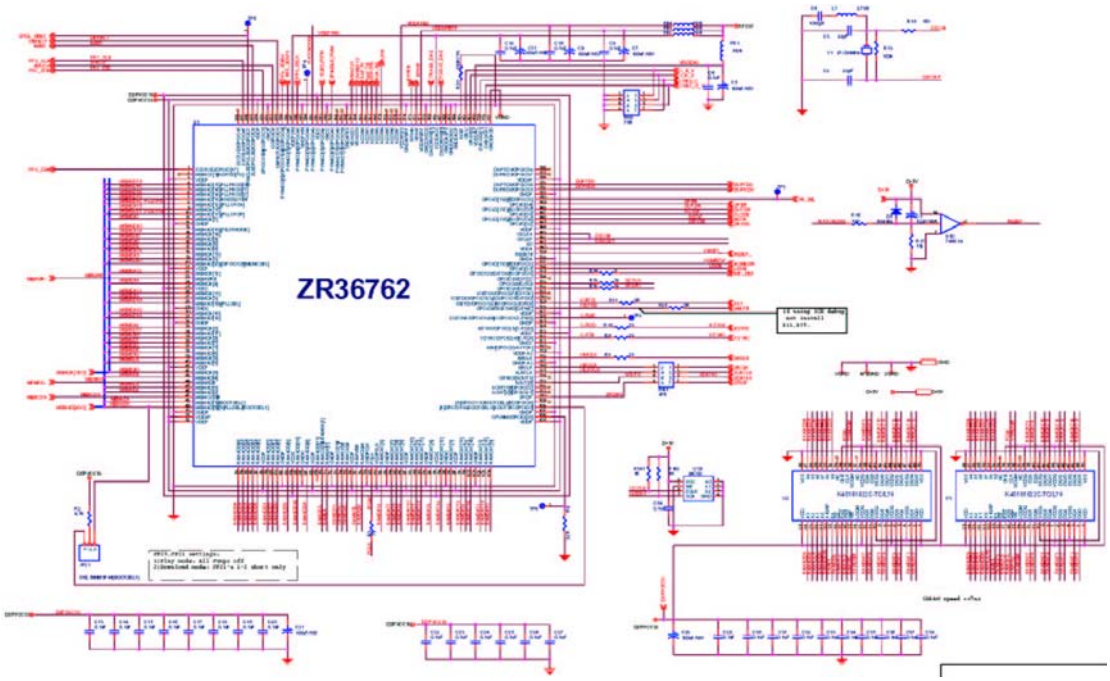


Fig 2-8 ZR36762/ZR36768&SDRAM

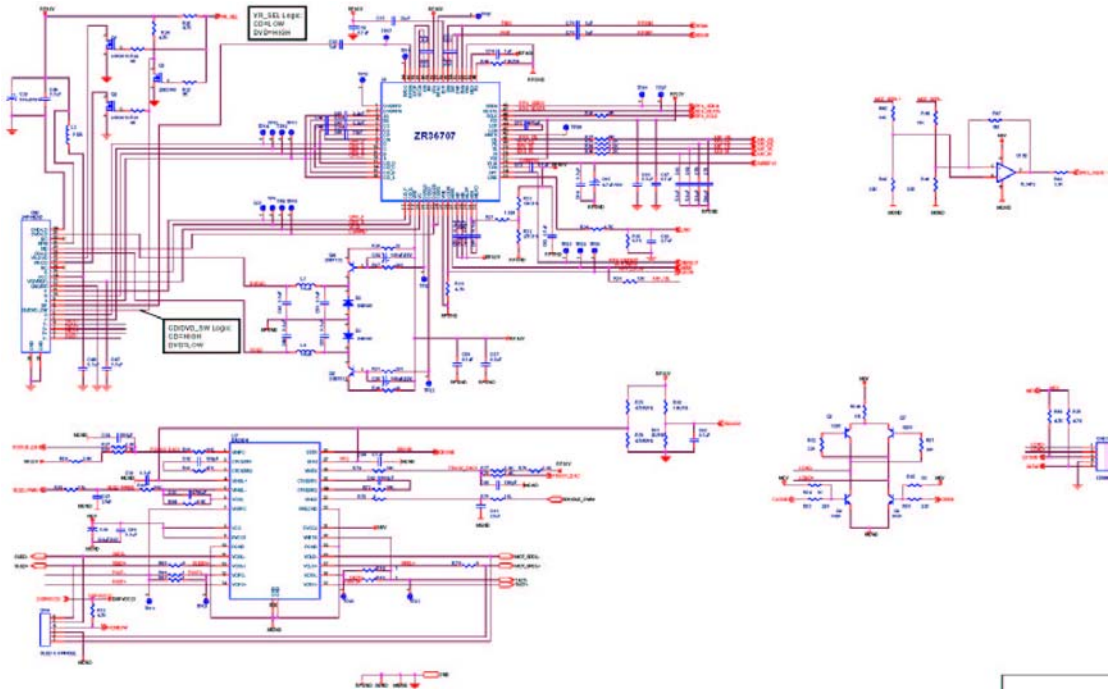


Fig2-9 RF AMPLIFIER&DRIVER

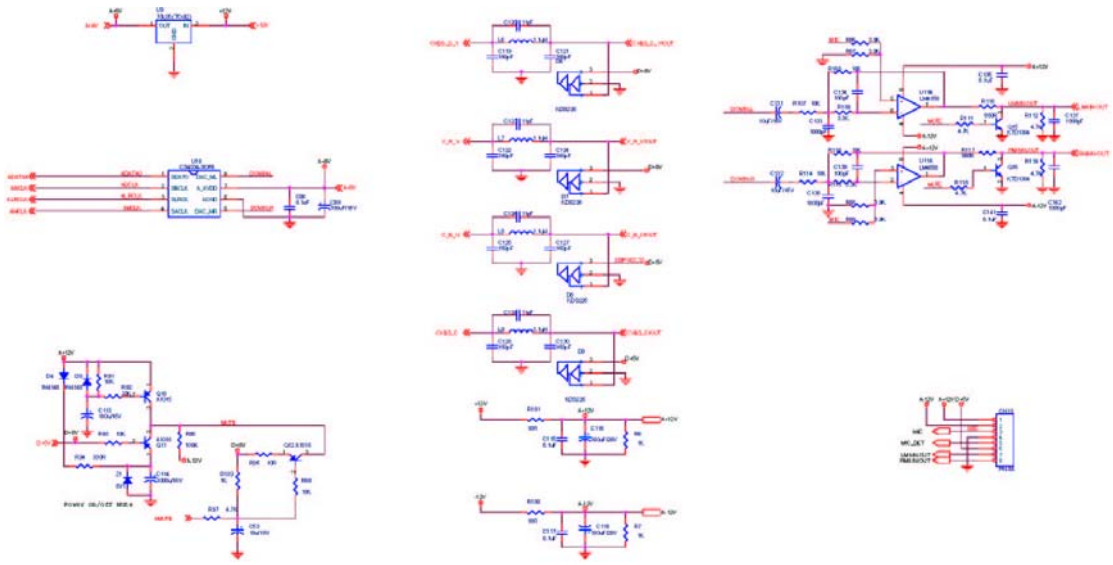


Fig 2-10 AUDIO&VIDEO FILTER

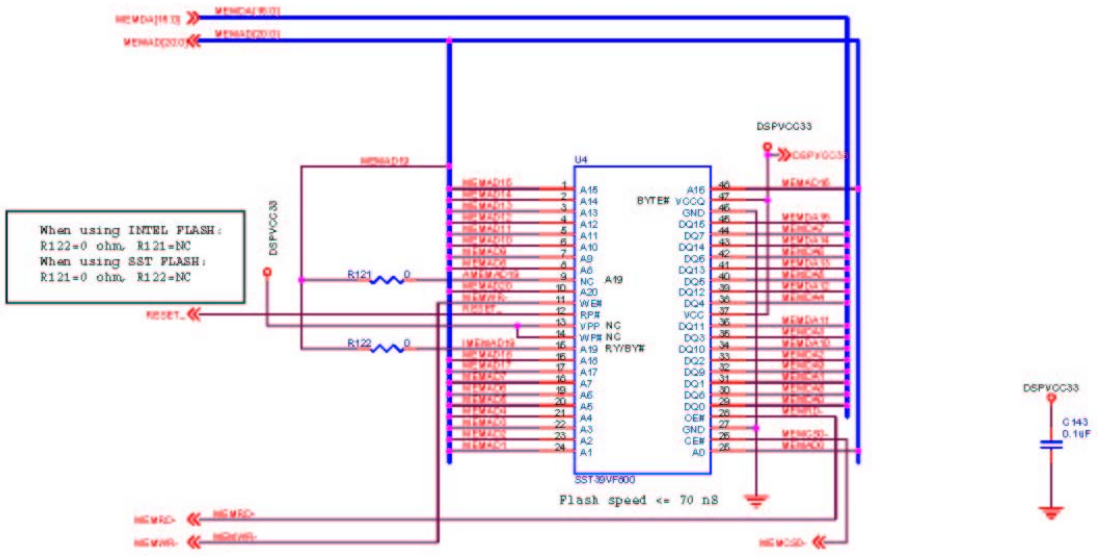


Fig 2-11 MEMORY

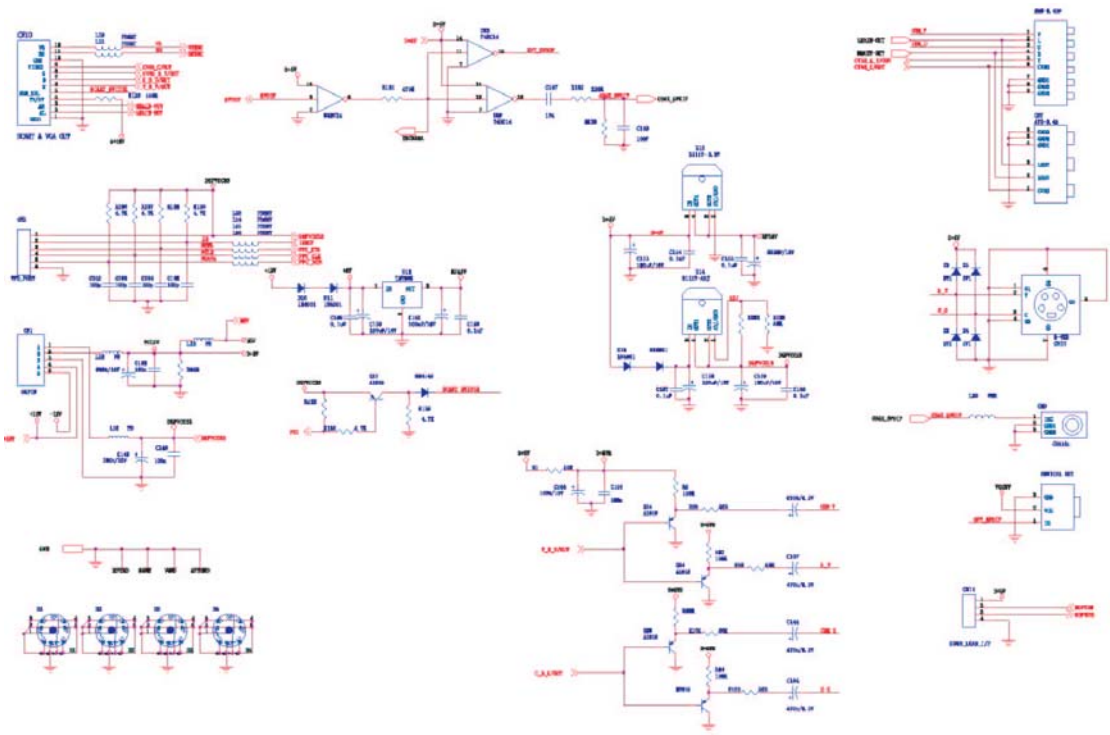
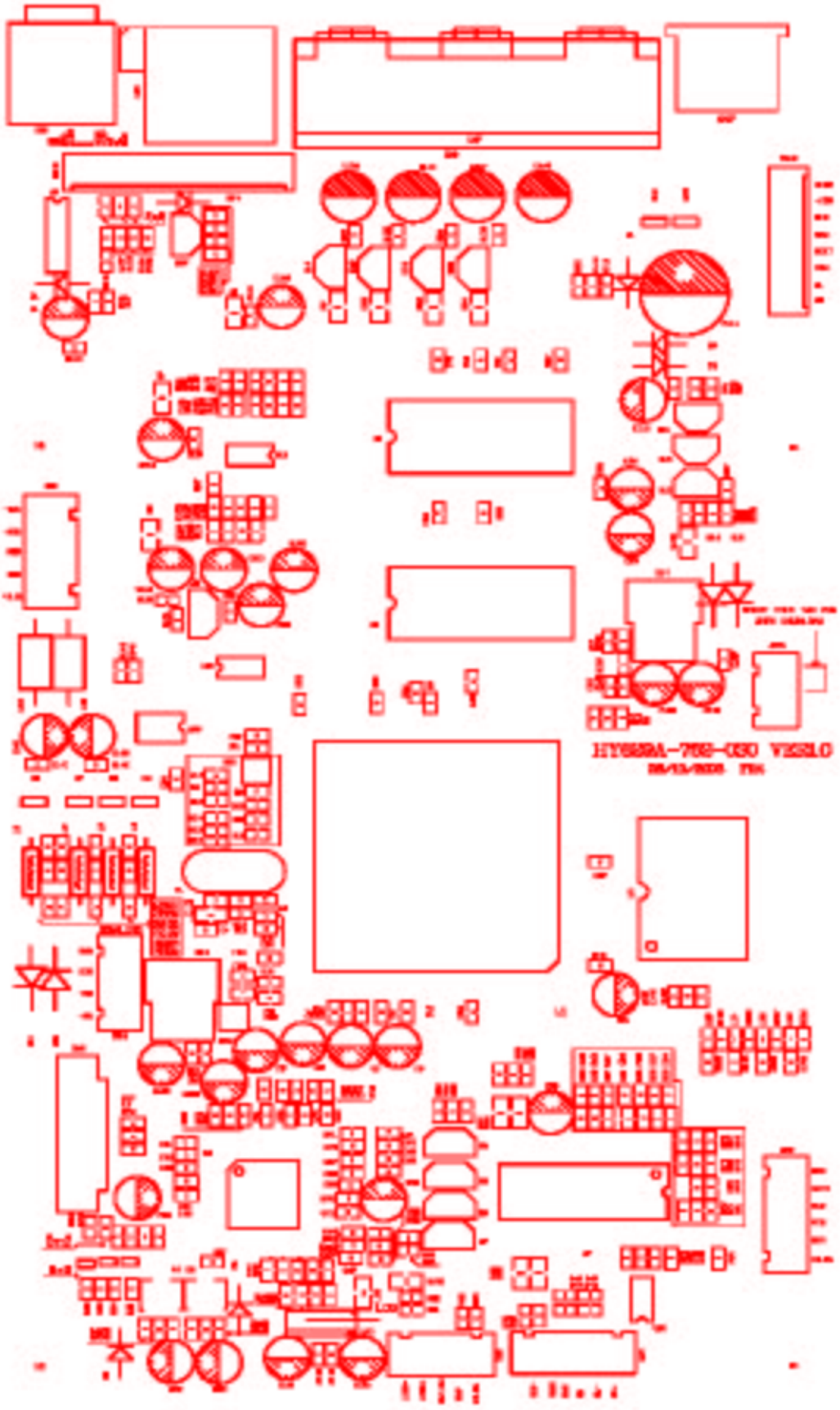


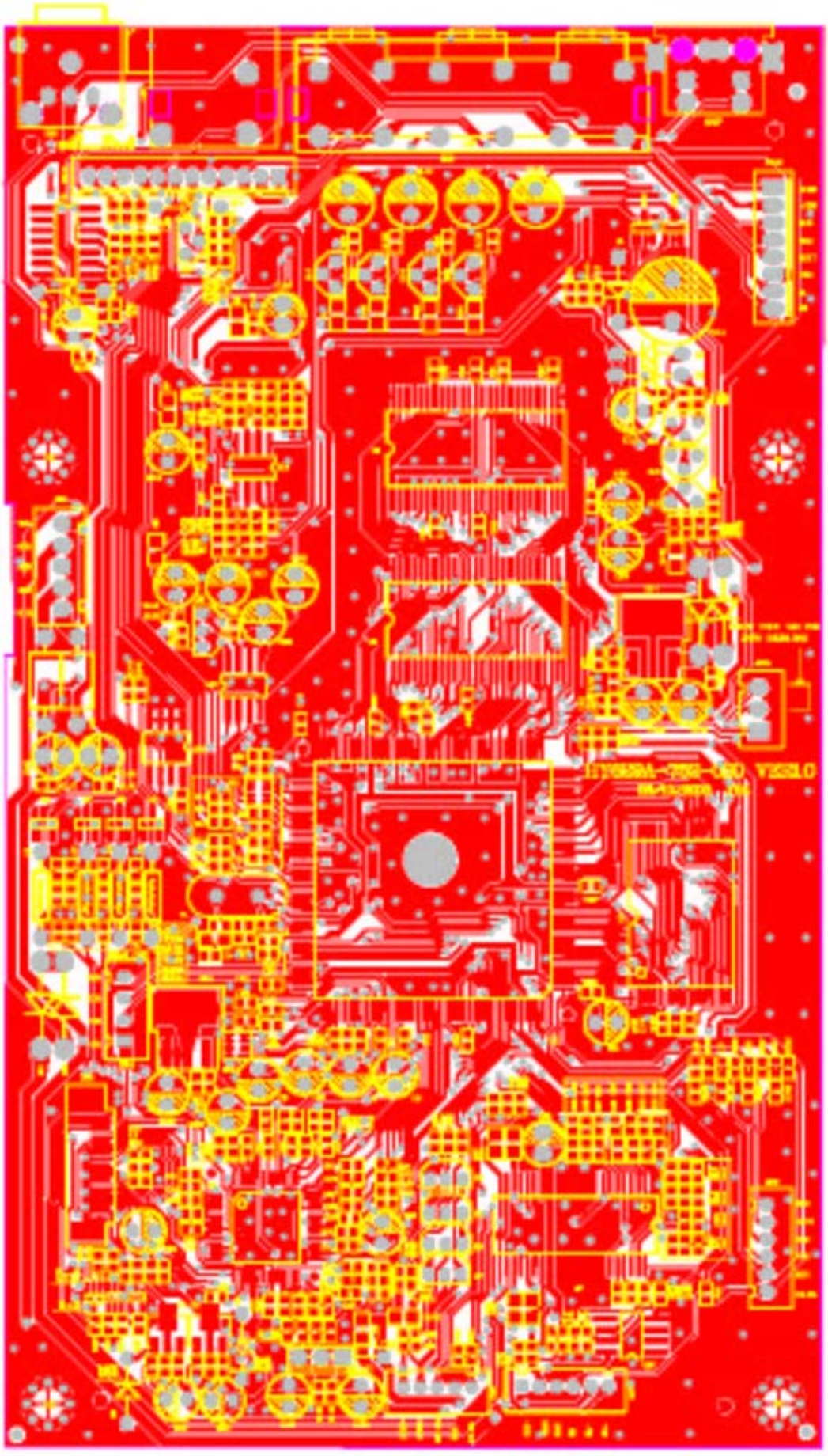
Fig 2-12 POWER&AV PORT

2.3.3. MPEG Composite (Fig 2-14)



2.3.2. MPEG Assembly Drawing (Fig 2-13)

2.3.2. MPEG Assembly Drawing (Fig 2-13)



2.4. Front panel Circuit Diagram and Component Layout

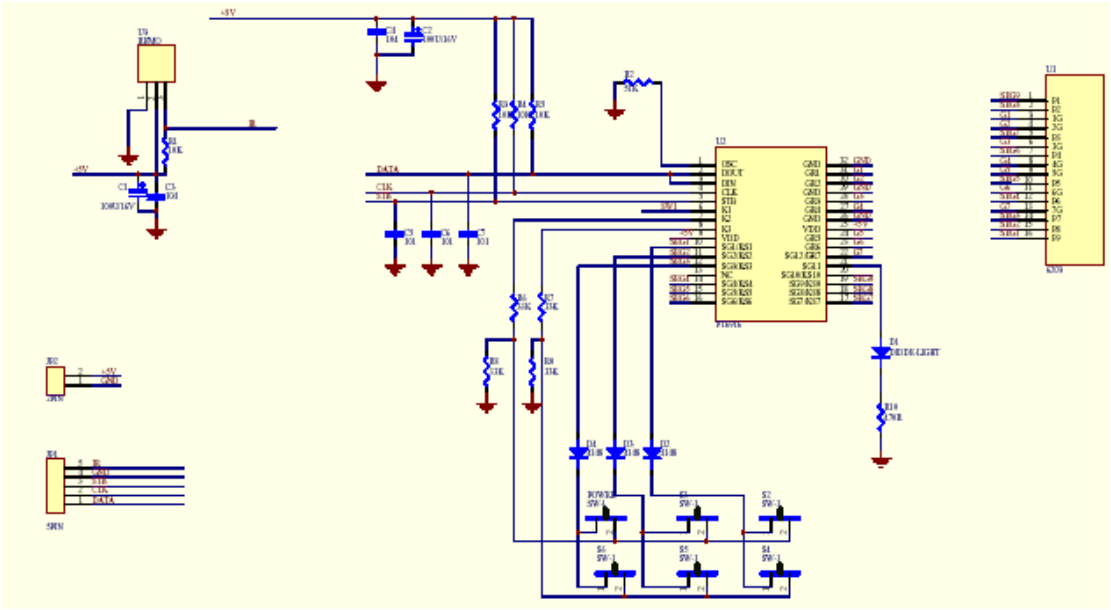


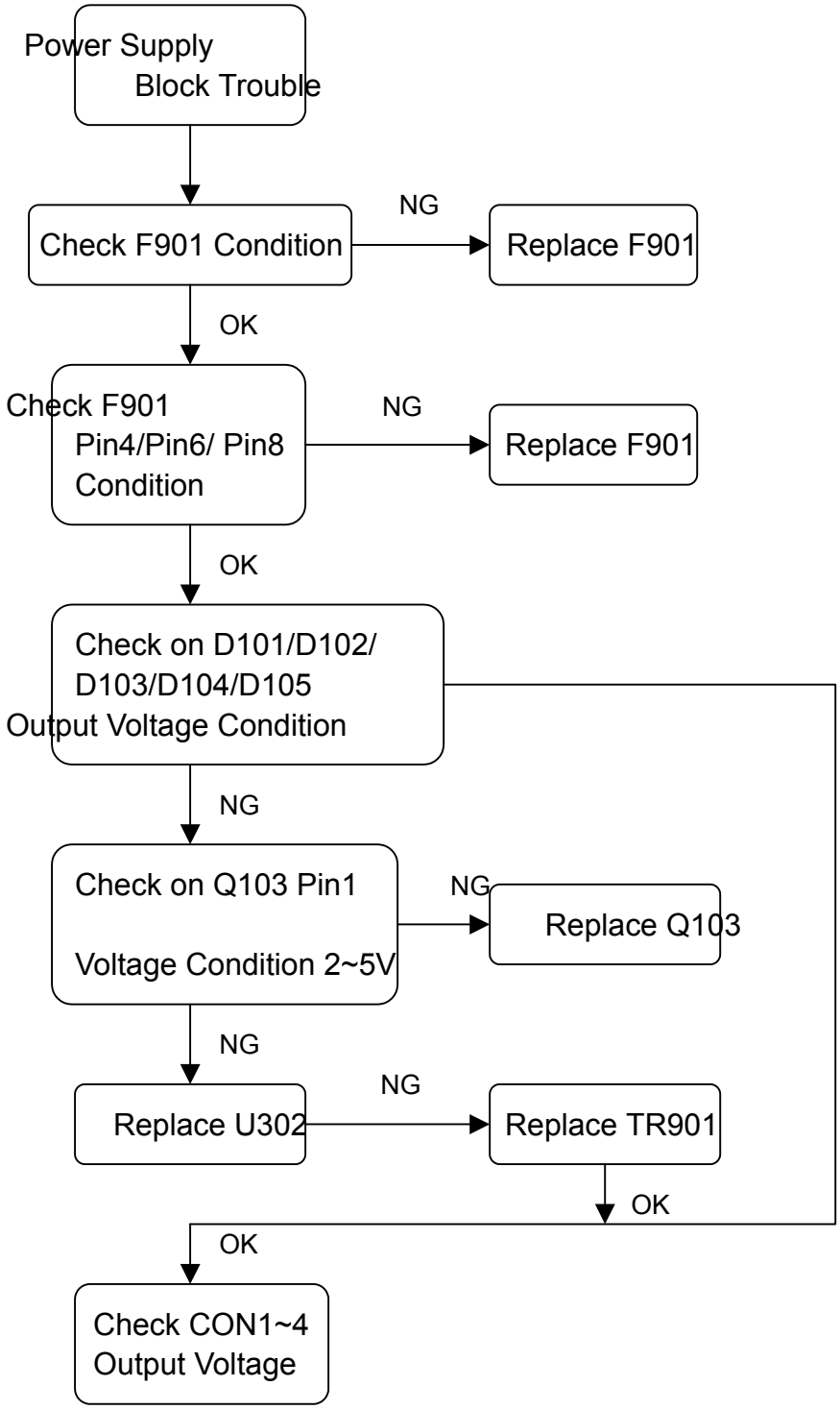
Fig 2-16 Front Panel Circuit Diagram

Fig 2-17 Front Panel Assembly Drawing

Fig 2-18 Front Panel Composite

3. Servicing Procedures

3.1. Power Supply Trouble Service Flow Chart



3.2. Read Disc Trouble Service Flow Chart

Read disc problem in a DVD player is a very complicated issue that may involve complex issues. This problem is not only relation to the electronic circuit, but also very much relation to the operation environment.

DVD loading unit is a very complicate part that contains big number of ESD components, which require specific equipment, tools and technique to repair; in general, service technician is not suggested to disassemble the DVD loading unit. It is suggest proving the trouble and replacing the complete DVD loading unit, instead of repairing the DVD loading unit in local workshop.

It is suggested to prove the faulty of a DVD loading unit by replacement by a good DVD loading unit.

Before checking the "NO Disc" Trouble, ensure excluding the following possibilities:

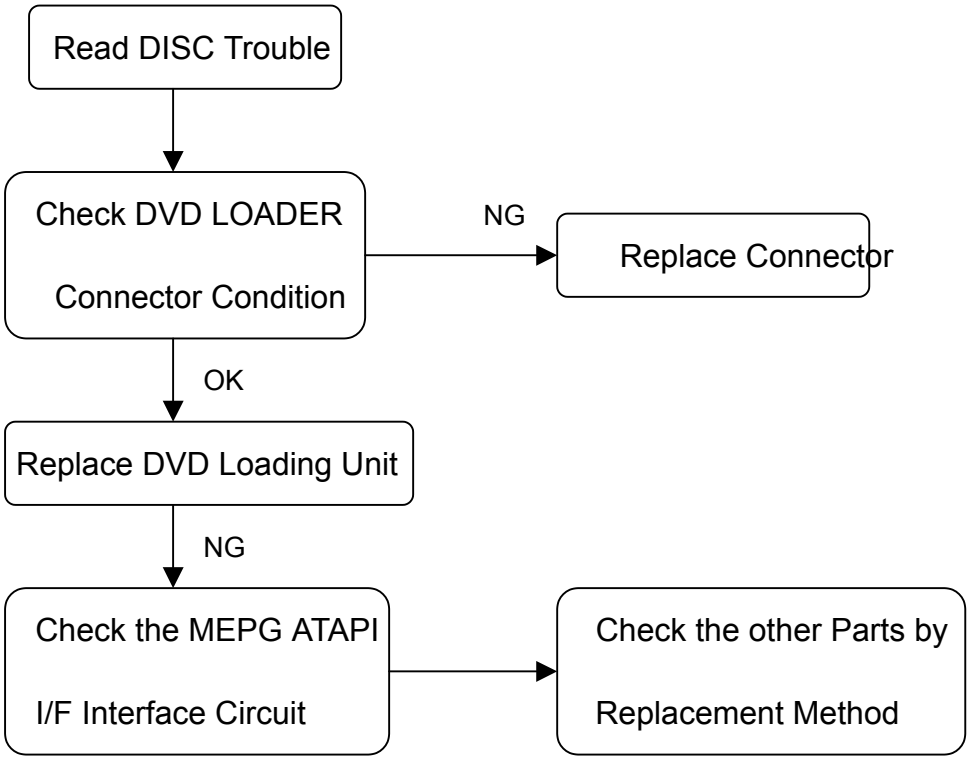
The test disc is damage.

AC power supply voltage dropped below the minimum required level.

DVD disc region code and color system is not matching to the DVD player or system setting.

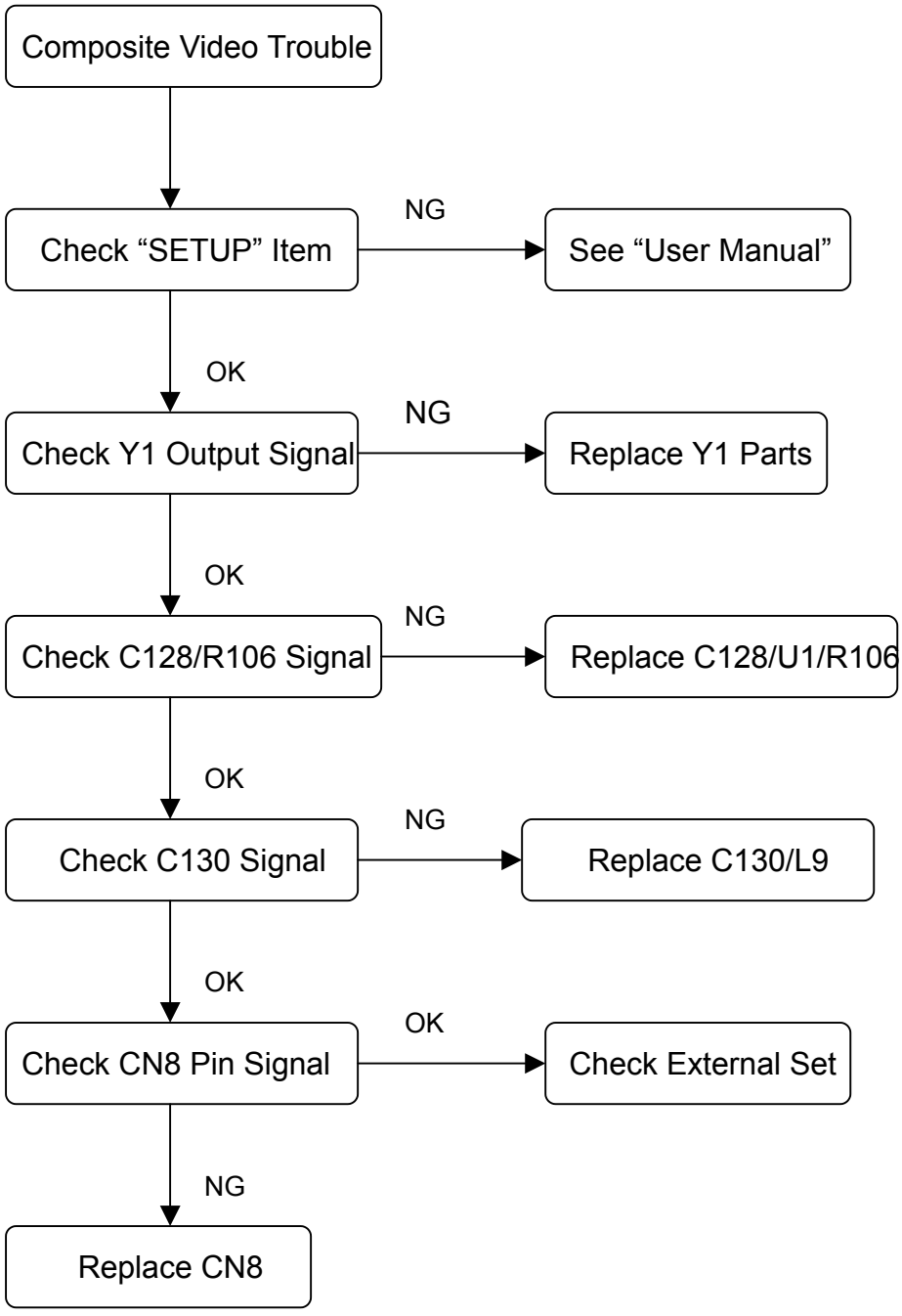
Moisture condensed inside the unit. (Power on the unit, without disc loaded, for 1/2 to 2 hours).

Service Flow Chart

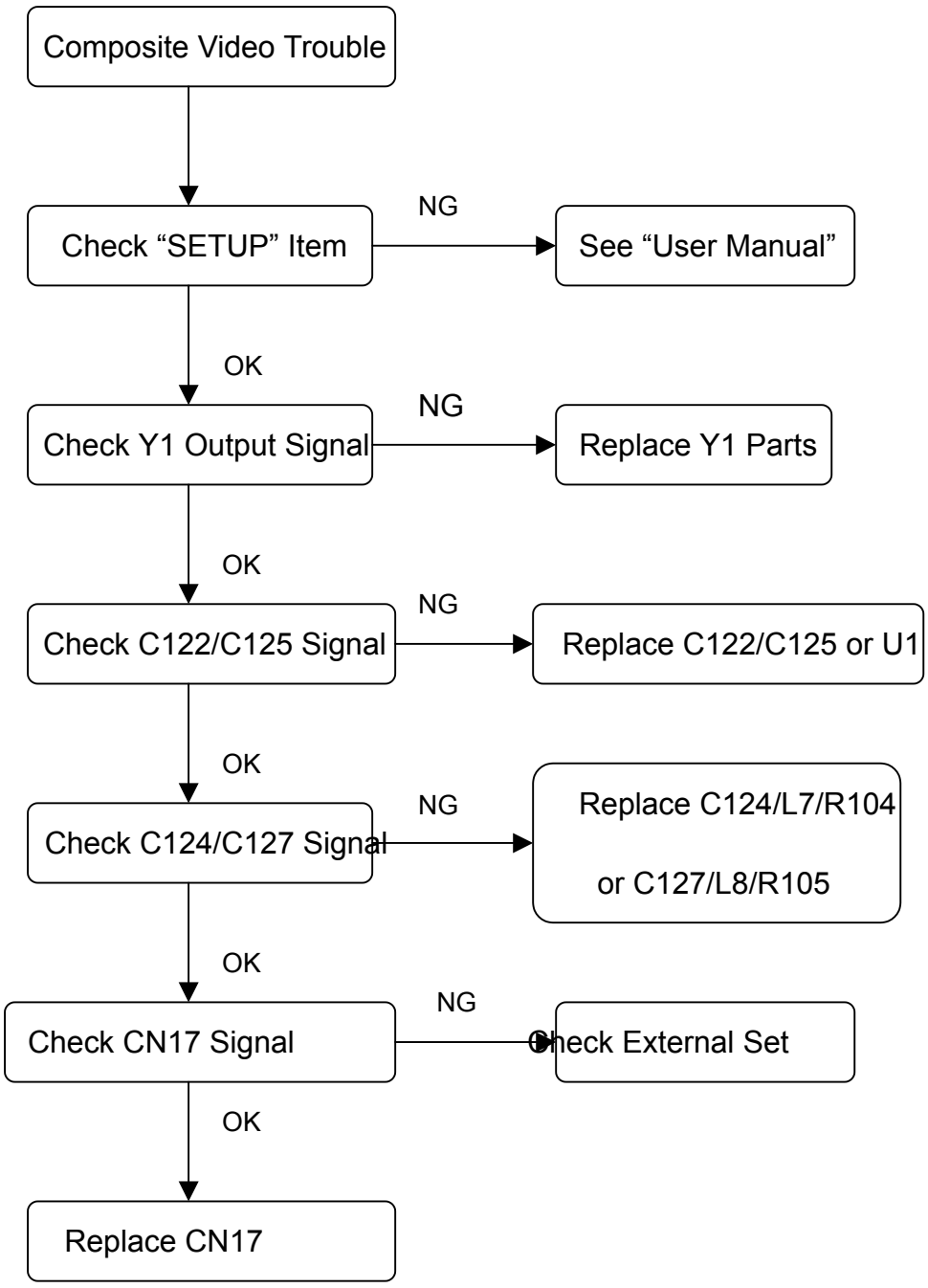


3.3. Video Trouble Service Flow Chart

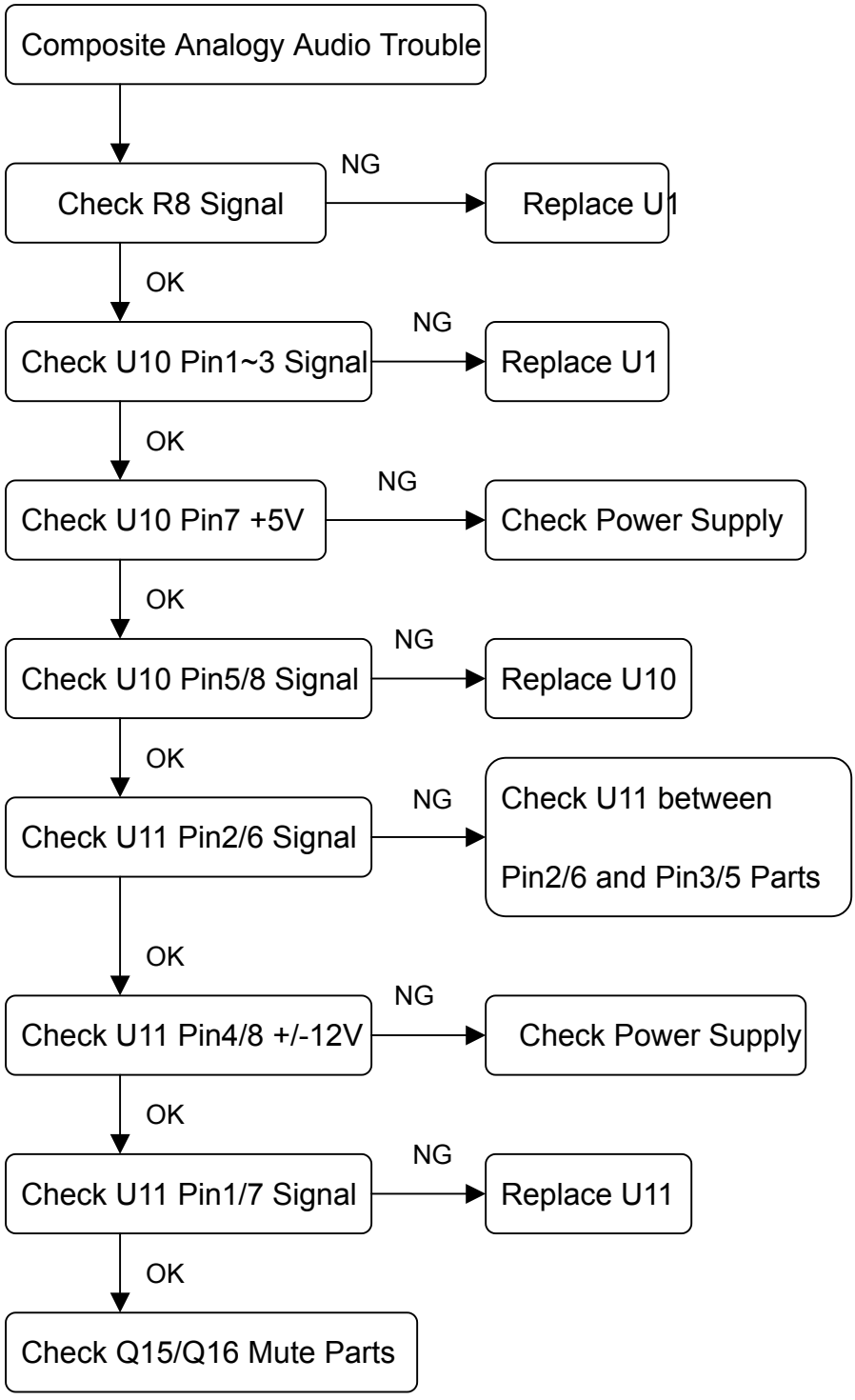
3.3.1. Composite Video Trouble Service Flow Chart



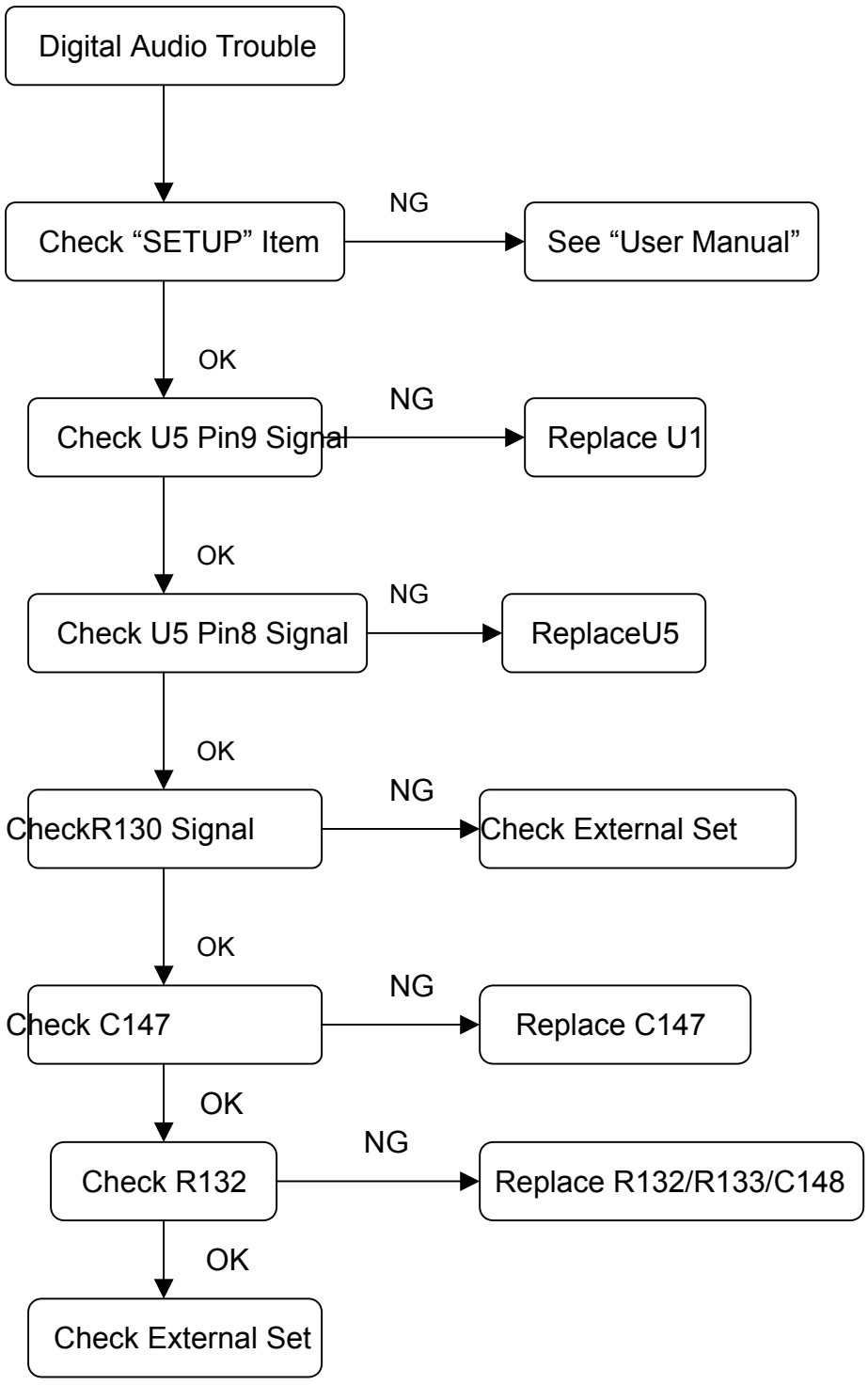
3.3.2. S-Video Trouble Service Flow Chart



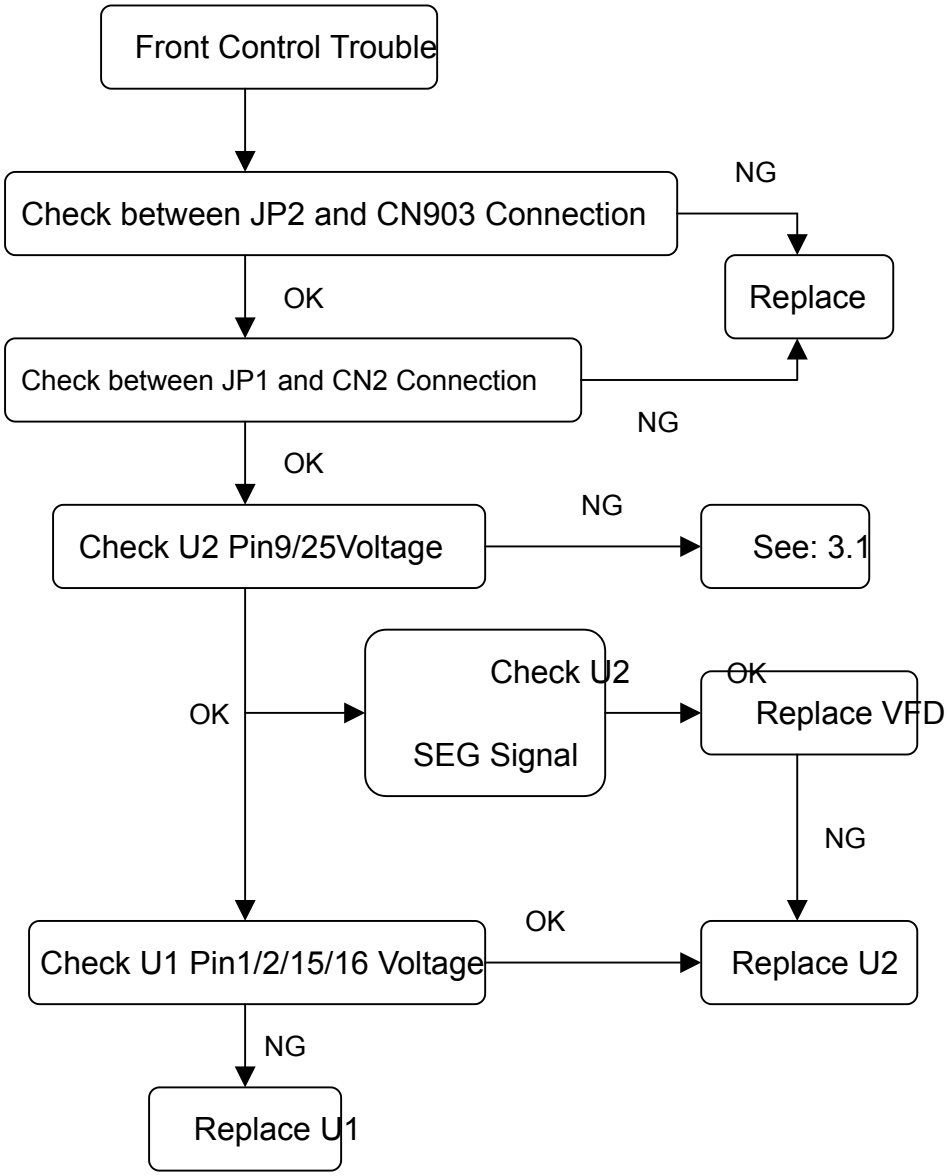
3.4. Composite Analogy Audio Trouble Service Flow Chart



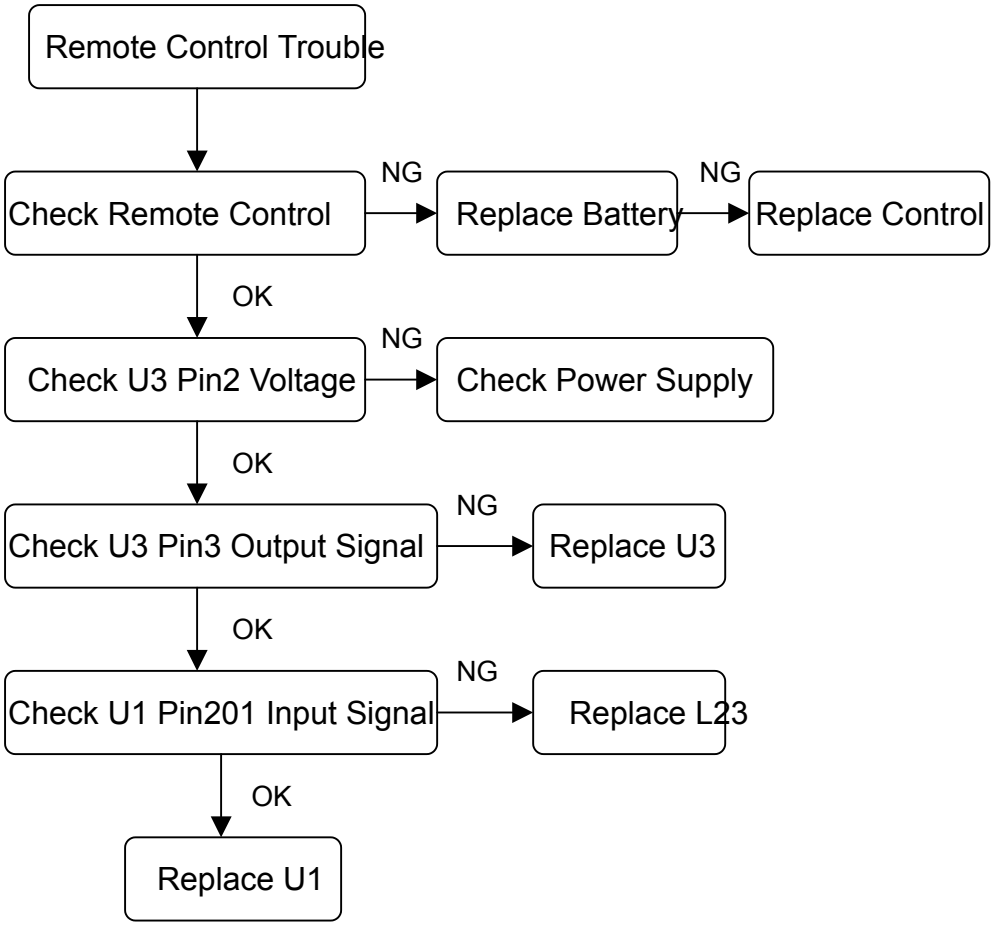
3.5. Digital Audio Trouble Service Flow Chart



3.6. Front Control Trouble Service Flow Chart



3.7. Remote Control Trouble Service Flow Chart



4. Parts List

4.1. Power parts list

NO.	PART NO.	DESCRIPTION	QTY	LOCATION
		Carbon Resistor		
1	M2R1130330433110	RT14-1/4W-30K±5%	1	R905
2	M2R1139330433110	RT14-1/4W-39K±5%	1	R902
3	M2R1110030433110	RT14-1/4W-10R±5%	2	R908 R118
4	M2R1120130433110	RT14-1/4W-200R±5%	2	R107,L101
5	M2R1110230433110	RT14-1/4W-1K±5%	1	R110
6	M2R1110330433110	RT14-1/4W-10K±5%	3	R111,R112,R102
8	M2R1110130433110	RT14-1/4W-100R±5%	3	R108,R109,R906
9	M2R1122030433110	RT14-1/4W-22R±5%	1	R904
10	M2R1147130433110	RT14-1/4W-470R±5%	2	R101,R104
11	M2R112R030433110	RT14-1/4W-2R±5%	2	R907,R909
12	M2R1110530233110	RT15-1/2W-1M-J	1	R900
12	M2R8833430133110	RYG1-1W-330K-J	1	R901
13	M2R8827330133110	RYG1-1W-27K-J	1	R903
14	M2R8810330133110	RYG1-1W-10K-J	1	R910
15	M2I00SS2N60B0000	SS2N60B TO220	1	Q901
		AC Porcelain Capacitor		
16	M2C1102G54000022	CT7-400VAC-102M	3	C903,C904,C909
17	M2C1104F84000022	CT-50V-104-Z	5	C107,C113,C114,C117,C120
18	M2C1151M44000022	CT81-1000V-151-K	1	C910
19	M2C1103L84000022	CT81-500V-103-Z	1	C908
20	M2C1472M89000022	CT81-1000V-472-Z	1	C906
		Electrolytic Capacitor		
21	M2C2476K59163222	CD293-47U-400V-M-105℃	1	C905
22	M2C2107T59061222	CD288-35V-100U-M	2	C101,C102
23	M2C2107B59051122	CD288-16V-100U-M	3	C103,C109,C115
24	M2C2337B59081222	CD288-16V-330U-M	1	C108
25	M2C2228C59051122	CD288-10V-2200U-M	1	C111
26	M2C2476E59051122	CD288-25V-47U-M	1	C907
27	M2C2337C59051122	CD288-10V-330U-M	1	C112
28	M2C5104F49000022	0.1uFK-275VAC	2	C901, C902
		Diode		
29	M2D1IN4007220000	1N4007-（DO-41A）	5	D901, D902, D903, D904,D106
30	M2D1HER107220000	HER107	2	D907,D908

NO.	PART NO.	DESCRIPTION	QTY	LOCATION
31	M2D1IN4148110000	1N4148-（DO-35）	1	D906
32	M2D1HER104220000	HER104	2	D102,D103,
33	M2D10SR360220000	SR360	1	D105
34	M2D1IN5392220000	1N5392	2	D108,D109
		Steady Diode		
35	M2D1BZX12V220000	BZX-12V-1/2W-（DO-35）	1	Z101
38	M2H20000L0710000	L071-10uH	1	L105
40	M2H20BC202290000	BC-20229	1	LF901
		IC		
41	M2I00PC817B00000	PC817B	1	U902
	M2ILTV8170000000	LTV817	1	U902
42	M2I000TL43100100	TL431A TO92	1	*Q104*
43	M2I0NCP1200P6000	NCP1200P60	1	U901
44	M2U110T0A5250V00	T0.5A 250V	1	F901
45	M2P3300000520000	5＊20	2	F901
		Transformer		
46	M2T11EEL193883BE	EEL19-3883B	1	TR901
		Jack		
47	M2P2200000VH3000	VH-3	1	CN901
49	M2P000000PH5A000	PH-5A	1	CN903
50	M2P0000TJC35A000	**TJC3-5A**	1	CN904
51	**********	J-10mm	5	JP1,JP3, JP4, D107, CN102
52	**********	J-5mm	1	JP6
53	M2A00GDP31400001	GDP-314	2	GDP1,GDP2
		PCB		
53	M2B000HY31509C24	HY315-1200-09C VER2.4	1	94V0 PCB

4.2. MEPG parts list

NO.	PART NO.	DESCRIPTION	QTY	LOCATION
		Chip Resistor		
1	M2R001R030811000	RC-05K1R0JT	5	R66 R67 R68 R69 R140
2	M2R0010030811000	RC-05K100JT	1	R1
3	M2R0010130811000	RC-05K101JT	4	R5 R82 R83 R84
4	M2R0033130811000	RC-05K331JT	1	R130
5	M2R0010230811000	RC-05K102JT	2	R6 R7
6	M2R0000031000000	RC-03K000OT	14	R11 R21 R22 R23 R41
				R85 R72 R121 R65
				R70 R86 R87 R88 R89
7	M2R0010031000000	RC-03K100JT	3	R96 R100 R101
8	M2R0022031000000	RC-03K220JT	2	R29 R26
9	M2R0033031000000	RC-03K330JT	5	R8 R9 R10 R12 R13
10	M2R0056031000000	RC-03K560JT	1	R138
11	M2R0062031000000	RC-03K620JT	4	R90 R99 R102 R103
12	M2R0075031000000	RC-03K750JT	1	R3
13	M2R0010131000000	RC-03K101JT	1	R125
14	M2R0012131000000	RC-03K121JT	1	R137
15	M2R0015131000000	RC-03K151JT	1	R19
16	M2R0022131000000	RC-03K221JT	7	R27 R28 R51 R52 R53 R56 R132
17	M2R0039131000000	RC-03K391JT	1	R20
18	M2R0047131000000	RC-03K471JT	3	R78 R79 R131
19	M2R0056131000000	RC-03K561JT	2	R110 R117
20	M2R0010231000000	RC-03K102JT	4	R133 R139 R141 R142
21	M2R0013231000000	RC-03K132JT	3	R38 R39 R40
22	M2R0033231000000	RC-03K332JT	3	R48 R109 R115
23	M2R0047231000000	RC-03K472JT	19	R2 R4 R15 R24 R25 R30 R34
				R49 R50 R97 R111 R112 R118
				R119 R126 R127 R128 R129
24	M2R0051231000000	RC-03K512JT	1	R81
25	M2R0056231000000	RC-03K562JT	6	R57 R58 R59 R75 R76 R77
26	M2R0068231000000	RC-03K682JT	1	R64
27	M2R0091231000000	RC-03K912JT	1	R35
28	M2R0010331000000	RC-03K103JT	11	R43 R60 R63 R73 R74
				R80 R91 R93 R98 R107 R114
29	M2R0011331000000	RC-03K113JT	3	R44 R62 R71
30	M2R0012331000000	RC-03K123JT	1	R42
31	M2R0013331000000	RC-03K133JT	1	R36
32	M2R0015331000000	RC-03K153JT	1	R17
33	M2R0018331000000	RC-03K183JT	2	R108 R116

NO.	PART NO.	DESCRIPTION	QTY	LOCATION
34	M2R0022331000000	RC-03K223JT	2	R45 R46
35	M2R0033331000000	RC-03K333JT	1	R92
36	M2R0047331000000	RC-03K473JT	1	R61
37	M2R0010431000000	RC-03K104JT	2	R18 R95
38	M2R0010531000000	RC-03K105JT	1	R47
		Chip Row Resistor		
39	M2R9947030899004	RCML08W470JT	1	RN1
40	M2R9975030899004	RCML08W750JT	1	RN2
		Chip Capacitor		
41	M2C0120F30060300	CC-0603CG120JN500T	4	C120 C123 C126 C129
42	M2C0220F30060300	CC-0603CG220JN500T	2	C2 C3
43	M2C0330F30060300	CC-0603CG330JN500T	1	C45
44	M2C0101F30060300	CC-0603CG101JN500T	9	C85 C92 C134 C139 C102
				C103 C104 C105 C148
45	M2C0151F30060300	CC-0603CG151JN500T	4	C119 C122 C125 C128
46	M2C0161F30060300	CC-0603CG161JN500T	4	C121 C124 C127 C130
47	M2C0221F30060300	CC-0603CG221JN500T	1	C60
48	M2C0471F30060300	CC-0603CG471JN500T	1	C73
49	M2C0561F30060300	CC-0603CG561JN500T	3	C71 C84 C93
50	M2C0102F44060300	CC-0603B102K500NT	15	C4 C74 C75 C76 C77 C78 C79 C80
				C83 C108 C100 C133 C137 C138 C142
51	M2C0222F44060300	CC-0603B222K500NT	4	C41 C42 C43 C44
52	M2C0272F44060300	CC-0603B272K500NT	1	C63
53	M2C0472F44060300	CC-0603B472K500NT	1	C88
54	M2C0562F44060300	CC-0603B562K500NT	3	C68 C69 C70
55	M2C0682F44060300	CC-0603B682K500NT	1	C58
56	M2C0273F54060300	CC-0603F273M500NT	2	C91 C87
57	M2C0223F54060300	CC-0603F223M500NT	1	C59
58	M2C0333F54060300	CT-0603F333M500NT	1	C81
59	M2C0104F84060300	CC-0603F104Z500NT	66	C6 C8 C10 C12 C13
				C14 C15 C16 C17 C18
				C19 C20 C22 C23 C24
				C25 C26 C27 C29 C30
				C31 C32 C33 C34 C35
				C36 C37 C38 C40 C46
				C47 C48 C49 C50 C51
				C56 C57 C61 C62 C64
				C66 C67 C72 C82 C86
				C90 C94 C95 C98 C115
				C117 C136 C141 C143 C149

NO.	PART NO.	DESCRIPTION	QTY	LOCATION
				C152 C154 C155 C157 C160
				C146 C162 C147 C101 C97
		Electrolytic Capacitor		
60	M2C2475F89051122	CD11-50V-4.7UF-M	1	C65
61	M2C2106E57051122	CD11-25V-10UF-M	3	C1 C131 C132
62	M2C2107B57051122	CD11-16V-100UF-M	24	C5 C7 C9 C11 C21 C166
				C28 C39 C89 C99 C150 C96
				C153 C156 C158 C159 C52 C55
				C116 C118 C161 C151 C113 C145
63	M2C2477C89081222	CD11-10V-470UF-M	4	C106 C107 C144 C164
64	M2C2108B59101622	CD11-16V-1000UF-M	1	C114
		Chip Inductor		
65	M2H0500M02U70805	L0805-2.7UH-500MA-K	1	L1
66	M2H0500M010U0603	L0603-10uH-500MA-K	2	L3 L4
		Chip Bead		
67	M2HL500M070R0805	L0805-500MA-70R	1	L13
68	M2HL500M070R0603	L0603-500MA-70R	10	L23 L24 L25 L26 FB1 L2
				FB3 FB4 L20 FB2
		Color loop Inductor		
69	M2H4LGA1UH1J0307	LGA0307-1.1UH-K	4	L6 L7 L8 L9
		Ferrite Bead		
70	M2H1RH3560083560	RH3.5*6*0.8	2	L12 L15
		Diode		
71	M2D1IN4148110000	1N4148-（DO-35）	5	D1 D2 D3 D4 D5
72	M2D1IN4007220000	1N4007-(DO-41A)	4	D15 D16 D10 D11
74	M2D1BZX5V1220000	BZX-5V1-1/2W-(DO-35)	1	Z1
75	M2D1BZX6V8220000	BZX-6V8-1/2W-(DO-35)	10	Z2, Z3, Z4, Z5, Z6, Z7
				Z8, Z9, Z10, Z11
		Transistor		
76	M2Q02SK301800000	2SK3018-(SOT-18)	3	Q1 Q2 Q3
77	M2Q000D130400000	KTD1304-(SOT-23)	2	Q15 Q16
78	M2Q02SB113200000	2SB1132-(SOT-89)	2	Q5 Q4
79	M2Q100S8050D2200	S8050D-(TO-92)	2	Q9 Q8
80	M2Q100S8550D2200	S8550D-(TO-92)	2	Q6 Q7
81	M2Q100A101502200	2SA1015GR(TO-92)	7	Q10 Q11 Q12 Q14 Q24 Q25 Q26
		Crystal		
82	M2L1127M00003000	27.000MHz-30ppm-THIRD-20PF	1	Y1
		IC		
83	M2I0ZR36762E0000	Zoran ZR36762-PQFP208(E0)	1	U1
	M2I0ZR36762B2000	Zoran ZR36762-PQFP208(B2)	1	U1
	M2I0ZR36762V0000	Zoran ZR36762-PQFP208(V0)	1	U1

NO.	PART NO.	DESCRIPTION	QTY	LOCATION
84	M2I0ZR3670700000	Zoran ZR36707-PQFP64	1	U6
85	M2I029LV80007000	MBM29LV800BA-70 PFCN	1	U4
	M2I039VF80000000	SST 39VF800A-70-4C-EK-TSOP48	1	U4
	M2I039VF80000001	SST 39VF800-70-4C-EK-TSOP48	1	U4
	M2I0M29W80070000	M29W800DT-TSOP48	1	U4
	M2ITE28F160C0000	TE28F160C3BD70	1	U4
	M2I039VF80090000	SST 39VF800-90-4C-EK-TSOP48	1	U4
	M2I029W800B70000	M29W800DB-70N	1	U4
86	M2IM12L16161A000	M12L16161A-7T	2	U2 U3
	M2IVT36171600000	VT361716T-6AA	2	U2 U3
	M2ITM50S11600000	TM50S116T-7	2	U2 U3
87	M2I0CS4334K00000	CS4334K-SOIC8	1	U10
88	M2IAZ1117H330000	AZ1117H-3.3V-(SOT-223)	1	U13
89	M2IAZ11170000000	AZ1117H-ADJ(SOT-223)	1	U14
90	M2I000D595400000	D5954-HSOP28	1	U7
91	M2IAZ4558AM00000	AZ4558AM-SO8	1	U11
92	M2I00078L0500100	78L05-(TO-92)	1	U9
94	M2I0L7805CV00100	L7805CV	1	U12
95	M2I074HC14D00000	74HC14D-SO14	1	U5
96	M2I0GP1F32T00100	GP1F553TZ/554TZ	1	CN6
97	M2I0MC3407200000	MC34072-SO8	1	U18
		Jack		
98	M2P0000TJC35A000	TJC3-5A	1	CN1
99	M2P88FPC24005000	JP24-05M	1	CN3
100	M2P000000PH5A000	PH-5A	1	CN5
101	M2P00000PH6AB000	PH-6A-B	1	CN2
102	M2P000000PH6A000	PH-6A	1	CN4
103	M2P660000S4KB000	S-4KB	1	CN17
105	M2P11000RCA1A000	RCA-1A-COAX	1	CN9
106	M2P11AV684120003	AV6-8.4-12-03	1	CN8
		PCB		
107	M2B100HY629AS012	HY629A-762-0S0 VER1.3	1	PCB

4.3. Front panel parts list

NO.	PART NO.	DESCRIPTION	QTY	LOCATION
		Electrolytic Capacitor		
1	M2C2107B57051122	CD11-16V-100UF-M	2	C1 C2
		Porcelain Capacitor		
2	M2C1101F44000022	CC1-50V-101-K	3	C5 C6 C7
3	M2C1104F84000022	CT81-50V-104-Z	2	C3 C4
		Carbon Resistor		
4	M2R1110330633110	RT13-1/6W-103-J	4	R1 R3 R4 R5
5	M2R1133330633110	RT13-1/6W-333-J	4	R6 R7 R8 R9
6	M2R1151330633110	RT13-1/6W-513-J	1	R2
7	M2R1147130633110	RT13-1/6W-471-J	1	R10
		Diode		
8	M2D1IN4148110000	1N4148-（DO-35）	3	D2 D3 D4
9	M2D100374N220000	LT0374N-43-M1	1	D1
		Jiggle Switch		
10	M2S00KAO06060501	KAO-6*6*5(230g)	6	POWER S2 S3 S4 S5 S6
		IC		
13	M2I00PT696100000	PT6961	1	U2
		IR		
14	M2IAT13812B00000	AT138BST-12M2	1	U3
		LED		
15	M2G11LCM07013G00	LC-MO7013G	1	U1
		Jump wire		
16	**********	JMP7.5	2	J1 J7
17	**********	JMP10	3	J2 J3 J5
18	**********	JMP5	1	J6
19	**********	JMP15	1	J4
		PCB		
20	M2B100HY166809E13	HY-166-809E-00S VER1.3	1	PCB

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