SONY

Training Manual

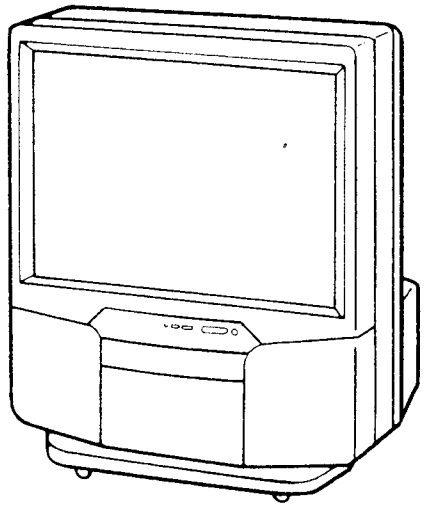
Projection Television

AP Chassis

Circuit Description and Troubleshooting Guide

KPR-41EXR95 Base Model

COURSE TVP-03



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Introduction

Sony has introduced a new line of rear projection sets which utilize an advance pro-optics 90 degree reverse deflection CRT. Pro-optics design results in a 20% reduction of CRT length with a 40% increase in sharpness over conventional set's. This design provides a shorter focal distance which allows for a slimmer TV body framing as well as improved beam spot characteristics over those of conventional 67 degree rear projection set's.

Due to the larger deflection angles different picture distortions, not normally seen in the 67 degree system, will appear. As a result, new convergence circuits and adjustments are employed.

Designated the AP chassis, it shares much of the same FN chassis circuit boards and design configuration built into the new Sony XBR line of Super Flat Screen television set's. For information on the FN chassis, please refer to the CTV-20 Training Manual, Part # CTV-20992-1.

This manual begins by providing an overview of the entire television. After the overview, detail circuit analysis along with simplified drawings are provided. Troubleshooting information and testing procedures are provided where applicable. A separate insert containing troubleshooting flowcharts, diagrams and waveforms are provided to aid the technician in the repair of this chassis.

Projection Basic Overall Block Diagram

A simplified block diagram of the projection set AP chassis is shown below. The major circuits for this chassis are contained on the following circuit boards:

G Board AC input filtering, Voltage Doubler and Rectifier, Power Regulating Transformer (PRT), Standby Power and Power Input Transformer (PIT).

A-Board Standby 5V regulator, Relay Drive, Protection circuits, Tuner, Front Speaker Amp, IK-Detect, Horizontal Drive and Horizontal Output, and Pincushion Modulation.

V-Board RGB Horizontal Deflection Centering.

N-Board High Voltage Drive and Regulation, Flyback Transformer, Focus Block and High Voltage Block.

M-Board System Control.

S-Board On Screen Menu Display Control CPU.

P1-Board Picture in Picture (PIP).

E2-Board Luminance Sharpness Control, Menu Display Character Generator, Main picture and PIP RGB switch.

E1-Board Y/C Jungle IC.

CR, CG, CB Boards RGB CRT Drives.

DS-Board Sine Wave Generator.

D-Board Multiplier, Wave Generator, Matrix, RGB Sub and Main Vertical Drive and Deflection.

U-Board Audio/Video Input/Output switching and Y/C Separate.

UT-Board External Audio/Video I/O terminal and speaker output.

Y2-Board MTS Decoder, Bass/Treble Control, and I^2C EEPROM.

X2-Board Surround Sound Processor.

H2-Board Demo User Push Button Controls.

H1-Board Power ON/OFF, TV/Video, Volume Up/Down, Channel Up/Down User Push Button Controls.

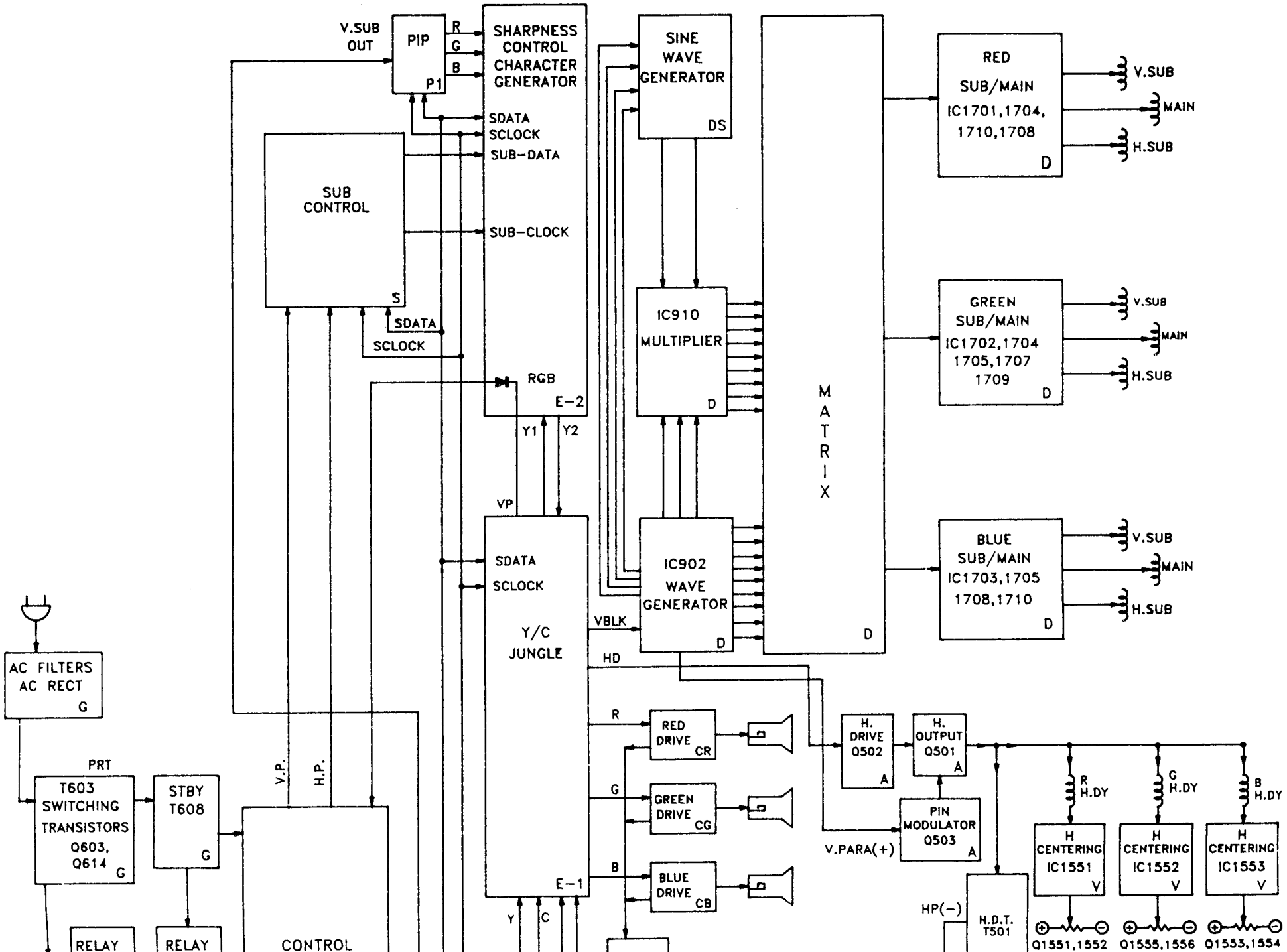
Operation

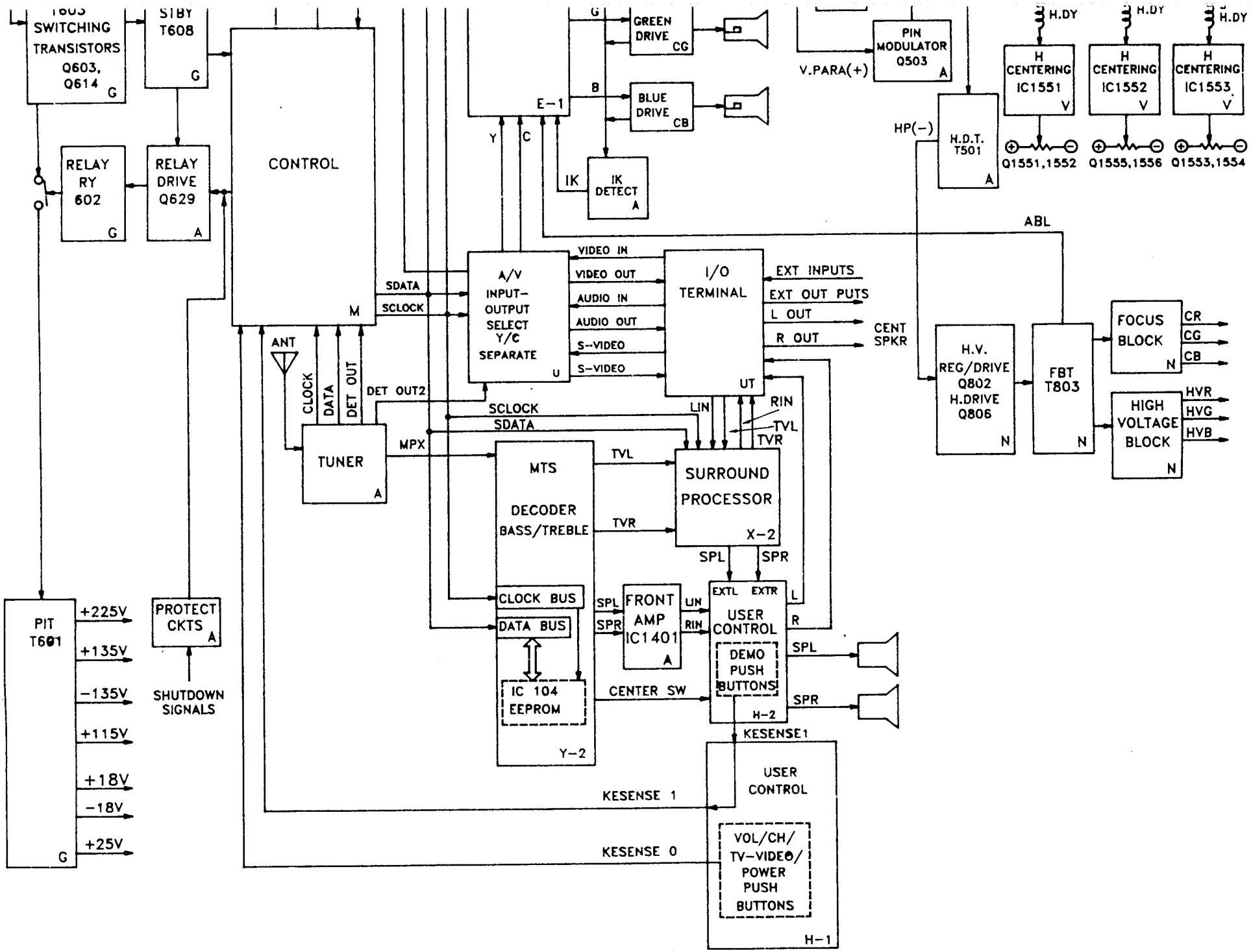
The 117Vac is input to the G-Board where it is noise filtered and DC rectified. The resulting DC voltage is coupled to a Power Regulating Transformer (PRT) and to switching transistors Q603 and Q614 circuit. The switching transistors oscillate with the PRT whenever the set is connected to the AC line. The oscillations produce a Pulse Width Modulated (PWM) voltage. In turn, the PWM voltage drives standby transformer T608 to produce standby 17Vdc. The 17Vdc standby voltage feeds the set's Power ON relay and 5Vdc regulator IC204 (not shown). IC204 powers the Control Microprocessor IC001 on the M-Board.

To turn the set ON, control IC001 in the control circuit outputs a relay drive signal to Q629. Q629 energizes RY-602, closing its contacts, which couples the PWM signal from the Switching and PRT circuit to Power Input Transformer (PIT) T601. The Power Input Transformer is responsible for producing the primary voltages used throughout the set. In the event the protection circuits sense a circuit misoperation, such as horizontal deflection loss, a protection latch is triggered. This removes relay drive thus powering down the set.

The control IC, located on the M-Board, communicates initially with EEPROM IC104 located on the Y2-Board, via the I^2C bus, so as to load into its internal CPU RAM all pertinent data such as:

* The alignment settings.
* Whether the set was last ON or OFF.
* The last active video input source. (In the case of the tuner, the last station viewed).
* The feature control settings for every video input source.


V.SUB OUT
PIP
R
G
B
P1
SHARPNESS CONTROL CHARACTER GENERATOR
SDATA
SCLOCK
SUB-DATA
SUB-CLOCK
SUB CONTROL
S
SDATA
SCLOCK
RGB
E-2
Y1
Y2
VP
SDATA
SCLOCK
Y/C JUNGLE
E-1
Y
C
SINE WAVE GENERATOR
DS
IC910 MULTIPLIER
D
IC902 WAVE GENERATOR
D
VBLK
HD
MATRIX
D
RED SUB/MAIN IC1701,1704, 1710,1708
D
V.SUB
MAIN
H.SUB
GREEN SUB/MAIN IC1702,1704 1705,1707 1709
D
V.SUB
MAIN
H.SUB
BLUE SUB/MAIN IC1703,1705 1708,1710
D
V.SUB
MAIN
H.SUB
R
RED DRIVE CR
G
GREEN DRIVE CG
B
BLUE DRIVE CB
H. DRIVE Q502
A
H. OUTPUT Q501
A
PIN MODULATOR Q503
A
V.PARA(+)
R H.DY
G H.DY
B H.DY
H CENTERING IC1551
V
H CENTERING IC1552
V
H CENTERING IC1553
V
Q1551,1552
Q1555,1556
Q1553,1554
HP(-)
H.D.T. T501
AC FILTERS AC RECT
G
PRT
T603 SWITCHING TRANSISTORS Q603, Q614
G
STBY T608
G
RELAY
RELAY
V.P.
H.P.
CONTROL



PROJECTION BASIC OVERALL BLOCK DIAGRAM

Once data communication with the EEPROM IC stops, the control IC synchronizes all data transfer along the I^2C Bus using the VP (Vertical Pulse) signal output from the Y/C Jungle IC on the E1-Board.

The control IC responds to key matrix or SIRCS inputs from the H-1 and H-2 User Control Boards then acts on these control inputs by communicating with the peripheral ICs via the I^2C Data Bus. In the case of video inputs, the control IC can select from various external video inputs. These inputs are applied either from the I/O Terminal UT-Board or from the tuner (DET OUT 2), via the A/V Input Output Select switch on the U-Board.

From the A/V Input/Output Select switch, the video input signal is separated into Y and C components and input to the Y/C Jungle IC on the E1-Board. The Y signal (Y1) is output from the Y/C Jungle IC and input to the Sharpness Control circuits on the E2-Board. The Sharpness Control circuits enhances the Y signal and inputs it back to the Y/C jungle IC (as the Y2 signal). The Y and C signals within the Y/C Jungle IC are then processed into RGB signals and output to their respective red, green and blue CRTs via the CR, CG and CB circuit Boards.

The Y/C Jungle IC outputs the main horizontal drive signal to the horizontal driver and horizontal output stage. The horizontal output signal is modulated with a vertical parabola signal from the PIN modulator to correct for the CRT's pincushion distortions. The horizontal deflection signal drives the deflection yokes for all three CRT's. The yoke return signals receive a dc offset through the horizontal centering circuits to allow the picture to be centered.

The horizontal output deflection signal is also input to the horizontal output transformer (H.O.T). The horizontal output transformer feeds the hi voltage Drive stage, which in turn feeds the flyback transformer. The flyback transformer output is connected to the high voltage block, which in turn, distributes the high voltage to the CRTs and the Focus Block.

The sub control circuits on the S board generate tuner station numbers, volume up/down, brightness, contrast, "on screen display graphic symbols", etc., over the main picture. The sub control circuits generates these graphic symbols with the aid of vertical and horizontal sync, and data and clock signals which are output from the control IC. The graphic symbols, output from the sub control IC, are input to the character generator circuits within the E2-Board via sub data and sub clock signals. From the internal character generator, the On Screen symbols are sent to the Y/C Jungle IC, on the E1-board, and mixed with the output RGB signals.

The Picture In Picture (PIP) circuitry is located on the P1-Board. To generate the PIP picture, the control IC inputs data and clock signals to the PIP controller via the I^2C Bus. The PIP Controller processes the V. SUB signal picture information from the U-Board A/V Select and Y/C Separate circuits for the child picture. From this signal, the PIP circuit outputs separate RGB signals to the sharpness control/character generator circuits on the E2-Board. Within the E2-Board, the PIP picture information can be mixed with the "menu on screen display" signals generated by the SUB Control circuits on the S-Board. From the sharpness control/character generator circuits the PIP signal is finally input to the Y/C Jungle as Separate RGB signals.

The MTS decoder processes the multiplex (MPX) signal output from the tuner into separate Tuner Left (TVL), Tuner Right (TVR), Speaker Left (SPL) and Speaker Right (SPR) signals, and outputs these signals to their respective circuit boards. In the case of the Tuner Left/Right signals, they are input to the surround processor stage and output to the set's speakers via User Control H2-Board and to the external speaker via the I/O Terminal U-Board. The surround sound processor acts on the audio signal through user control inputs via control IC outputs to the I^2C Data Bus.

The registration circuits are located on the D-Board. The signals necessary to converge the RGB color signals are generated by wave generator IC902, multiplier IC910 and the Sine Wave Generator circuit. These signals are sent to a potentiometer matrix to allow adjustment of the set's registration. The output signals from the matrix are fed to separate sub deflection yokes via their respective sub deflection drives.

Power ON

Overview

The purpose of the Power ON circuit is to supply main power from the PRT switching supply section to the set's Power Input Transformer (PIT) section. When the set is connected to the AC outlet, only the standby section receives power form the PRT section. Therefore, the output of the PRT switching supply must be switched ON to the PIT. The main power section consists of a power regulating transformer, PRT T603, and dual switching power converter transistors Q603 and Q614. Since the operation of the Switching Power Converter circuit is described later, only the events pertaining to the operation of the main power supply will be described.

Operation

Controller IC001 responds to a LOW from either the Power ON switch S1606 at IC001/pin 8 or from the SIRCS Detector IC1601 at IC001/pin 11. IC001/pin 21(RLYO) then outputs a HIGH through connector A-11/pin 5, G-11/pin 5, R694, D638, and R687 to the base of relay drive Q629. This energizes relay RY-602, which closes its contacts. As a result, current flows from AC ground through power input transformer (PIT) T601, C623, PRT T603, Switching Power Converters Q603 and Q614, Bridge Rectifier Section D633, R662, Line Filter network, F601 to the AC line. The flow of current through the primary of the PIT induces a current in the secondary of the PIT.

D603 provides 18Vdc to relay RY-601 via R689. RY-601 is immediately energized through Q629 collector to emitter junction, R688, connectors G-11/pin 7 and A-11/pin 7 and D645. This closes the relay contacts. As previously described, relay RY-602 is powered by the standby 12Vdc regulator IC602, via bridge rectifier D632 and standby transformer T608. The control IC001 is powered by the 5Vdc regulator IC205/pin 1 via standby 12Vdc Regulator IC602.

Troubleshooting

When troubleshooting for a "no power ON" symptom, first verify the operation of the Standby power supply section (Refer to the "Standby Power" Troubleshooting section of this manual). Also pay special attention to the items that appear to work, such as a relay click noise, the presence of CRT filament lighting, etc.. Much of this information will save you troubleshooting time. If the standby power supply section is operating but the set's secondary outputs are dead, then proceed with the following:

1. Apply AC power and turn the set ON. Check for 0.7Vdc at the base of Q629. If missing, check for 5Vdc at connector G-11/pin 5. If missing, troubleshoot control IC001 circuits on the M-Board. Check for 5Vdc at M-1/pin 12 (not shown). If okay, check for a LOW at connector M-1/pin 11 when the power button is pressed, and for SIRCS inputs at M-1/pin 4 when the remote power key is pressed. If okay the problem is on the M-Board.

2. If 5Vdc is present at M-1/pin 12, check for 2.3Vdc at the anode of D638. If it is 1.5Vdc or less, suspect the OVP circuits. (Refer to the "Main Power Supply Shutdown Protect" troubleshooting section of this manual).

3. If okay, check for a LOW at connector G-11/pin 6. If okay, check R-602 relay contacts for continuity.

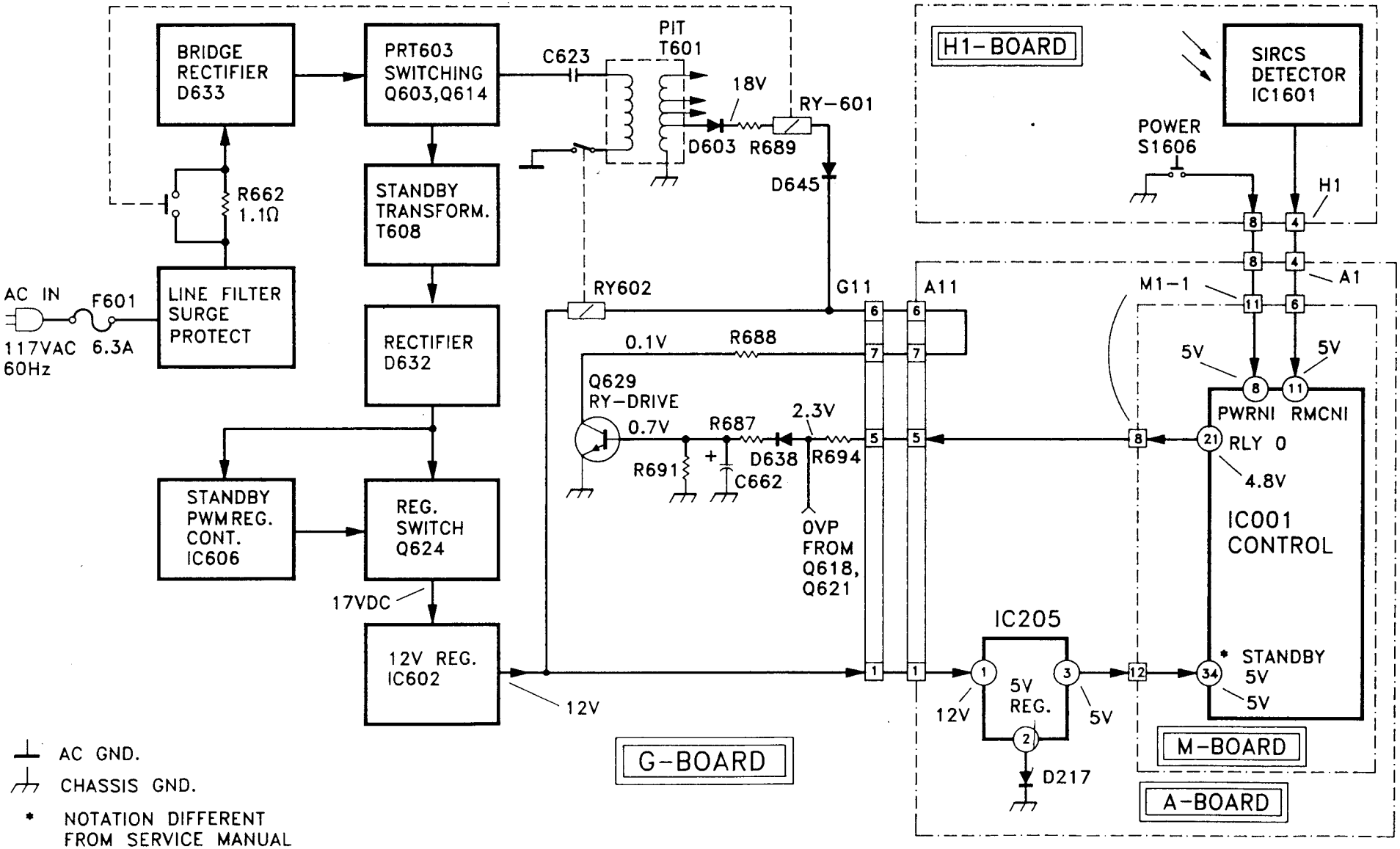
If the problem is traced to the M-Board, you can easily operate the set in the following manner:

A. Connect the set to a variac and input 70Vac.

B. Apply 5Vdc to connector G-11/pin 5 from an external DC supply source. By doing this you will not have defeated the OVP circuits. It will continue to operate in the event a problem exists elsewhere.

The set's relays should energize and PIT secondary voltages should be present.

NOTE: First, apply 70Vac to the set. Then, apply 5Vdc to G-11/pin 5. Failure to follow the above order will prevent the set from powering ON due to under voltage circuit protection.


BRIDGE RECTIFIER D633
PRT603 SWITCHING Q603,Q614
C623
PIT T601
18V
RY-601
D603
R689
D645
R662 1.1Ω
STANDBY TRANSFORM. T608
AC IN
F601
117VAC 6.3A 60Hz
LINE FILTER SURGE PROTECT
RECTIFIER D632
RY602
G11
A11
0.1V
R688
Q629 RY-DRIVE
0.7V
R687
2.3V
R691
D638
R694
C662
OVP FROM Q618, Q621
STANDBY PWM REG. CONT. IC606
REG. SWITCH Q624
17VDC
12V REG. IC602
12V
G-BOARD
H1-BOARD
SIRCS DETECTOR IC1601
POWER S1606
H1
M1-1
A1
5V
PWRNI
RMCNI
RLY 0
4.8V
IC001 CONTROL
IC205
5V REG.
12V
5V
D217
* STANDBY 5V
M-BOARD
A-BOARD
AC GND.
CHASSIS GND.
* NOTATION DIFFERENT FROM SERVICE MANUAL

POWER ON

Standby Power

Overview

The standby power supply found in the KPR-41EXR15 projection set is a variable frequency (20kHz - 35kHz) chopper converter circuit. It consists of a power regulating transformer (PRT), dual power converter transistors Q603 and Q614, standby transformer T608, a pulse width modulator (PWM) 17 volt standby regulator control IC606, and standby 12 volt regulator IC602.

The standby section operates whenever the set is connected to the AC line. The standby 17 volt regulator circuit feeds the 12 volt standby regulator and the P3-Board. The P3-Board is found only in models that have a second tuner. The standby 12 volt regulator circuit feeds power relay RY601 and the set's Control IC via a 5 volt regulator IC located on the A-Board.

AC Input

The 117Vac power line is coupled through connector G-8/pins 1 and 2, line fuse F601, line filter (LFT) T606 and current limiting resistor R662 to AC power rectifier D633. R662 serves to limit the initial inrush AC current flow as the filter capacitors charge during standby and the initial main power ON mode. The set is in standby anytime it is connected to the AC line. In standby R662 will drop 0.15Vac.

When the set's main power is turned ON, the contacts in relay RY601 will close and remove R662 from the series AC current path leading to power rectifier D633. This allows full AC power to be applied to the power rectifier.

The chassis ground is connected to the AC line through the RC filter network consisting of R667, C649 and C647. This in turn, provides a return path for the isolated COLD chassis ground circuits to the AC power line for noise suppression.

Voltage Dependent Resistor VDR601 protects the set from conditions such as lightning, by clamping voltage spikes across the input AC line .

The 117Vac line voltage is rectified by D633, R663, R668, C639 and C648, R663, R668, C639 and C648 to form a voltage doubling circuit which outputs 305Vdc when measured with respect to HOT AC ground. R663 and R668 are bleeder resistors. They discharge C639 and C648 when the set is unplugged.

Connector G-9 is a test plug for verifying AC input to the set.

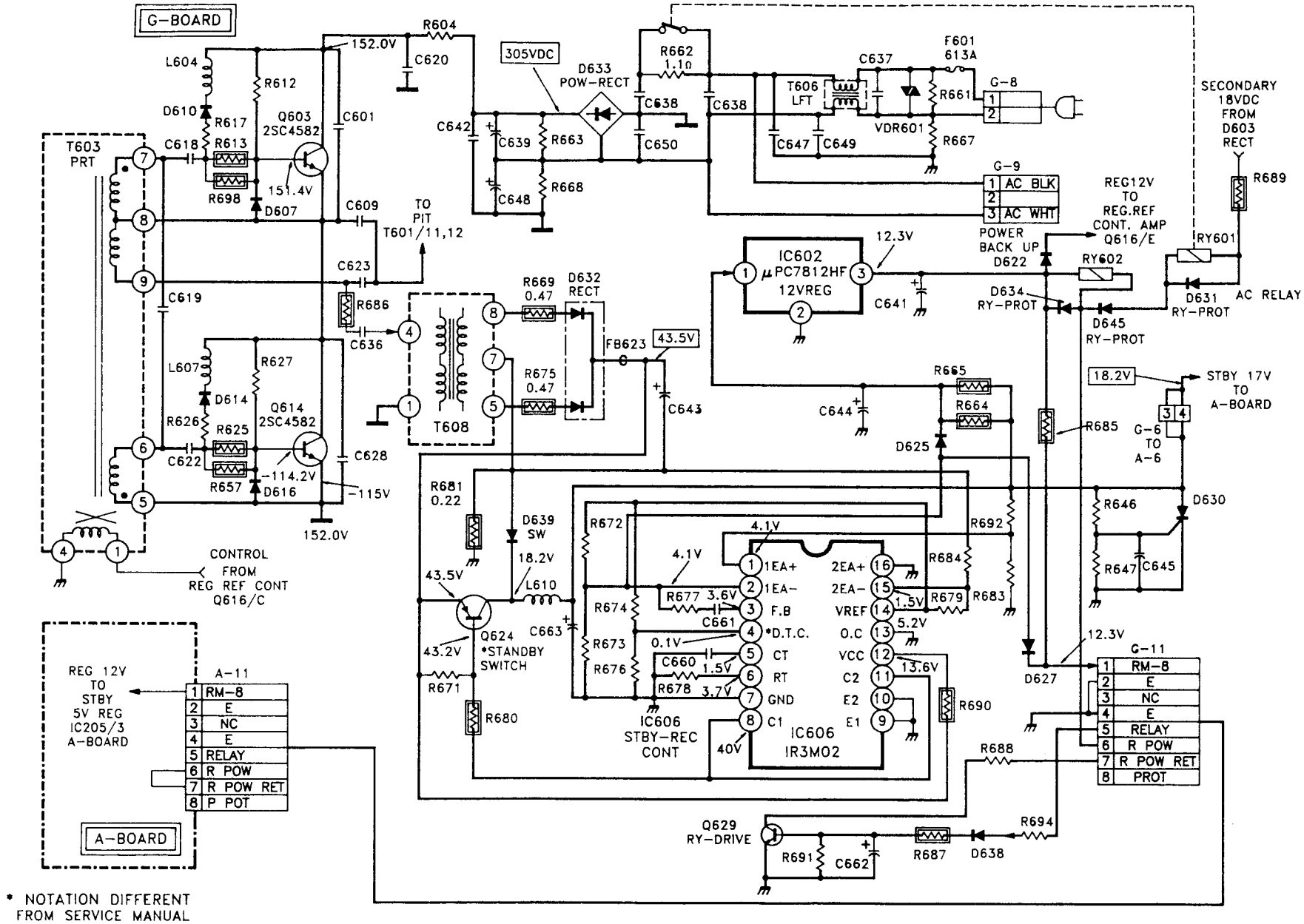
Switching Power

As previously indicated, the standby power supply consists of chopper circuit Q603, Q614 and PRT T603. When the set is plugged into the AC line, rectified 152Vdc is coupled to the collector of Q603. R612 provides a slight forward bias to Q613. This initially starts current flow from AC ground through the following components: T608/pin 1 and pin 4, C636, R686, PRT T603/pin 9 and pin 8, through Q603's emitter collector junction, R604, and bridge rectifier D633.

The initial current flow generates a voltage at PRT T603/pin 7, which is coupled through C618, R613 and R698 to Q603's base junction. As a result, Q603 turns fully ON, C636 charges rapidly stopping the flow of current through T603. The voltage at T603 /pin 7, therefore, immediately reverses polarity. This completes the positive half cycle of current flow through T603.

The reversal in voltage, at T603/pin 7, causes Q603 to turn OFF and a positive voltage to be generated at T603/pin 6. This voltage is coupled through C622, R625 and R657 to the base of Q614. As a result, Q614 turns ON, causing the build of energy in T603 to collapse and C636 to discharge from AC ground through the following components: Q614 emitter collector junction, T603/pin 8 and pin 9, C623, R686, C636, T608/pin 4 and pin 1. This completes the negative half cycle of current flow through T603. Q603 will now turn ON again, as described previously, and maintain oscillation.

The resonant frequency in the standby mode is 21kHz, which is mainly determined by the inductance between T603/pin 7 and pin 8 and C618. Later we will discussed how this frequency is varied to maintain regulation.



STANDBY POWER

Standby Pulse Width Modulator (PWM)

The standby power section is a 17 volt PWM voltage regulated circuit, comprised of switch Q624 and standby control IC606. The secondary current from standby transformer T608/pins 8 and 9 is rectified to 43.5Vdc by D632 and filter capacitor C643. This 43.5Vdc is applied to the emitter of Q624 and to IC606/pin 12 (Vcc) through voltage dropping resistor R690. Q624 is switched ON/OFF by PWM pulses output from IC606/pin 8 and pin 11. These pulses are applied through R690 to the base of Q624 to produce 17. 5Vdc, through filter network L610 and C663.

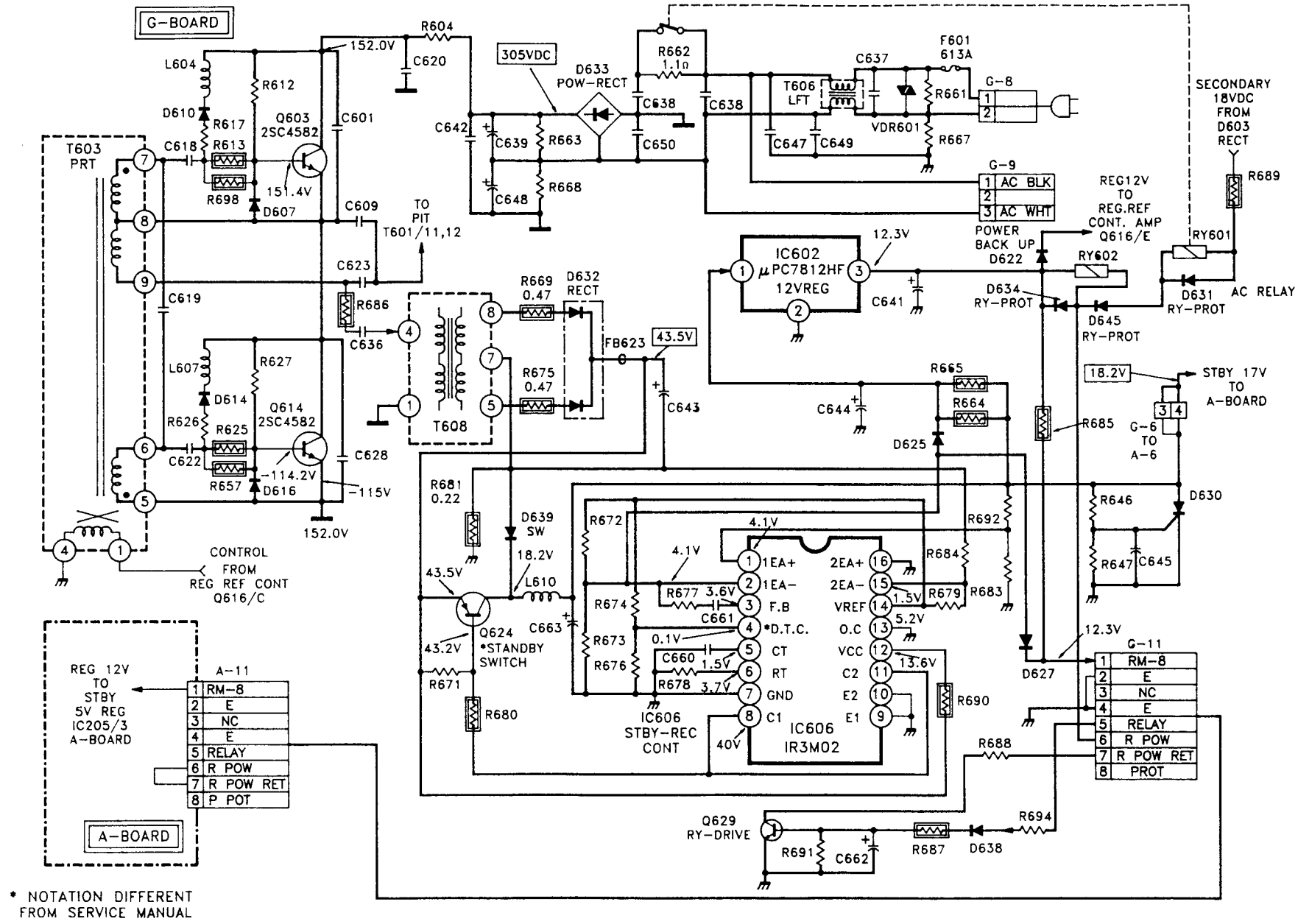
The switching frequency is determined solely by C660 and R678 at IC 606/pins 5 and 6, which produces a 50kHz sawtooth signal. To maintain regulation, a sample of the regulated 17.5Vdc, output from L610, is coupled through voltage divider R692 and R683 to IC606/pin 1. This voltage is then compared with a sample of an internally generated stable DC reference output from IC606/pin 14 and coupled through voltage divider R674 and R676 to IC606/pin 4. The duty ratio of the PWM pulses from IC606/pins 8 and 11, depend on the voltage difference between IC606/pins 1 and 4.

The output current is limited for short circuit conditions by the voltage reference set through voltage divider resistors R681, R684 and R679 at IC606/pin 15. Should the load current rise above 1.6A, the PWM output from IC606/pins 8 and 11 is inhibited. As a result, Q624 is prevented from turning ON.

Over voltage protection is sensed by the crowbar circuit comprised of R646, R647, C645 and D630. The crowbar circuit will trigger in the event the 17 volt line exceeds approximately 27Vdc. As a result, this will short circuit the 17 volt line to ground and cause fusible resistors R669 and R675 which are in series with T608/pins 8 and 5 to open.

The regulated 17.5Vdc is output to connector G-6/pin 4 and pin 3. Regulated 17.5Vdc is also output to 12 volt regulator IC602/pin 1 through R665 and R664. Regulated standby 12Vdc is output from IC602/pin 3 to feed RY602 and the G-11/pin 1 (RM-8) connector via R685. From G-11/pin 1, standby 12Vdc feeds the 5 volt regulator IC205 on the A-Board, producing standby 5Vdc for the Control IC located on the M-Board.

Standby control IC606 monitors regulator IC602 and the RM-8 standby supply lines for overloads circuit conditions at IC606/pin 2, through voltage divider resistors R672, R673, and overload sense diodes D625 and D627, respectively. If an overload occurs in either the 12 volt regulator or the RM-8 lines, it will cause overload sense diodes D625 or D627 to conduct. In this case the under voltage lockout control feature, within IC606, will lock the PWM pulses output from IC606/pins 8 and 11 OFF until the overload condition is corrected



* NOTATION DIFFERENT FROM SERVICE MANUAL

STANDBY POWER

Troubleshooting

CAUTION: The set's chassis is isolated from the AC line. However, the power supply is NOT fully isolated from the AC line. Therefore, the use of an isolation transformer is essential when servicing the set.

Lethal voltages are present in the primary and secondary circuits of this supply. Therefore, exercise extreme caution when hooking-up any type of test equipment to the set.

When troubleshooting a dead set condition, you must verify the operation of the standby power supply. Below is a list of strategic steps you can take to quickly help you locate the problem area:

1. Check line fuse F601 to ensure that it is not open. If it is, suspect surge protect VDR601, bridge rectifier D633 and power converter switching transistors Q603 and Q614 for PN junction failure. Remember that a simple front-to-back ratio test done with a digital multimeter will show the condition of these components.

2. If Q603 and Q614 are defective, check the damper diodes D607 and D616 for possible PN junction failure.

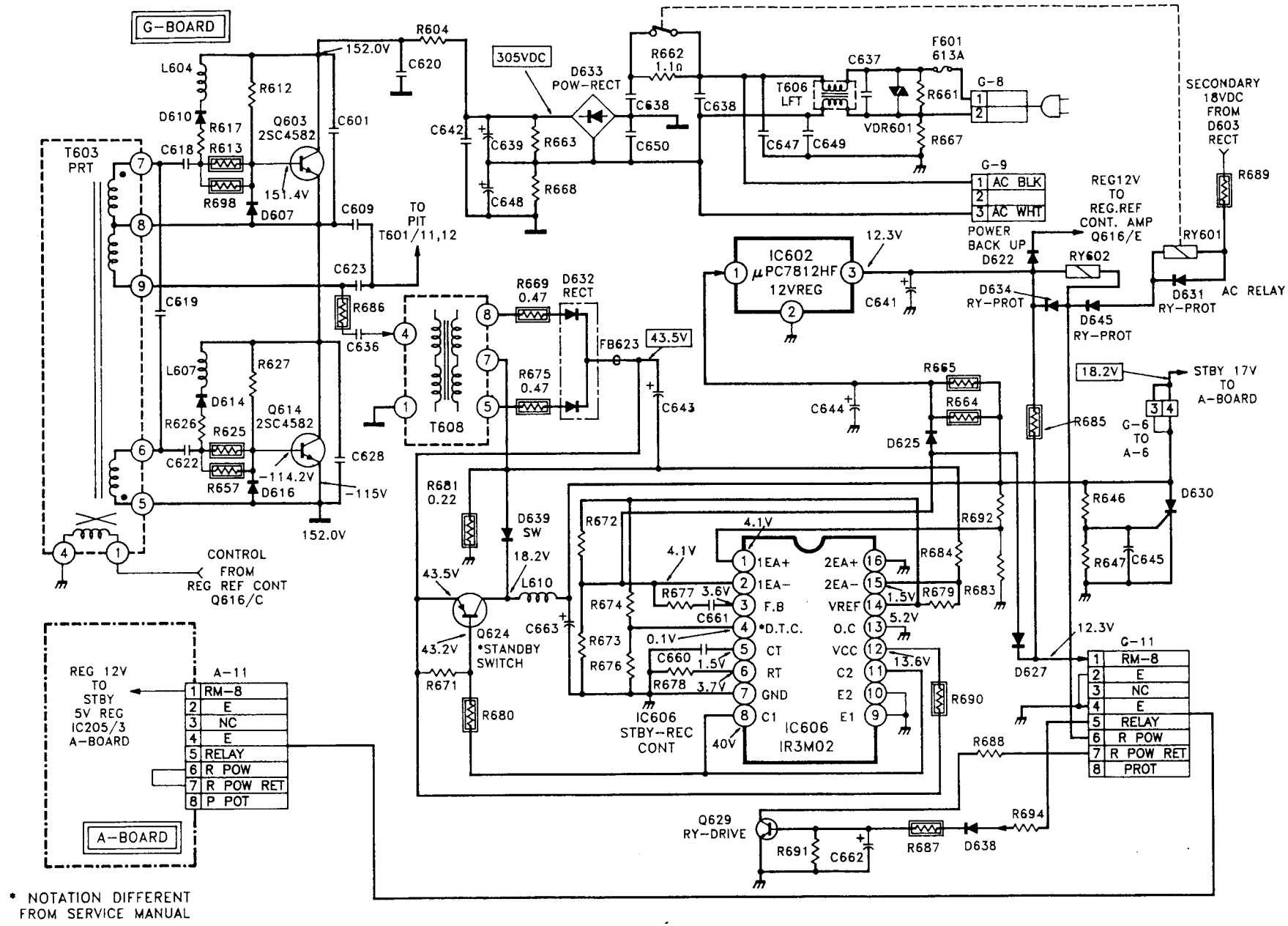
3. If no problem is found, replace the fuse, then connect the set to a variac and slowly raise the input line voltage to 117Vac while observing the fuse and the variac's current meter for any abnormal indications. From the list below, check the normal switching frequency versus input voltage/current response.

AC Input	Switching Frequency	Volts Peak to Peak	Current
40Vac	23.6kHz	117Vp-p	0.1A
60Vac	21.9kHz	171Vp-p	0.125A
80Vac	21.8kHz	220Vp-p	0.150A
100Vac	21.3kHz	276Vp-p	0.25A
120Vac	20.9kHz	331Vp-p	0.35A

4. If okay, and the set will still not respond to power ON, check for regulated 12Vdc at IC602/pin 3 and for regulated 17Vdc at IC602/pin 1. If missing, check for unregulated 43.5Vdc at the emitter of Q624 and for 17Vdc at its collector. If the 43.5Vdc is present but the 17Vdc is missing, suspect Q624, PWM Regulator IC606, or a shorted 17Vdc line. (Refer to the "Standby Pulse Width Modulator (PWM)" troubleshooting section of this manual.)

5. If the 43.5Vdc is missing, check for a 348Vp-p 21kHz waveform at T608/pin 4 (measured with respect to AC ground). If present, suspect T608 for an open winding and the components around the secondary of T608.

6. If all checks okay, but the set will not respond to power ON, then refer to the "Power ON" troubleshooting section of this manual.



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STANDBY POWER

PRT Regulation

Overview

The PRT regulation circuit compensates for AC input line voltage fluctuations and Power Input Transformer (PIT) secondary load variations so that the secondary output voltages from the PIT remain constant. Regulation is done by varying the resonant frequency of the switching regulator circuit and PRT T603. Controlling this frequency will determine the level of the output voltages at the secondary of power input transformer T601.

Operation

As explained, controlling the resonant frequency of the switching converters keeps the output voltages of the power input transformer constant. The resonant frequency of the converter and power regulating transformer is determined by the inductance and capacitance of the circuit components. In the power ON mode, this is between 30kHz to 35kHz. Since the capacitance of the circuit is fixed, only the inductance can be made to vary. This is done in the following manner.

The power regulating transformer is cross-wound. That is, it has a control winding wound at right angles to the main windings. In the diagram, the control windings are connected between T603/pin 1 and pin 4.

The characteristics of the PRT is such, that current flow through the control winding changes the inductance of the PRT. The inductance varies inversely with the current flowing through the control winding. In other words, a current rise through the control winding decreases the inductance of the PRT. As a result, the resonant frequency of the PRT will increase.

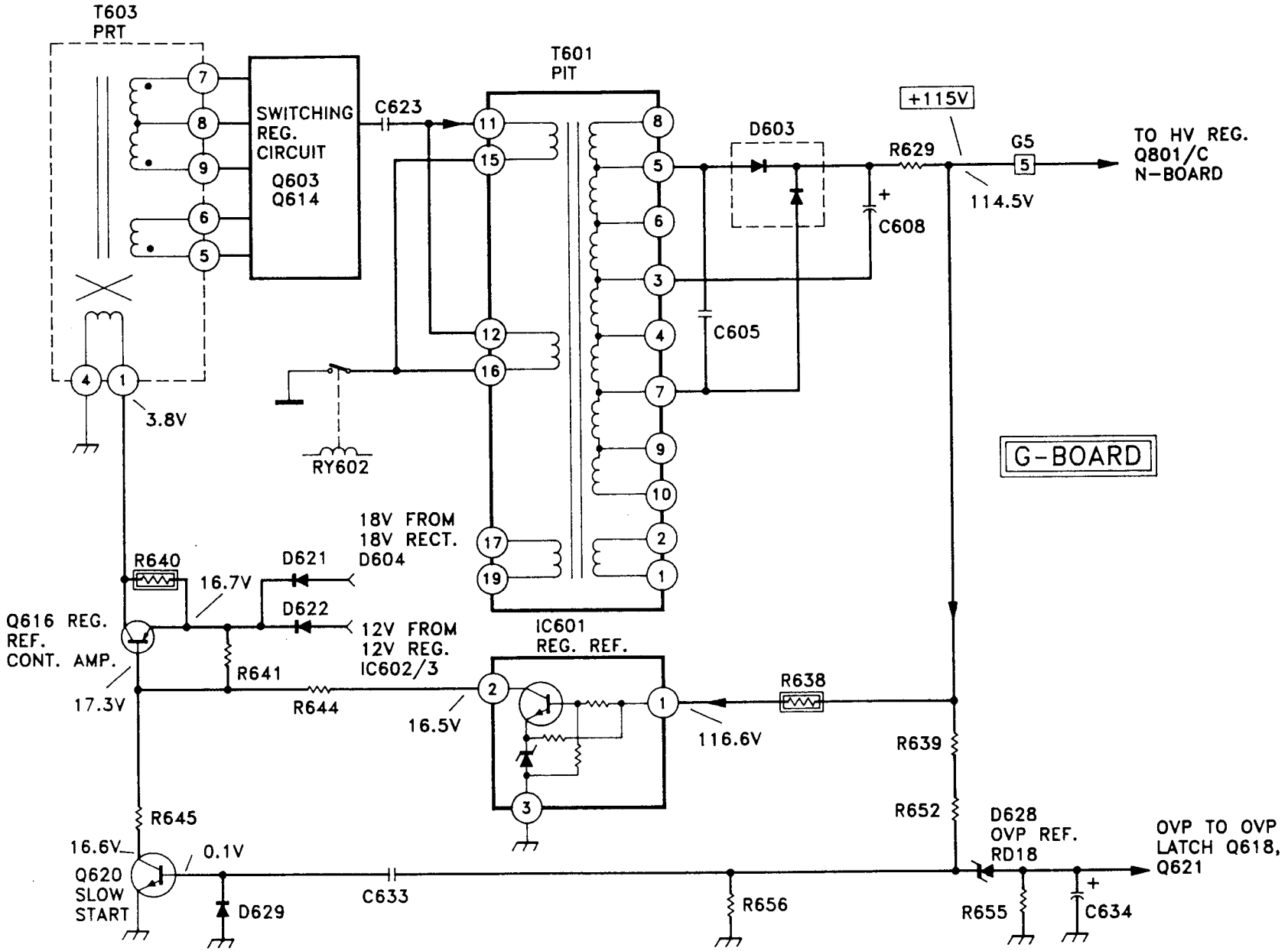
The control winding current is dependent on the conduction of control amp Q616 emitter to collector junction. To regulate, a sample of the rectified +115Vdc from D603 is coupled through R629, R638, IC601/pin 1, IC601/pin 2, R644, to the base of Q616. Any changes in secondary voltage is sensed at the base of Q616.

Q616s conduction varies in inverse proportion to its base voltage. That is, a drop in Q616's base voltage results in a higher collector voltage and collector current. If the secondary +115Vdc voltage increases, then Q616's base voltage becomes less positive, which allows Q616 to conduct harder and the PRT control winding current to increase. This causes more current to flow through the PRT control windings. As a result the PRT's inductance decreases, which raises the resonant frequency of the PRT. Since the PRT's efficiency is higher at the lower end of its 30kHz to 35kHz frequency range, the output power from the PRT decreases as its inductance is lowered.

The +115Vdc is connected to connector G-5/pin 5, N-5/pin 5, L803, L801, and L802 to the High Voltage Regulator Q801 on the N-Board (not shown).

Soft Start

Q620, C633 and R656 comprise a soft start circuit. The soft start circuit reduces the initial secondary load stress placed on the switching circuits as the filter capacitors in the PIT's secondary charge. This circuit delays the rise time of the PIT secondary line voltages by approximately 100ms. The time constant is determined by the resistance of the Q620 base to emitter junction, C633, and R656.



PRT REGULATION

Troubleshooting

Regulation problems fall under two basic categories:
1. Over voltage.

2. Under voltage.

Over voltage problems often can be recognized by the set shutting OFF when main power is turned ON. In this situation, first determine if shutdown stems from over voltage. To verify this condition, check the voltage at the cathode of OVP-REF diode D628 when power is turned ON. If the voltage at the cathode of D628 is greater than 17.8Vdc at turn ON, then check the following:
1. Check for 17.1Vdc at the emitter of Q616 when the set is turned ON. If missing, trace it back to its source. If present, check for 17.3Vdc at the base of Q616 when power is turned ON. If missing, suspect a shorted soft start transistor Q620, IC601 or leakage from C633.

2. Check for 3.8Vdc at the collector of Q616. If missing suspect Q616.

3. Check for 16.5Vdc at REG REF IC601/pin 2 when power is turned ON. If missing check for 114.3Vdc at IC601/pin 1. If missing check R638 and the 115Vdc source. If okay, suspect IC601.

Use the following procedure to verify the integrity of the PRT:
1. Unsolder T603/pin 1 from the circuit.

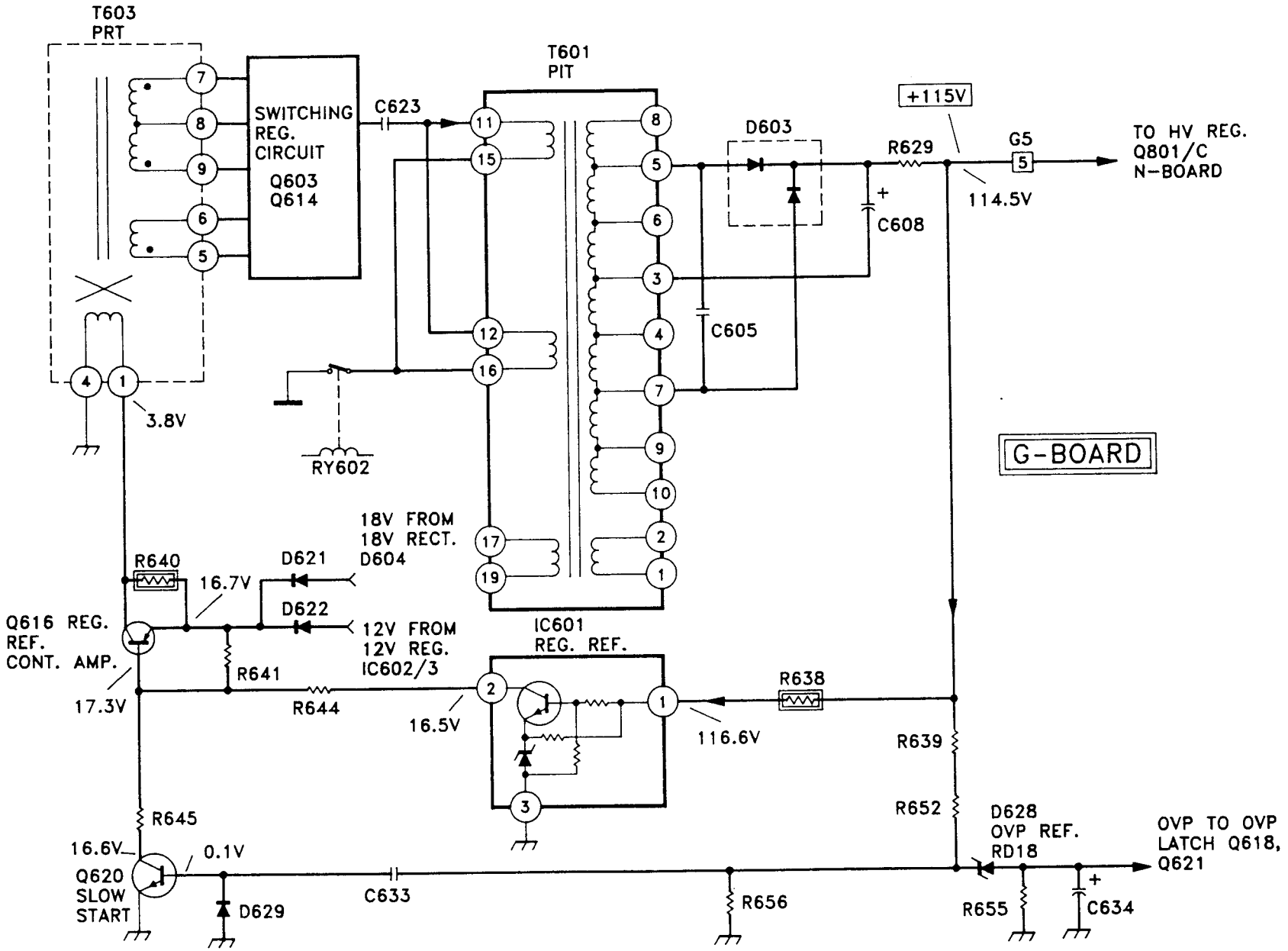
2. Tack solder a 0.47 ohm ¼ watt fusible resistor to T603/pin 1 for safety.

3. Connect the other end of the resistor to a variable DC power supply source and set the input voltage to 4.1Vdc.

4. Connect the unit to an isolated variable AC supply, and set the input voltage to 70Vac.

5. Turn the set ON and quickly turn the variable DC power supply ON. The set should run.

Now, if the DC supply input is varied, a voltage change at the secondary of power input transformer (PIT) T601 will be observed. This confirms PRT integrity and also allows troubleshooting the regulation circuits with the set powered-up to a LOW AC input voltage.



PRT REGULATION

Main Power Supply Shutdown Protect

Overview

The function of the main power supply shutdown circuit is to safeguard the set from over current, over voltage, loss of horizontal deflection, or from loss of one of the set's many regulated B+ supplies. In the event of a malfunction, a protection latch is triggered which cuts off the power supply relay.

Operation

The set's shutdown protection circuit centers around the Over Voltage Protection (OVP) protection latch comprised of Q618 and Q621. To protect the set, this latch operates when a HIGH (0.6Vdc) is sensed at the base of Q621 or a LOW (0Vdc) at the base of Q618. Triggering the latch grounds the RELAY signal which is output from the set's control IC001/pin to the base of Q629. The RELAY signal is applied to the relay drive transistor Q629 through connector A-11/pin 5, G-11/pin 5, R694, D638 and R687.

There are many causes for power supply shutdown. This section covers over current and over voltage protection.

Over Current Protection

A current overload in the secondary of the Power Input Transformer (PIT) will cause a large current to flow through its primary winding. This induces a large voltage in the winding at PIT T601/pin 17 and pin 19. The resulting output voltage is coupled through R666, L611 to T605/pin 4 and pin 3. During normal operation this voltage is 68Vac. When a fault is detected, this voltage will approach 120Vac.

T605 is a three to one ratio step down transformer. It isolates the primary of PIT T601 from the set's chassis ground. Based on the turns ratio, the output from T605 secondary is 24Vac if T605 has 68VAC applied to its primary. From T605/pin 2, the 24Vac is rectified by D626. C632, R651, C631, R654 and R642 provide filtering and voltage dropping. The resulting voltage is coupled through D624 to the base of Q621.

The voltage normally present at the junction of R642 and the cathode of zener diode D624 is about 3.8Vdc. If an overload occur,s the voltage at this junction will exceed the zener diode breakdown voltage of 5.6Vdc. As a result, protection latch Q621 and Q618 turn ON, grounding the relay drive signal output from control IC001/pin 21. The following will then occur:

A. Q629 turns OFF (collector goes HIGH).

B. Relay current path is removed from both relay RY-602 and RY-601.

C. Main Power to the set is removed. Standby power will continue to operate.

The latch will remain energized as long as standby power continues to operate and main control IC001 receives standby 5Vdc. The latch is reset by disconnecting the set from the AC power line.

In addition to secondary current overload detection, the 115Vdc line is also protected from overloads and short circuit conditions via current limiter Q615. This circuit operates whenever current flow through R629 exceeds 1 ampere. As a result, Q615 turns ON (collector goes HIGH), which causes latch Q621 and Q618 to turn ON grounding the RELAY signal output from control IC001/pin 21, and operating the relay.

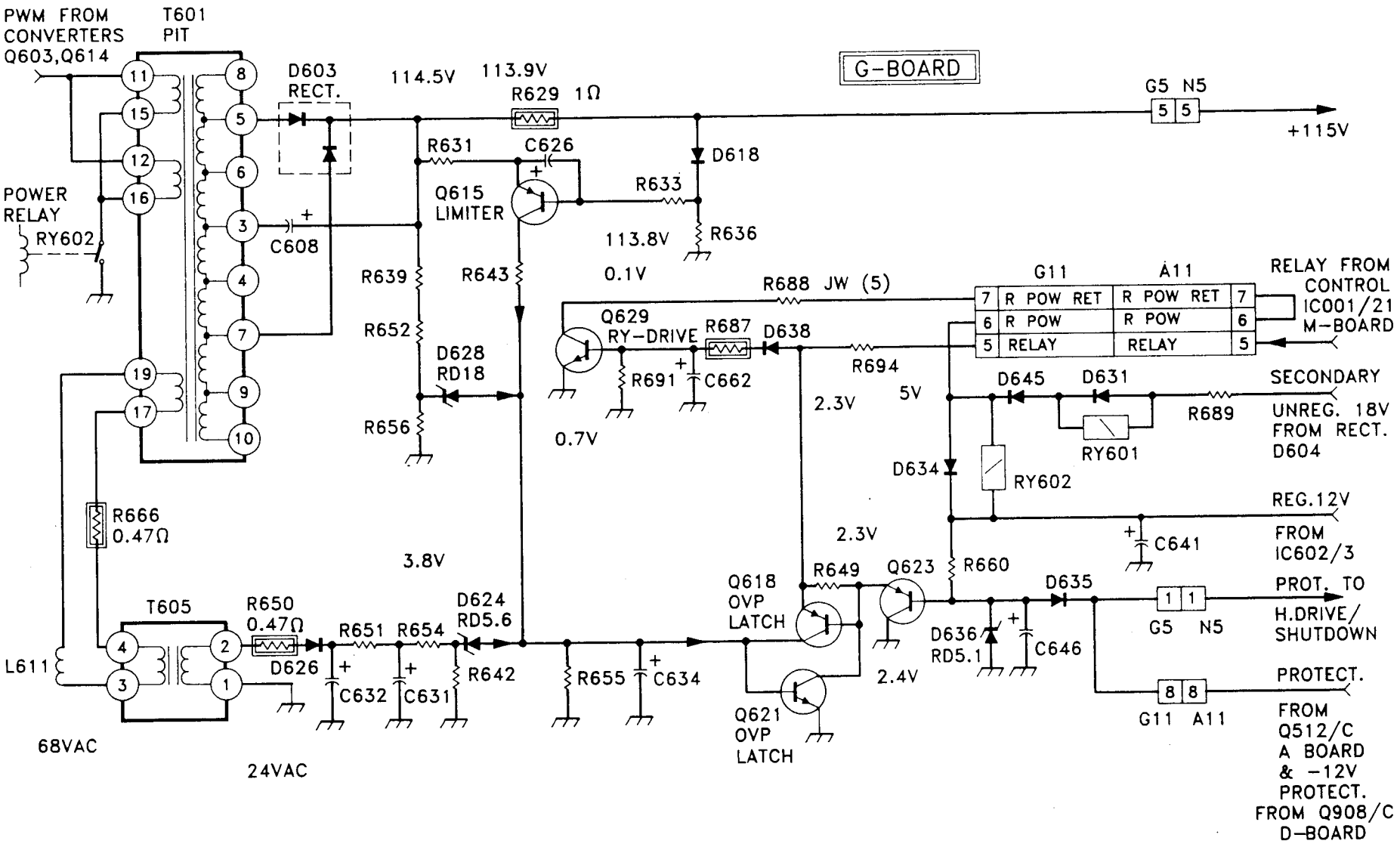
Over Voltage Protection

Over voltage protection works basically the same as over current protection. To sense for an over voltage condition, 115Vdc is sent through voltage divider R639, R652, R656 and zener diode D638, to the base of Q621. The voltage normally present at the junction of R656 and the cathode of D628 is about 17.4Vdc. If an over voltage condition occurs (approximately 121Vdc), the voltage at the cathode of zener diode D628 will exceed the 18V zener voltage. As a result, latch Q621 and Q618 turns ON, grounding the RELAY signal output from control IC001/pin 21. The following then occur:

A. Q629 turns OFF (collector goes HIGH).

B. Relay current path is removed from both relay RY-602 and RY-601.

C. Main Power to the set is removed. Standby power will continue to operate.



MAIN POWER SUPPLY SHUTDOWN PROTECT

The latch circuit also operates in the event horizontal deflection or regulated -12Vdc on the D-Board, which supplies the vertical drive circuits is lost. Horizontal Drive is input to the latch from Horizontal Pulse (H.P.) Protect Q512 on the A-Board through connector, G-11/pin 8, D635, to Q623. Regulated -12Vdc sense, from the D-Board, is also input to the latch, through connectors A-11/pin 8, G-11/pin 8, D635, to Q623.

A loss from either of these inputs will cause the cathode of D635 to become LOW. Q623 turns ON (collector goes LOW), which triggers the latch grounding the RELAY signal output from control IC001/pin 21. Main Power to the set is removed. Standby will continue to operate.

Troubleshooting

When servicing a dead set or "no power ON" conditions" first confirm the operation of the standby power supply. If the standby supply is operating but the secondary voltages are missing, when the set is turned ON, verify proper operation of the power ON circuits. If those circuits check okay, it indicates that the OVP latch is activated.

To determine if the latch has been activated, check the voltage at the emitter of Q618. If it measures 1.2Vdc or less, the latch is operating. To determine which circuit is responsible for activating the latch, check the voltage at the base of Q623. If it measures 0.65Vdc, check for shorts on the regulated B+ string. If it measures 1.4Vdc, check H.P Protection. (Refer to the Protection Shutdown Block diagram of this manual for the respective circuits).

If the voltage at the base of Q623 is OK (2.4V), unplug the set from the AC line and wait at least 15 seconds to allow the filter components in the set to discharge. Re-connect the set to the AC line and turn power ON. Check that the voltage at the cathode of D624 does not exceed 5.6Vdc when turning power ON. If this voltage goes above 5.6Vdc, then check for short circuit conditions in the secondary of the PIT.

If the cathode of D624 does not exceed 5.6Vdc, then unplug the set from the AC line and wait at least 15 second. Re-connect the set to the AC line and turn power ON. Check that the voltage at the cathode of D628 does not exceed 18Vdc when the set is turned ON. If it does, then check PRT Regulation. (Refer to the "PRT Regulation" Troubleshooting section of this manual.

Running the Power Supply Partially Unloaded

Running the power supply partially unloaded will allow you to troubleshoot the regulated B+ PRT secondary stages at a reduced voltage potential.

Caution: The following steps describes how to partially unload the power supply, and temporarily disable the power supply main shutdown protection latch circuit. Therefore, it is important to ensure that circuit shorts are not present in the secondary supply lines of the PRT. Because certain component failures may not actually reveal a direct short, verify the integrity of the high voltage converter output and horizontal deflection output transistors separately, since these are the items most susceptible to short circuit failure. Remember, a simple front to back PN junction test performed with a multimeter will reveal the condition of these components. Then, proceed to the following:

1. Unplug only the following four connectors from the G-Board: G-2; G-4; G-5; G-3. NOTE: Do not unplug connector G-7 (+18Vdc and -18Vdc). The power supply cannot be run fully unloaded without damage to other power supply components.

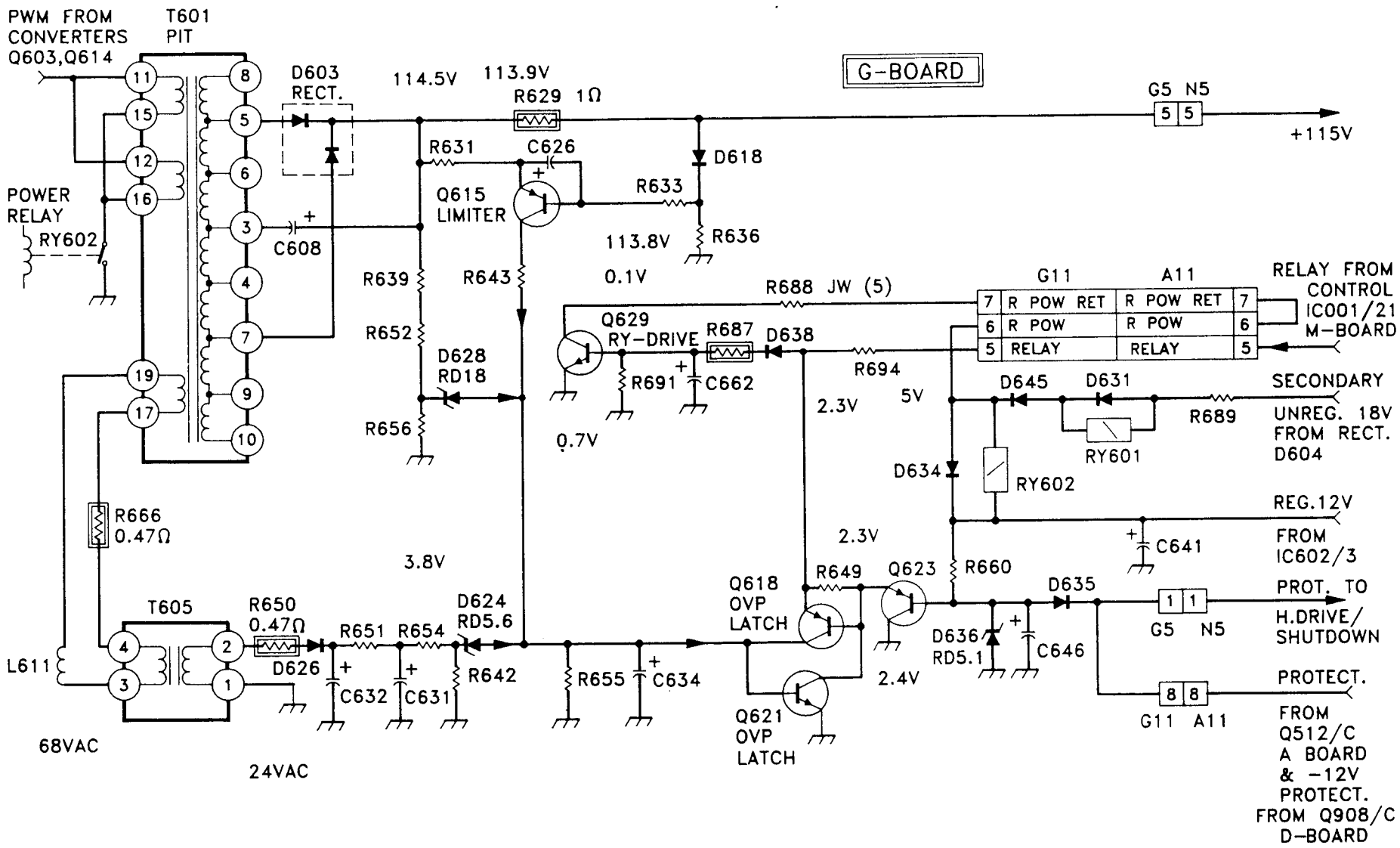
2. Install a jumper wire across the RY-602 power relay contacts. This step defeats the power supply shutdown protection. It supplies power to the PRT section when AC power is applied to the set.

3. Connect the set to a variac and isolation transformer .

4. Set the variac input voltage to minimum and then turn the variac ON.

5. Slowly raise the variac input voltage while monitoring the level of the variac's current meter for abnormal current surges.

   As the variac level is slowly raised, monitor each regulated secondary output voltage. If an abnormally high current reading is detected when raising the variac level, stop immediately and check for short. Do not continue until the problem has been corrected. This method also allows basic troubleshooting on the G-Board to be done at reduced voltage levels.

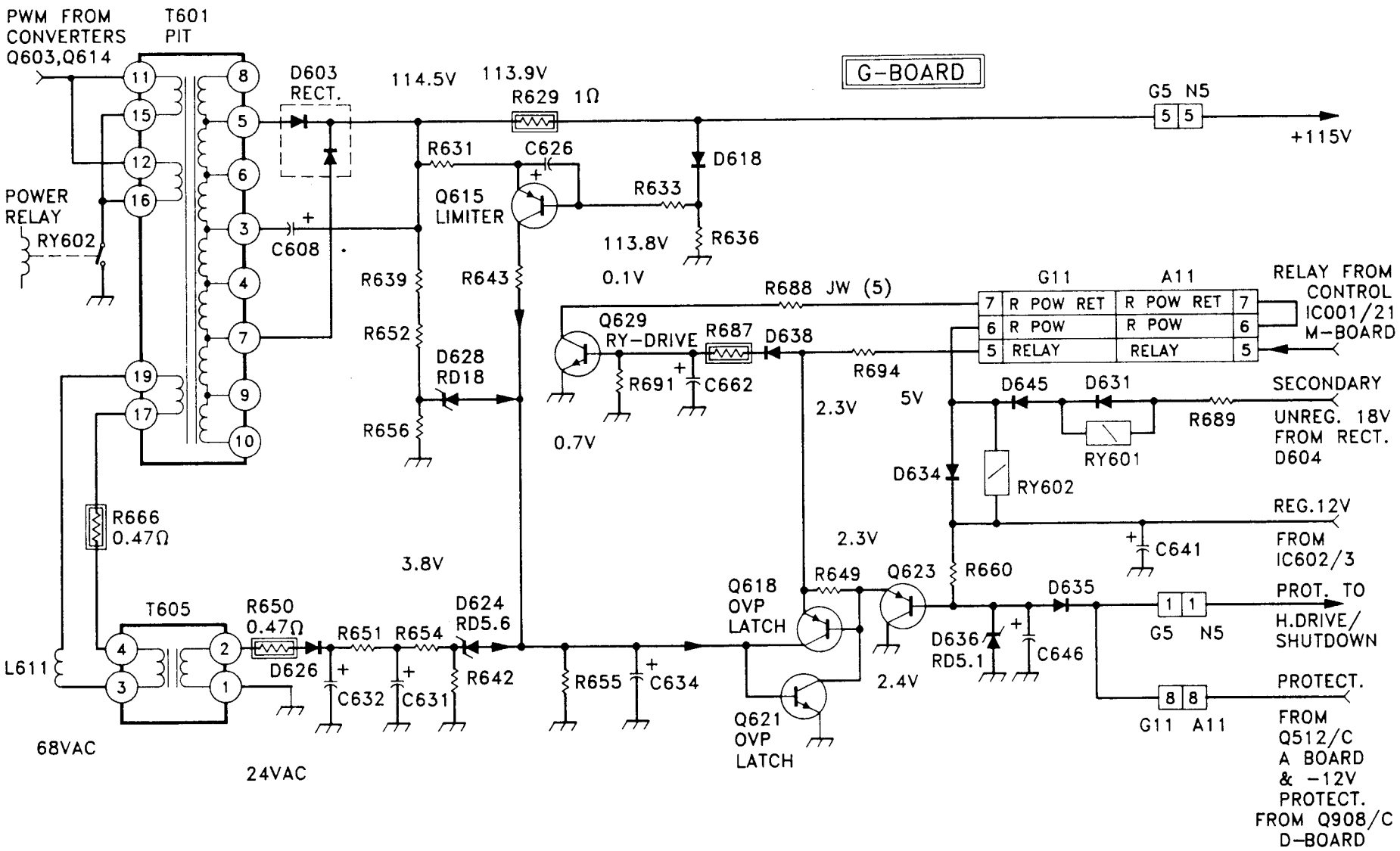


MAIN POWER SUPPLY SHUTDOWN PROTECT

6. If no problems are encountered, in the unloaded state, reconnect each connector previously unplugged in step 1, one plug at a time, and repeat the procedure from step 4.

By carefully observing the variac current meter readings, it is possible to isolate over current problems to a particular connector.

It is also possible to troubleshoot the set's, many stages at reduced voltage levels once all the connectors have been reinstalled. Simply start troubleshooting by following the procedure outlined in step 2 through step 5.



MAIN POWER SUPPLY SHUTDOWN PROTECT

Secondary Power/Regulation

The Power Input Transformer's secondary circuits provide the set with the necessary regulated voltages. The following secondary voltages are produced:

+135Vdc D601, D612 and filter capacitor C610 rectify and filter the +135Vdc for the Horizontal Drive and Velocity Modulation Output stages. Q601, Q602, Q605 and Q606 regulate the rectified 135Vdc line.

Regulator transistors Q601 and Q602 are connected in a Darlington pair configuration. Q601 is a series pass transistor. All of the output current must pass through it to the load. Basically, Q601 acts as a variable resistor. If less output voltage is needed, Q601 is turned ON less (higher resistance). As the resistance goes up more voltage is dropped across its collector to emitter junction and less voltage is seen at the output. The reverse happens if more voltage is needed at the output. The conduction of Q601 is governed solely by the voltage applied to its base from the emitter of Regulator Control Amplifier Q602, thereby controlling the output voltage.

The conduction of Q602 is governed by the voltage applied to its base from the +135Vdc source and voltage divider network comprised of R602, Q606 and R610. Q606 and Q605 are connected as differential amplifiers driving the Darlington circuit. A stable DC reference is applied to the base of Q606, thereby clamping the emitter of Q606 to 4.5Vdc.

To regulate, a sample of the +135Vdc from the emitter of Q601 is fed to the base of Q606 through voltage divider R603, R608 and the +135Vdc adjust resistor RV602. The +135Vdc output voltage is adjusted with RV602. Since the emitter of Q606 is clamped to the DC reference, only its base voltage will vary. If the output voltage increases, Q606 turns ON harder (its collector to emitter resistance becomes less) and the voltage at its collector is reduced. As a result, Q602 and Q601 are turned ON less (higher resistance). As the resistance goes up more voltage is dropped across Regulator Q601 collector to emitter junction and less voltage is seen at the output.

-135Vdc This circuit is similar to the +135Vdc circuit. D611, D602 and filter capacitor C614 rectify and filter the -135Vdc needed by the horizontal output and pincushion output stages. Q611, Q612, Q609 and Q610 regulate the rectified -135Vdc line source. RV-603 is used to adjust the -135Vdc regulated output line voltage.

+18Vdc D604, C606, C607 and L602 rectify and filter the +18Vdc for Relay RY-601 Drive and the +5Vdc, +9Vdc and +12Vdc Regulators on the A-Board (not shown).

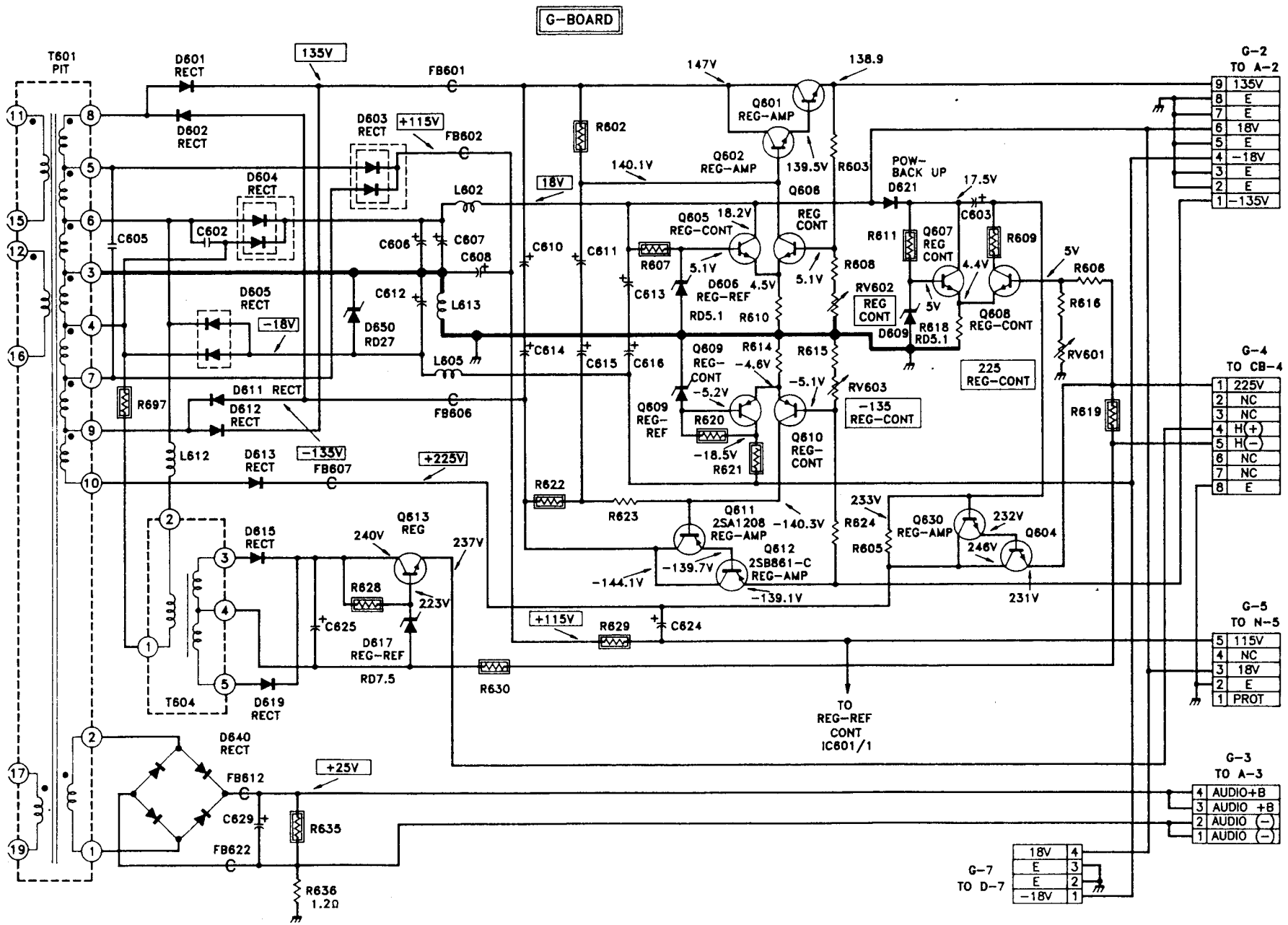
-18Vdc D605, C612, L605 and C616 filter and rectify the -18Vdc for Sub Deflection Output, -5Vdc and -15Vdc Regulators on the D-Board (not shown).

+225Vdc D613 and filter capacitor C624 rectify the +225Vdc for the RGB Drives on the CR, CG, CB-Boards. Q630, Q604, Q607 and Q608 regulate the rectified +225Vdc line source. RV-601 is used to adjust the +225Vdc regulated output line voltage.

+115Vdc D603 and filter capacitor C607 rectify and filter the +115Vdc for the High Voltage Converter stage on the N-Board.

Heater Supply D615 and filter capacitor C625 rectify and filter the +240Vdc for the CRT's filament. The +240Vdc source is connected to the filaments through Regulator Q613 and connector G-4/pin 5 and pin 4. The CRT's filament's voltage is actuality 6Vdc, which is the voltage difference measured between the emitters of Q613 and Q604. The filament voltage potential however, is +240Vdc when measured with respect to chassis ground.

Audio B+ D640 and C629 rectify and filter the +25Vdc for the front audio amplifier on the A-Board.



SECONDARY POWER/REGULATION

Troubleshooting

A loss of secondary voltages will cause the set to shutdown. The cause of shutdown can be caused by a failure in the supply itself or from a circuit driven by a regulated supply section. As a result, troubleshooting for these problems can be quite difficult, as main power to the set will often be immediately cut off.

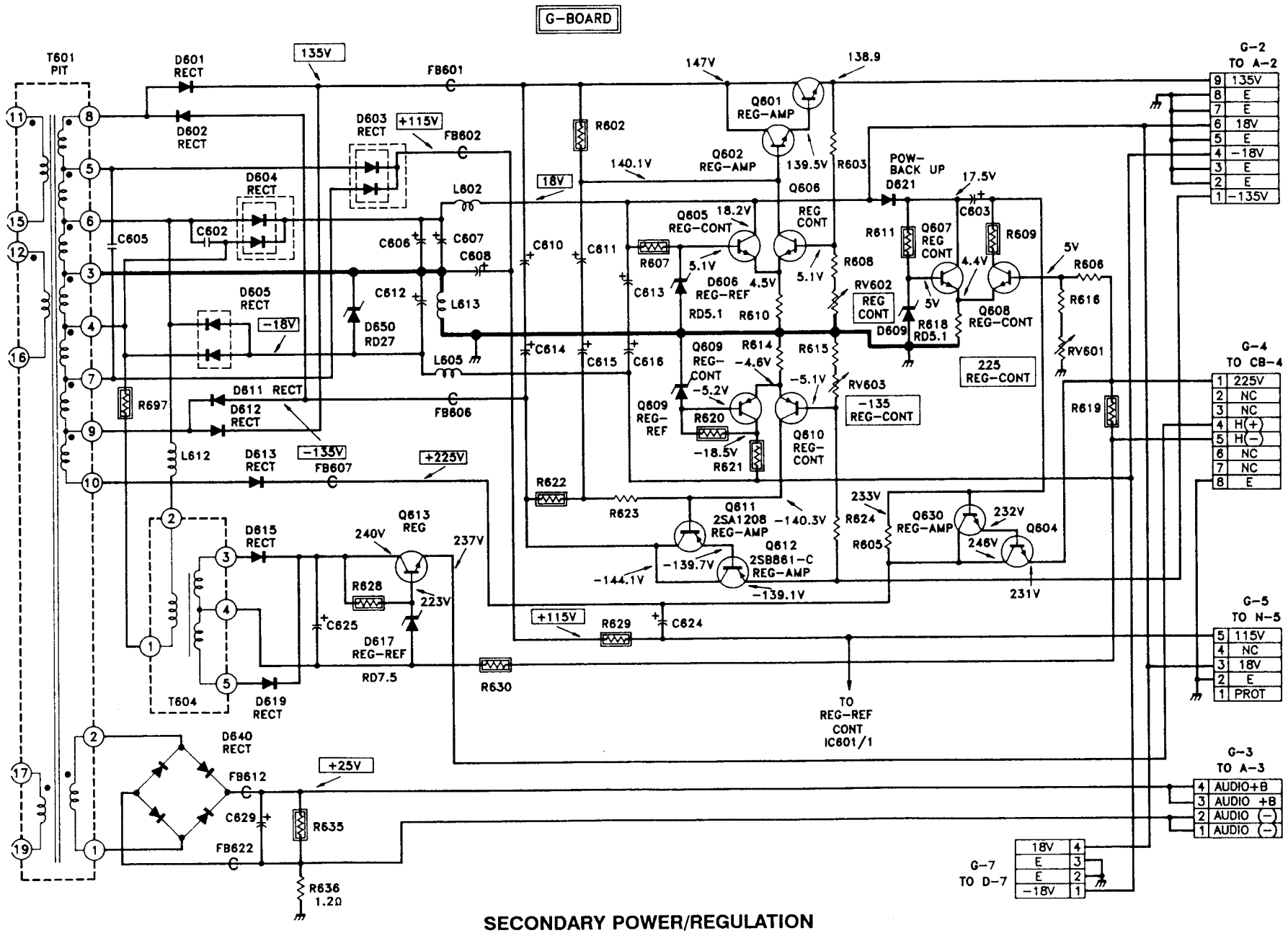
In testing the power supply, the technician should first follow the troubleshooting procedures outlined in the "Main Power Supply Shutdown Protect" section of this manual to determine the cause of shutdown. Those tests should point to the location of the problem. If the cause of shutdown cannot easily be determined, then refer to the resistance chart below to help you isolate the problem area.

Connector	Pin No.	Resistance
G-2	1	>135K
G-2	4	>2K
G-2	6	>3K
G-2	9	124K
G-3	3,4	5.7K
G-4	1	185K
G-5	3	>3K
G-5	5	24K
G-6	3,4	1.3K
G-7	1	>2K
G-7	4	>3K
G-12	1	>3K

Resistance on Power Supply side
(connectors removed)

Connector	Pin No.	Resistance
G-2	1	200k
G-2	4	16.7K
G-2	6	200K
G-2	9	∞
G-3	3,4	2.8K
G-4	1	>2M
G-5	3	53K
G-5	5	>10K
G-6	3,4	N/A
G-7	1	680
G-7	4	850
G-12	1	N/A

Resistance on Connector side



SECONDARY POWER/REGULATION

Tuner Control

Operation

The tuner control section on the M-Board works with Tuner TU101 to tune in broadcast stations. The tuner requires four separate supply voltages to function. These are:

* Regulated +9Vdc is derived from the +18V line on the G-Board, through R243, regulator IC207/pin 5 and pin 2, IC207/pin 3 and 4.

* Regulated +12Vdc is derived from the +18V line on the G-Board, through connectors A-2/pin 6, G-2/pin 6, IC206/pin 1, IC206/pin 3 and L205.

* Regulated +5Vdc is derived from the +18V line on the G-Board, through connectors A-2/pin 6, G-2,pin 6, R528, R529, IC204/pin 3 and IC204/pin 1.

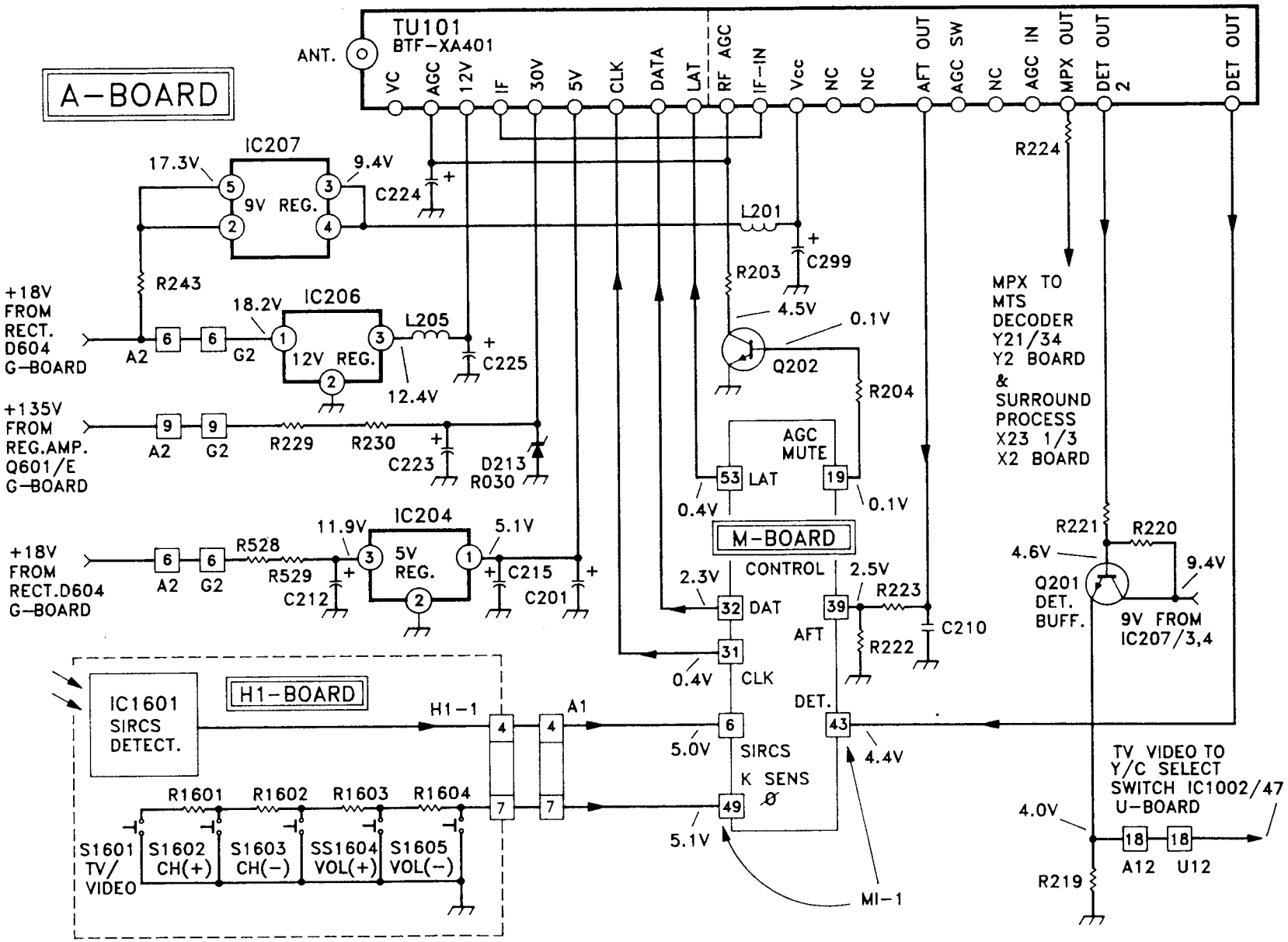
* Regulated 30Vdc is derived from the 135Vdc supply on the G-Board, through connectors A-2/pin 6, G-2/pin 6, series resistors R229, R230, filter capacitor C223 and zener diode D213.

Tuner control IC001, located on the M-Board, selects a station by transferring tuning data to TU101 via M-1/pin 32(DAT). Data transfer from the tuner control is synchronized to the clock signal output from M-1/pin 31(CLK). All data transferred from the tuner control IC is then latched into the tuner section via M-1/pin 33(LAT). Once latched, the data undergoes Digital to Analog (D/A) conversion within TU101. The resulting analog voltage is then used to change the tuner's internal Voltage Control Oscillator (VCO) to the proper station frequency. Tuning Data, Clock and Latch signals are signals are present at all times, even though a channel change function is not being performed.

The tuner's output is then coupled from the IF terminal to the IF-IN terminal of the tuner pack. The gain of the RF signal is controlled by the AGC (Automatic Gain Control) voltage output from the RF-AGC terminal of the tuner pack. Normally, this voltage is 7.2Vdc. The AGC Control provides a HIGH from M-1/pin 19 through R204 to the base of Q202 when a channel change is done. When Q202 turns ON, the RF-AGC line is connected to ground through R203 and Q202. The AGC voltage normally 7.2Vdc drops to 5.2Vdc, which helps the tuning system lock on to the broadcast station faster.

In order for the tuner control to know that it has found an active station it must sense horizontal pulses present from the DET OUT signal coupled to M-1/pin 43. Once horizontal sync pulses are found, tuner control starts to monitor the AFT (Automatic Fine Tuning) voltage coupled from the tuner pack's AFT OUT terminal through R223 to M-1/pin 39. The tuner control converts the AFT voltage to a digital signal. Based on the AFT information, it changes the tuning data so that the tuner remains locked to the broadcast station frequency.

The composite video signal, output from the tuner pack's DET OUT2 pin, is fed through R221, Q201, connectors A-12/pin 18, U-12/pin 18 to the Y/C Select IC002/pin 47 on the U-Board. The Multiplexed Audio signal is coupled from the tuner's MPX OUT terminal to the MTS Decoder on the Y-2 Board through connector Y2-1/pin 34 and to the Surround Sound Processor on the X2-Board through connector X-23-1/pin 3.



TUNER CONTROL

Troubleshooting

The BTF-XA401 Tuner module is a replaceable item. Therefore, troubleshooting to the component level is not necessary. However, when troubleshooting for defects in the tuning system, such as snowy picture, station drift problems or wrong stations, make sure that the required input signals and voltages are present. The following is a list of parameters from a normal operating set, to be used for comparison checks:

Tuner Inputs

5Vdc Supplied from IC204/pin 5 on the A-Board.

12Vdc Supplied by IC206/pin 3 on the A-Board.

9Vdc Supplied by IC207/pin 3 on the A-Board.

30Vdc Supplied by the 135Vdc supply on the G-Board.

DAT 5Vp-p pulses from M-1/pin 32 on the A-Board (Present only when a function key is pressed).

CLK 5Vp-p pulses from M-1/pin 31 on the A-Board (Present only when a function key is pressed)

LAT 5Vp-p pulses from M-1/pin 33 on the A-Board (Present only when a function key is pressed)

ANT RCA jack on the side of the tuner pack.

IF-IN 1Vp-p 45MHz signal(Off the air signal)

AGC 4.2Vdc when locked to an active station. 7.2Vdc when the antenna terminals are shorted together. 5.2Vdc when changing stations.

Tuner Outputs

IF 1Vp-p 45MHz signal(Off the air signal).

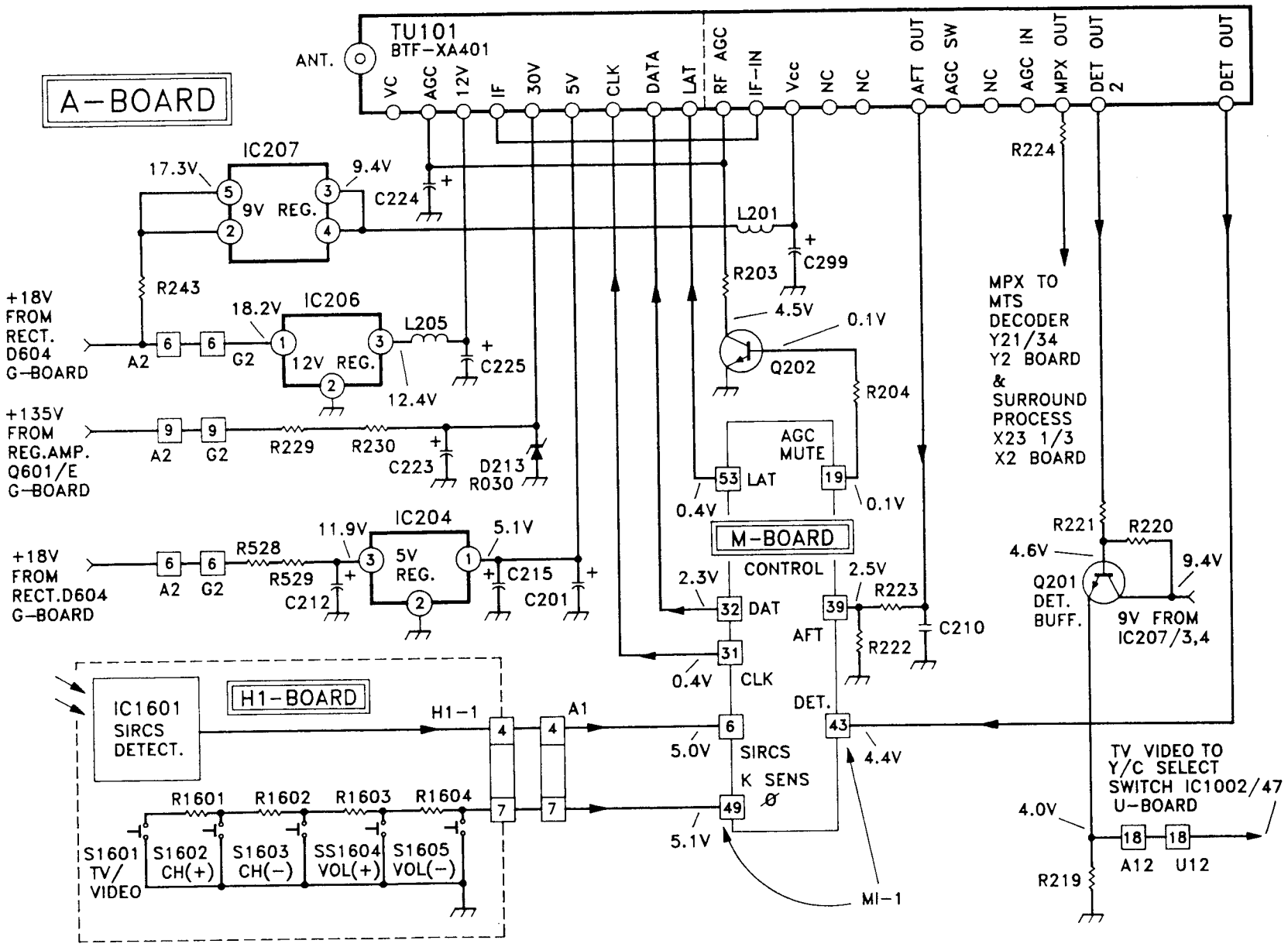
RF AGC 4.2Vdc when locked to an active station. 7.2Vdc when the antenna terminals are shorted together. 5.2Vdc when changing stations.

AFT OUT 2.4Vdc(When locked to an active station).

DET OUT 2.5Vp-p composite video signal.

DET OUT2 2.5Vp-p composite video signal.

VC 1.2Vdc when tuned to channel 2.
4.3Vdc when tuned channel 7.
6.9Vdc when tuned to channel 13.



TUNER CONTROL

Video Signal Process

Operation

The detected video output from the tuner is coupled through connectors A-12/pin 18, U-12/pin 18, the emphasis circuit comprised of Q1023, C1031,R1080, and R1081 to the Y/C Select switch IC1002/pins 17 and 33 (in the case of two tuners inputs) on the U-Board. The external composite video signal, is coupled from the input video jacks on the UT-Board through connectors UT-22/pin 6, pin 12 and pin 13 to the Y/C Select switch IC1002/pins 1, 7 and 13. All switching between these two video sources is done by the control IC001, from key matrix or SIRCS inputs via the I^2C data bus (Not shown).

From Y/C Select IC1002 the internal tuner signal and external video input signals are output at pin 40. These two signals are also available at IC1002/pin 29(SUB V OUT). From IC1002/pin 29, the tuner and external video signals are coupled to the Picture In Picture circuits. We will discussed this circuit later. From IC1002/pin 40 the regular video signal is coupled to a glass type comb filter CM1002/pin 2. This signal is also output to the Monitor Output terminal, located at the rear of the set on the UT-Board, through connectors U-22/pin 4 and UT22/pin 4. The comb filter separates the composite video signal to separate Y (luminance) and C (chroma) signals and outputs these two signals at CM1002/pin 6(Y) and pin 4(C). From the comb filter, the separate Y and C signals are returned to the Y/C Select IC1002/pin 37(Y) and pin 35(C).

S-Video Y and C signals from the S-Video terminal on the UT-Board, are coupled to the Y/C Select IC1002 at pin 3(Y) and at pin 5(C). All switching between these two video sources is done by control IC001 via the I^2C data bus (Not shown). From the Y/C Select IC1002, the Y and C signals are output at pins 43(Y) and 45(C), through connectors U-12/pins 11and 13, A-12/pins 11 and 1, E-1/pins 44 and 46 to Y/C Jungle IC302 on the E1-Board. The Y and C signals output from IC1002/pin 43(Y) and from pin 45(C) are also coupled to the S-Video Monitor Output jack through connectors U-22/pin 28 and pin 26, and UT-22/pin 28 and pin 26.

The Y signal input to the E1-Board/pin 44(Y) is coupled through Y buffers Q312 and Q321, clamp Q301 and Q302, pedestal clamp Q305, gamma correction Q311 and Q314, emphasis Q309 and Q303, connectors E1-26/pin 1 and E-2/pin 1 to Sharpness control IC2304/pin 28 on the E2-Board. The Y signal buffered by Q312 and Q321 is also applied to the Sync Separate circuit consisting of Q317, Q333 and Q335, then input to Y/C Jungle IC302/pin 44(V.Sync) and 45(H.Sync).

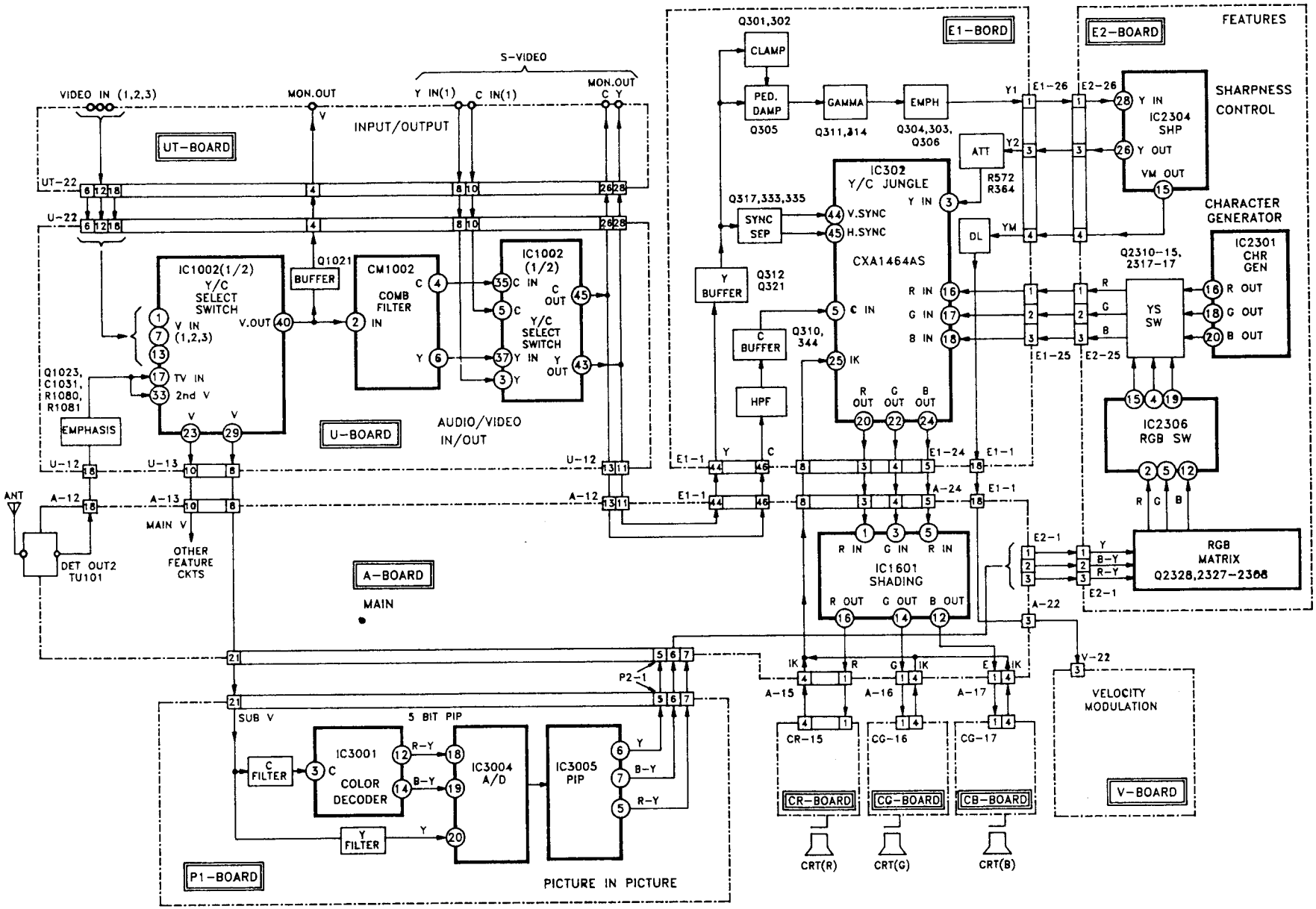
Within the Sharpness control IC, the Y signal undergoes detail enhancement. From the Sharpness control IC the Y signal is output at IC2304/pin 26(Y OUT) and is coupled through connector E2-26/pin 3, E1-26/pin 3 to the Y/C Jungle IC302/pin 3. The Sharpness control IC also outputs a Y signal from IC3204/pin 15 to the Velocity Modulation circuit on the V-Board.

Within the Y/C Jungle IC, the Y and C signals are decoded into separate RGB signals at IC302/pin 20(R), pin 22(G) and pin 24(B). The RGB signals are coupled through connectors E1-24 and A-24 pins 1, 3 and 5 respectively to shading compensation IC 1601/pin 1(R), pin 3(G) and pin 5(B). As will be explained later, the shading compensation IC corrects for the physical tinting effect of the projected image, resulting from the physical mounting positions of the Red and Blue picture tubes. From the Shading compensation, IC the RGB signals are coupled to the Red, Green and Blue CRTs via their respective CR, CG and CB circuit Boards.

As described earlier, the tuner and external video signals are also input to the Picture In Picture (PIP) circuits on the P1-Board. Within the PIP circuits the analog video signal is separated to Y and C components via filters. The chroma signal is input to the Color Decoder IC3001/pin 3(C) and output as separate R-Y and B-Y components from IC3001/pin 12(R-Y) and pin 14(B-Y). From IC3001 the R-Y and B-Y signals are input to the Analog to Digital (A/D) IC3004/pin 18 and pin 19. The Y signal is input to the A/D IC3004/pin 20. Internally these signals are converted to digital signals. From A/D Converter IC3004, the digital picture information is input to the PIP Processor IC3005. Within this IC the digital picture information is reconverted back to analog, and output from IC3005/pin 6(Y), pin 7(B-Y) and pin 5(R-Y).

From the PIP Processor the Y, R-Y and B-Y signals are input to an RGB Matrix on the E2-Board which converts the Y, R-Y and B-Y signals into separate RGB signals. From the Matrix, the RGB signals are input to RGB Switch IC2306. The output of the RGB Switch IC2306, is coupled to the Ys Switch. The Ys Switch also receives inputs from the Menu On Screen Character Generator IC2301. The display of these signals is controlled by the control IC001 (not shown). The output from the Ys Switch is input to the Y/C Jungle IC302/pin 16(R), pin 17(G) and pin 18(B). The display of PIP, On Screen Menu, On Screen Characters (station number,etc.) are superimposed, onto the main picture, internally within the Y/C Jungle. The combined RGB signals are output at Jungle IC/pins 20, 22 and 24.

1 and E-2/pin 1 to Sharpness control IC2304/pin 28 on the E2-Board. The output at Jungle IC/pins 20, 22 and 24.



VIDEO SIGNAL PROCESS

Main Signal/PIP/OSD Switching

Operation

The circuits for Main Video, Picture In Picture (PIP) and On Screen Characters (OSD) signal flow was already discussed. Therefore, only the circuits pertaining to generating the Menu Window display and switching these signals will be discussed.

Control IC001 on the M-Board (1/2) is responsible for generating the On Screen Characters or graphics symbols for station numbers, volume up/down, picture up/down, etc. The display timing for the character information is derived from an internal Voltage Control Oscillator (VCO). The VCO is synchronized to the vertical and horizontal signals which are output from the Y/C Jungle IC302/pins 28 and 39 and input to IC001/pins 68 and 67. The RGB On Screen Character display is output from IC001/pins 16 through 18 and input to the Y/C Jungle IC302/pins 10, 11, and 12. In the jungle IC, the RGB On Screen Character display signal is mixed with the main picture and output to the CRTs via shading compensation IC1601.

Because of internal limitations, control IC001 relies on an external or sub control CPU to generate the Menu On Screen Characters information. This CPU is located on the S-Board. To generate the Menu On Screen Characters, the Sub Control CPU responds to data, to clock and chip select (CS) signals from IC001/pins 47, 49 an 78, at IC3402/pins 22 and 23 and 70. The Sub Control CPU also relies on the vertical sync signal output from the Y/C Jungle IC302/pin 28 and input to the Sub Control CPU at pin 33 to generate characters.

From the Sub Control CPU, data and clock signals are generated and input to Sub Character Generator IC2301/pins 8 and 9 located on the E2-Board. Based on the externally clocked data information, the Sub Character Generator will generate the graphics symbols to display the On Screen Menu Window (background window) and On Screen Menu Character information. The RGB Sub Character signal is output from IC2301/pins 16 through 20 and input to the YS Switch circuit Q2310 through Q2319.

The Sub Character Generator relies on an external Voltage Control Oscillator (VCO) connected to IC2301/pins 13 and 14. The VCO frequency is governed by the voltage output from the Bus D/A IC2307/pin 6. The Menu display information can then be moved horizontally on the screen by shifting the On Screen Display Voltage Control (VCO) oscillator frequency via the I^2C data bus when the unit is in the service mode.

To superimpose the Sub Menu information onto the main picture, the Sub Character Generator outputs a YS digital signal from IC2301/pin 22 to the YS Switch circuit. This allows for either an RGB Menu display or PIP display to be switched to Y/C Jungle IC302/pins 16 through 18. At the same instant, the control IC001 outputs a YS and YM digital signal to the Y/C Jungle IC302/pin 15 and 14. This then allows for the proper mixing between the main picture information and the sub menu display picture information.

To insert the PIP picture information onto the main picture, PIP processor IC3005/pin 9 (not shown) outputs a digital YS signal to the RGB Switch, via Q2337 on the E2-Board. The PIP Processor also outputs this YS signal to the Y/C Jungle IC302/pin 15, on the E1-Board, via the YS switch circuit on the E2-Board. The YS signal allows for the proper mix between the main picture and the PIP picture onto the screen. The PIP digital picture is input to the YS Switch via the RGB Switch and RGB Matrix on the E2-Board from the PIP Processor on the P1-Board.

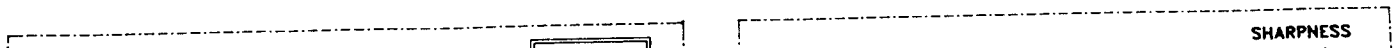
To create the transparent grey menu window effect, the Sub Character Generator outputs a INT digital signal from IC2301/pin 1 to BRT (Brightness) Switch IC2303/pins 1, 3 and 5. The Brightness Switch circuit acts on the level of the RGB background (window) signal, produced by the Sub Character Generator, to reduce the brightness of the background signal thereby generating the transparent window effect.

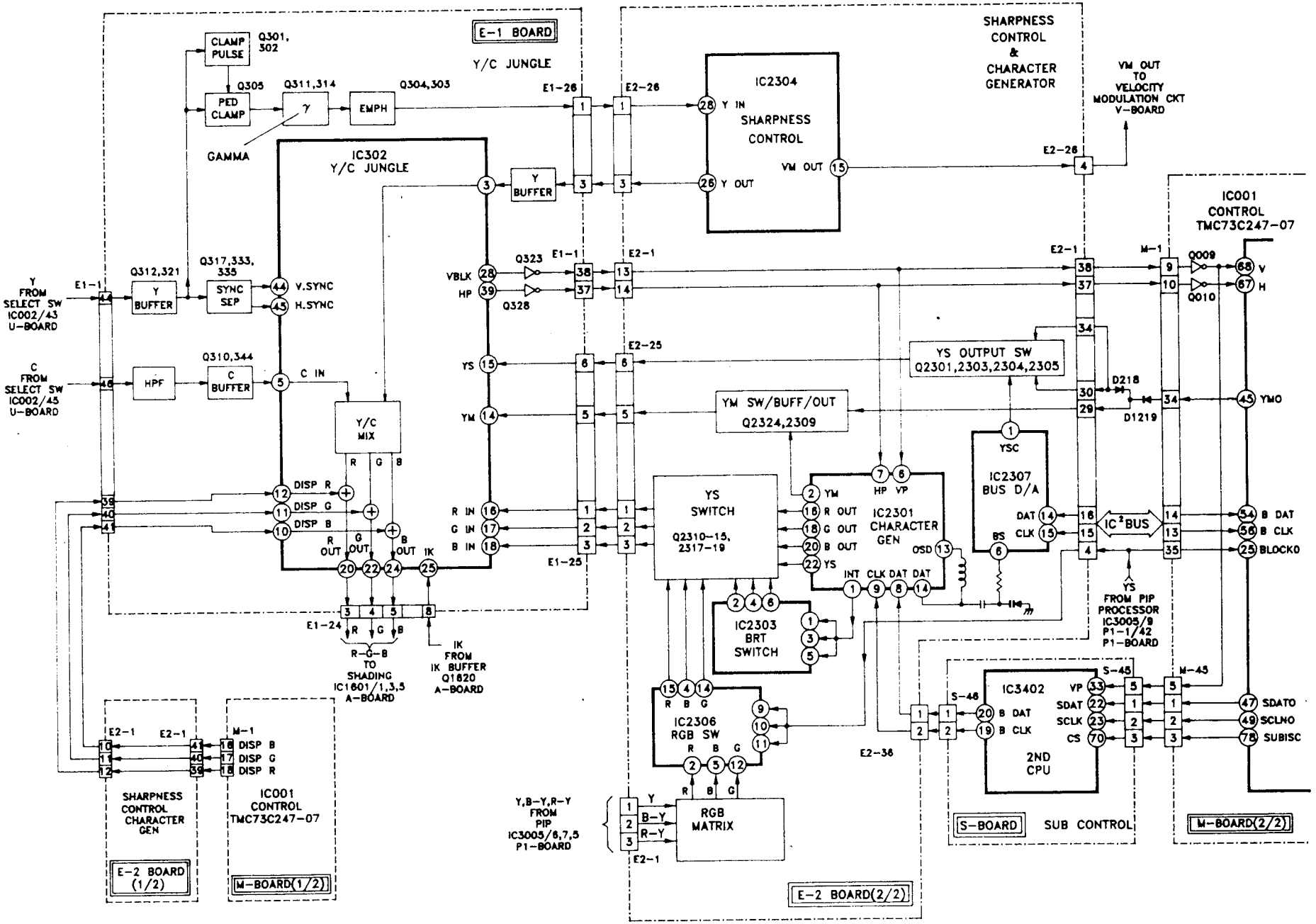
Troubleshooting

When troubleshooting for a missing display character signal, check for RGB output pulses from the appropriate circuit. In the case of station signal information, look for RGB signals output from IC001/pins 16, 17 and 18. If missing, troubleshoot the circuits on the M-Board.

In the case of the PIP picture, look for RGB pulses at connectors E1-25 and E2-25/pins 1, 2 and 3. If missing, check for a YS digital signal at connector E2-1/pin 4. If present, check for PIP RGB video at connector E2-1/pins 1,2 and 3. If missing the problem is in the PIP Processing stage.

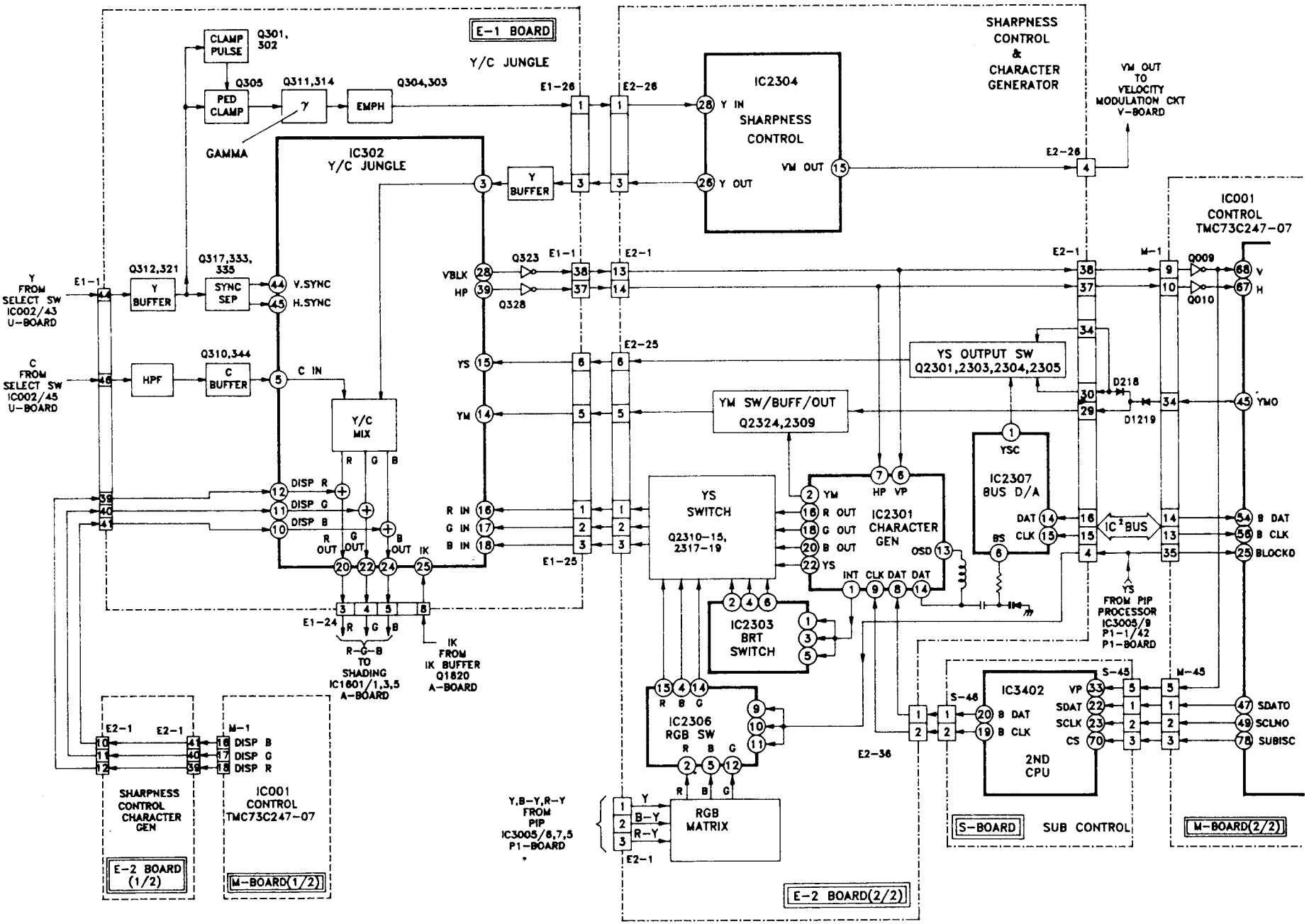
In the case of Sub Character signals, check for data and clock pulses from the Sub Control CPU at connectors S-46 and E2-36/pins 1 and 2. If present, check for YS and YM digital activity at connectors E1-25 and E2-25/pins 6 and





MAIN SIGNAL/PIP/OSD SWITCHING

5. If missing, check for data and clock activity at connector E2-1/pins16 and 15 respectively. If missing, the problem is on the M-Board. If sub control data and clock activity is not present at connectors S-46 and E2-36/pins 1 and 2, check for Data, Clock, CS and VP input signals to the Sub Control CPU. If present, suspect the Sub Control CPU. If missing, troubleshoot the circuits on the M-Board.



MAIN SIGNAL/PIP/OSD SWITCHING

Shading Compensation Block

As illustrated in the diagram, the rear projection system uses three separate color CRTs to project a video picture onto the rear of a flat screen surface. The picture information from each of the CRTs is the same. Each CRT will only project its own color picture information.

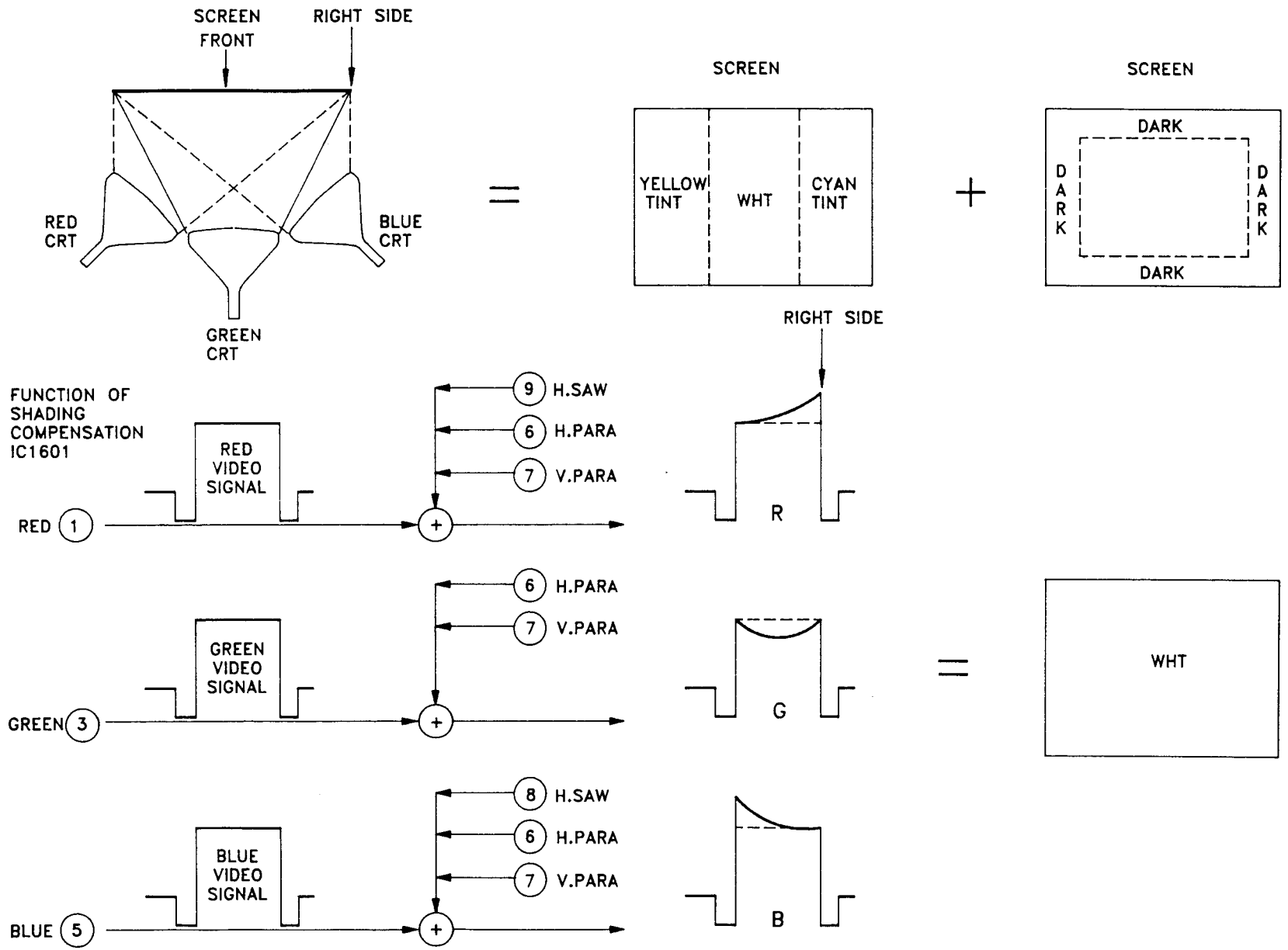
From a physical perspective, only one CRT can project a uniform image onto the screen surface. The Green color CRT is chosen as the primary color imaging device because it contains much of the brightness picture information. Therefore, it is centrally mounted so that its projected image has a direct physical relationship to the image seen on the screen surface.

The red and blue CRTs produce the lesser of the projected image picture brightness information. They are therefore, considered the secondary color imaging devices. The red and blue CRTs are mounted at an angle to each side of the centrally mounted green CRT. This results in uneven picture brightness at the left and right corners of the screen. The effect on the projected image, when all three colors combine on the screen surface, is a yellow tinting on the left side of the screen and a cyanic tint to the right side of the screen.

To correct this condition, a shading compensation circuit is introduced into the RGB video signal paths prior to feeding them to the red, green and blue CRT drives. This circuit boosts the amplitude of the red signal on the right side of the screen and of the blue signal on the left side of the screen. To function, this circuit relies on Horizontal Sawtooth (H.SAW), Horizontal Parabola (H.PARA) and Vertical Parabola (V. PARA) signals from the registration circuits.

To illustrate this circuit's affect, on the video signal, refer to the red video signal concept waveforms in the diagram. As illustrate, the red video signal is amplified so that its right most signal area is boosted in relation to the overall video signal amplitude. This has the effect of increasing the brightness of the video scene in the right corners of the screen. Since the red CRT is mounted where the projected image has to travel a much greater distance to the right side than to the left side of the screen, the brightness is equalized or compensated by the boosted output. The opposite is true in the case of the blue CRT.

Even though the red and blue CRT projected images are compensated for brightness at the edges of the screen, the center areas do not received any compensation The green video image however, focuses much of its picture brightness at the center of the screen due to its physical placement. As a result, the green center areas are much brighter than the projected images from the red and blue CRTs. The green signal is therefore, attenuated at the center portion of the projected image to equalize the overall projected picture brightness.



SHADING COMPENSATION CONCEPT BLOCK

RGB Interface/Shading Compensation

The RGB video signals output from the Y/C Jungle IC302, on the E1-Board, are input to the shading compensation circuit on the A-Board, through connectors E1-24/pin 3, pins 4 and 5, A-24/pin 3, pin 4 and pin 5, R1610, R1611, R1612, Q1601,Q1605 and Q1606 to shading compensation IC1601/pins1, 3 and 5.

To function, the Shading Compensation IC receives horizontal parabola (H.Para), vertical parabola (V.Para), and horizontal sawtooth (H.Saw) inputs from Wave Generator IC902 on the D-Board. The Horizontal Parabola signal is coupled from IC902/pin 18 through connectors D-5/pin 2, A-5/pin 2, voltage divider R1623 and R1620 and through coupling capacitor C1606 to IC1601/pin 6. The Vertical Parabola signal is coupled from IC902/pin 11 through connectors D-5/pin 4, A-5/pin 4, R1622 and through coupling capacitor C1607 to IC1601/pin 7. The Horizontal Sawtooth signal is coupled from IC902/pin 20 through connectors D-5/pin 6, A-5/pin 6, coupling capacitor C1608, R1624 and R1626 to IC1601/pin 8 and pin 9.

The shading compensated RGB signals are output from IC1601/pin 16, pin 14 and pin 12 respectively. From IC1601 they are coupled through buffers Q1603, Q1602, Q1604, R1656, R1657, R1658 to their respective RGB drive circuits via connectors A-15, A-16, A-17 and connectors CR-15, CR-16 and CR-17.

Q1619, and blocking diodes D1610, D1611 and D1612 comprise a peak signal limiting circuit. Q1619's limiting signal voltage is determined by the emitter bias resistor, R1617, and voltage divider network R1618 and R1654. This provides a forward bias to Q1619, which set's up a 6.6Vdc reference at its emitter. If the level of either the red, green or blue signal outputs exceed 7.2Vp-p at either D1610, D1611 or D1612, Q1619 will turn ON. As a result, the output signal will be attenuated by grounding through blocking diodes and Q1619's emitter collector junction.

The shading circuits, within IC1601 can be turned ON or OFF at IC1601/pin 21 by changing the data contained at address location "SHAD" while in the while in the service mode. To adjust shading, IC1601 responds to analog inputs from the Bus Decoder IC506/pin 3 to IC1601/pin 20. When the set is properly adjusted the "SCUT" data will be "16". Normally, the shading circuit has a greater effect, on the RGB output signal when this data is less than "16" and a lesser effect when the data is greater than "16".
service mode. IC1601 responds to analog inputs from bus decoder IC506/pin 2 to IC1601/pin 21 to turn the compensation circuits ON or OFF within the IC. Normally, this data is set to "1", which allows RGB shading compensation. At "0", compensation will be OFF. The shading circuits, internal to IC1601, are adjusted at IC1601/pin 20 by changing the data contained at address "SCUT"

Troubleshooting

Problems associated with the shading compensation IC fall under two categories:

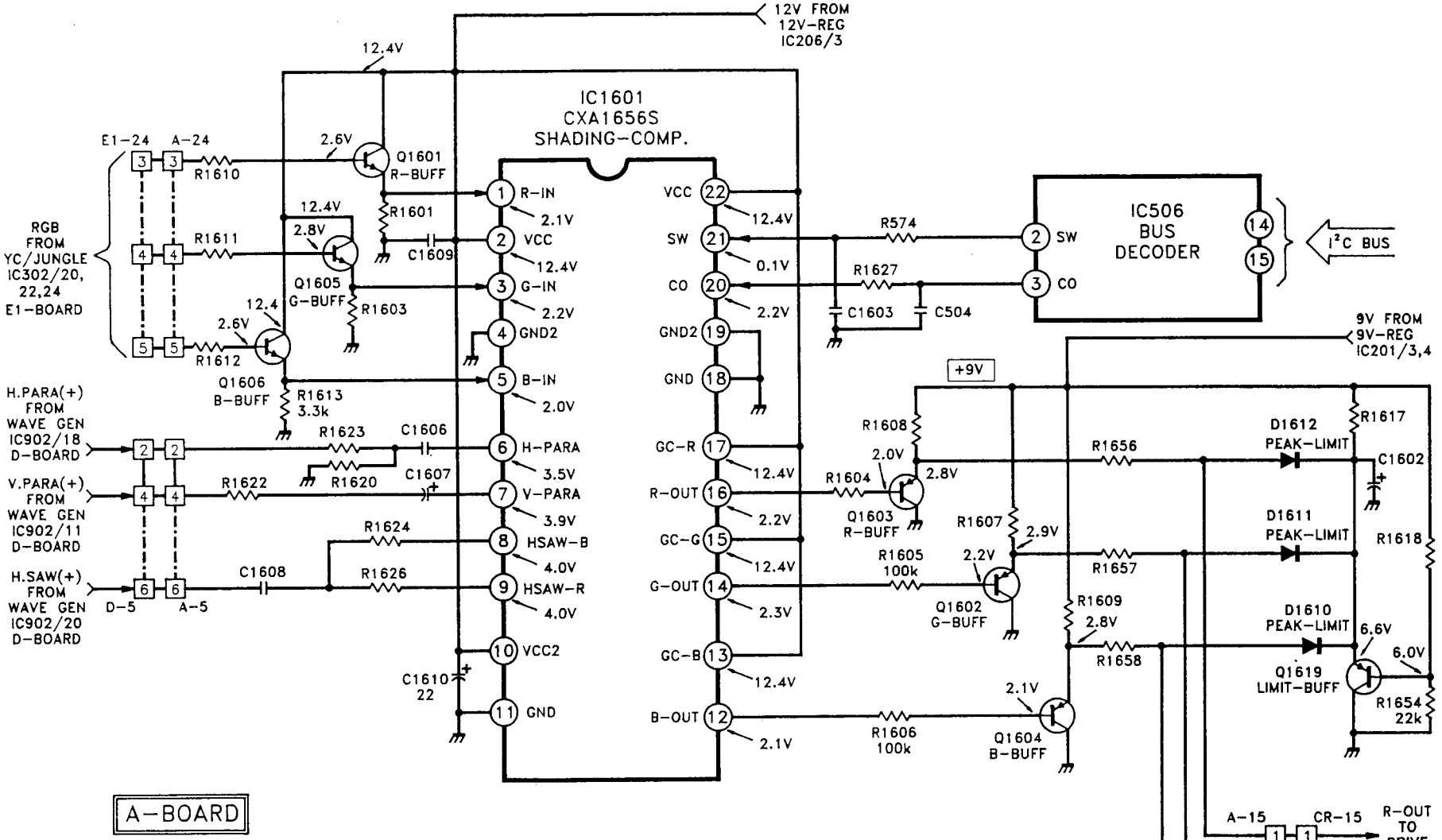
1. Loss of partial or total RGB outputs.

2. Tinting of the projected image.

In the event of a partial loss of RGB outputs, it is only necessary to scope the inputs to IC1601, then the outputs, to determine where the loss has occurred. If the RGB outputs at connectors A-15, A-16, and A-17, are non existent, then suspect a PN junction failure in peak limiter Q1619.

In the event the projected image has a tint, first check address "SHAD", which should be set to "1". If okay, check for 0.1Vdc at IC1601/pin 21 and for 2.2Vdc at IC1601/pin 20. If IC1601/pin 21 is 2Vdc or higher, and address "SHAD" is set to "1", then the problem may be due to a faulty Bus Decoder IC.

The set may also have been misadjusted. In this case, check address "SCUT" for data "16", then for 2Vdc at IC1601/pin 20. If address "SCUT" data is not "16", make the necessary adjustments so as to enter "16". If adjusting does not have an effect on the image, check for a voltage increase at IC1601/pin-20 when the data is set to higher than "16" and for a decrease when less than "16". Also check that the RGB outputs from IC1601/pins 12,14 and 16 change in amplitude. If the voltage at IC1601/pin 20 does not change, suspect Bus Decoder IC506. If the RGB outputs from IC1601/pins 12,14 and 16 do not change, check for registration inputs to IC1601/pins-6, 7, 8 and 9. If any are missing, troubleshoot that circuit. If okay, suspect IC1601.



RGB INTERFACE/SHADING COMPENSATION

RGB CR Drive

Operation

The RGB signals must be amplified and inverted before they can drive the CRT gun.

All picture related adjustments are done through EVRs circuits contained in the Y/C Jungle IC with the remote control unit while the set is in the service mode. Focus and screen control adjustments are located on the focus block assembly.

The red, green and blue drive circuits use similar amplifiers. Therefore, only the operation of the red drive circuit will be described.

The red video signal from shading compensation IC1601/pin 16 is coupled through buffer Q1603, connector A-15 and CR-15 pins-1, and to the base of drive transistor Q702. The emitter of Q702 is tied to voltage reference Q701 through R719, R723, RV701.

NOTE: RV701 is actually a fixed resistor. Therefore, the emitter of Q702 remains clamped to the Q701 emitter reference level.

The video signal is amplified and inverted by Q702, then dc coupled to the emitter of video amplifier Q703. Q703 buffers the video signal. From Q703, the video signal is output from its collector and dc coupled to the base of video amplifier Q704. Q704 is a video buffer. From Q704, the video signal is dc coupled through D703, D702, R706 and R705and L704 to CRT701/pin 10.

The video signal contains a special IK reference pulse in the vertical blanking area. This IK reference pulse is used to measured the cathode current of the CRT during the vertical blanking interval. (Refer to the "Color Television Troubleshooting the ANU-2 Chassis" CTV-18 Course for more on this topic).

The IK reference signal allows the CRT to conduct heavily. The cathode current is sensed at the base of IK Detect Q706. As a result, Q706 turns ON. When Q706 turns ON, current flows from ground (via the CRT bracket) through D707, R712, and Q706 collector to emitter junction, R706, R705, L704 and CRT701/pin 10, to the cathode of the picture tube. The current flow through Q706 causes a voltage drop across R712 and D707. This voltage is dc coupled through R715, connectors CR-15 and A-15 pins-4, voltage divider R1630 and R1601, to the base of IK Buffer Q1620. IK voltage from the green and blue CRTs are also input to the base of Q1620 through their respective circuit inputs. The IK signal is buffered by Q1620 and coupled from its emitter through connectors A-24 and E-24 pins-8 to the Y/C Jungle IC302/pin 25.

NOTE: The IK reference voltage is important to the operation of the video circuits within the Y/C Jungle IC. The Y/C Jungle IC must sense the three reference pulses from the CRTs, returned to IC302/pin 25. If a reference pulse is lost the Y/C Jungle will mute the output video signal by cutting all RGB outputs to the CRTs.

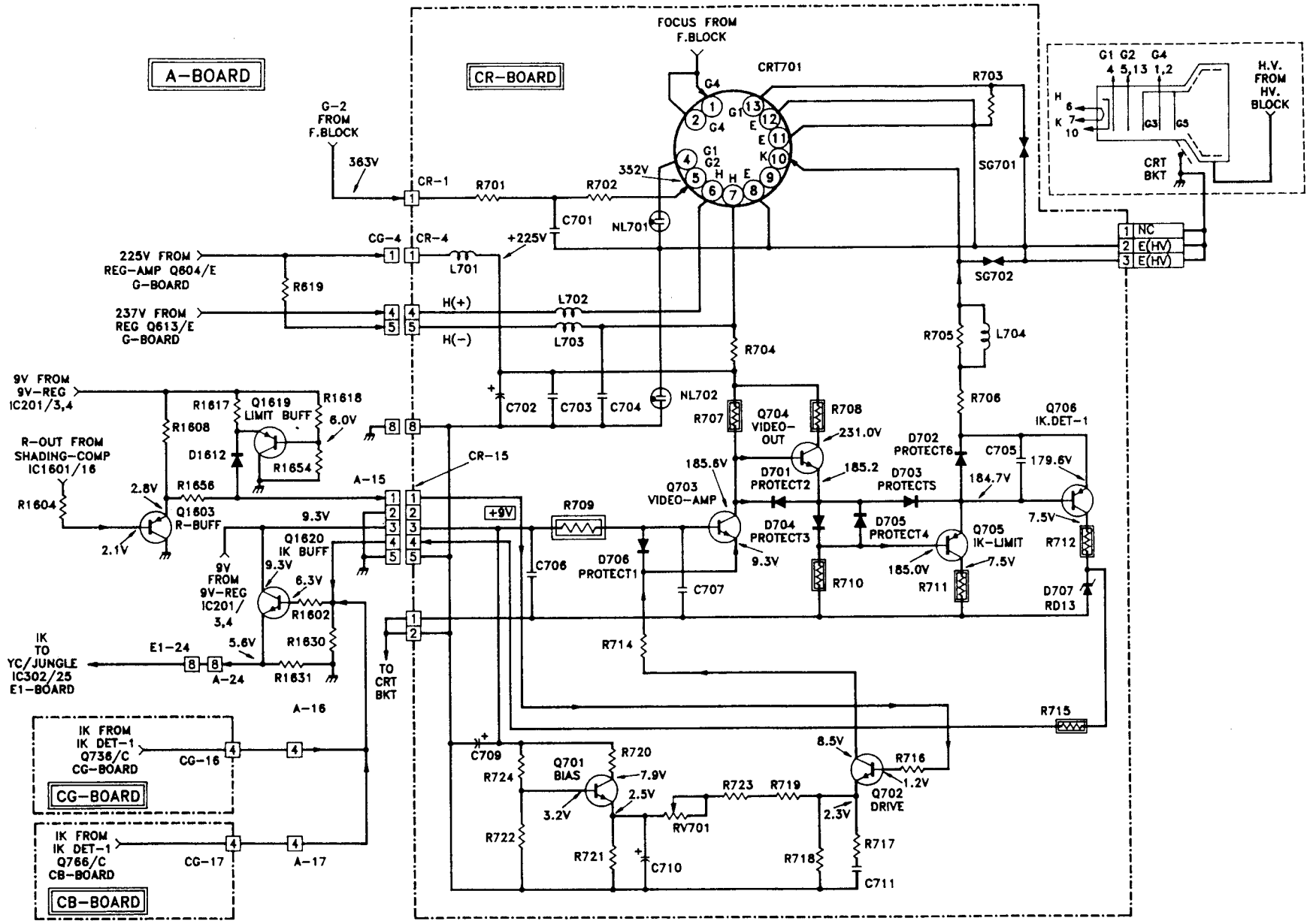
D704, D705 and IK Limiter Q705 comprise a peak signal limiting circuit. Q705 is normally reverse biased by D703 and D704, and therefore, it is OFF. Excessively large video signals, negative going, which exceed the 185Vdc bias at Q705 base, will forward bias the base via D705, causing Q705 to conduct and shunt (bypass) the video signal from collector to ground.

Troubleshooting

The symptom of a faulty RGB drive section is a color tint throughout the screen. Note, that this does not necessarily signify a failed RGB color section, as it is also possible to get tinting due to a mis-adjustment of a drive or background color. A neutral shade of grey or monochrome raster is a good pattern for troubleshooting or adjusting the white balance. Always refer to the service literature of the set when doing grey scale adjustments.

The amplifier stages in the CRT drive boards are dc coupled. Therefore, a problem with one stage will affect all other stages as well. If the voltages don't measure as indicated, suspect the transistors and diodes for PN junction failure. A front-to-back ratio test done with a digital multimeter will often show the condition of these components. Remember, that at times, a transistor or diode may check good, but will break down when it operates "in circuit". In such situations, testing the individual components with a semiconductor curve tracer may be the only way to reveal the condition of these components.

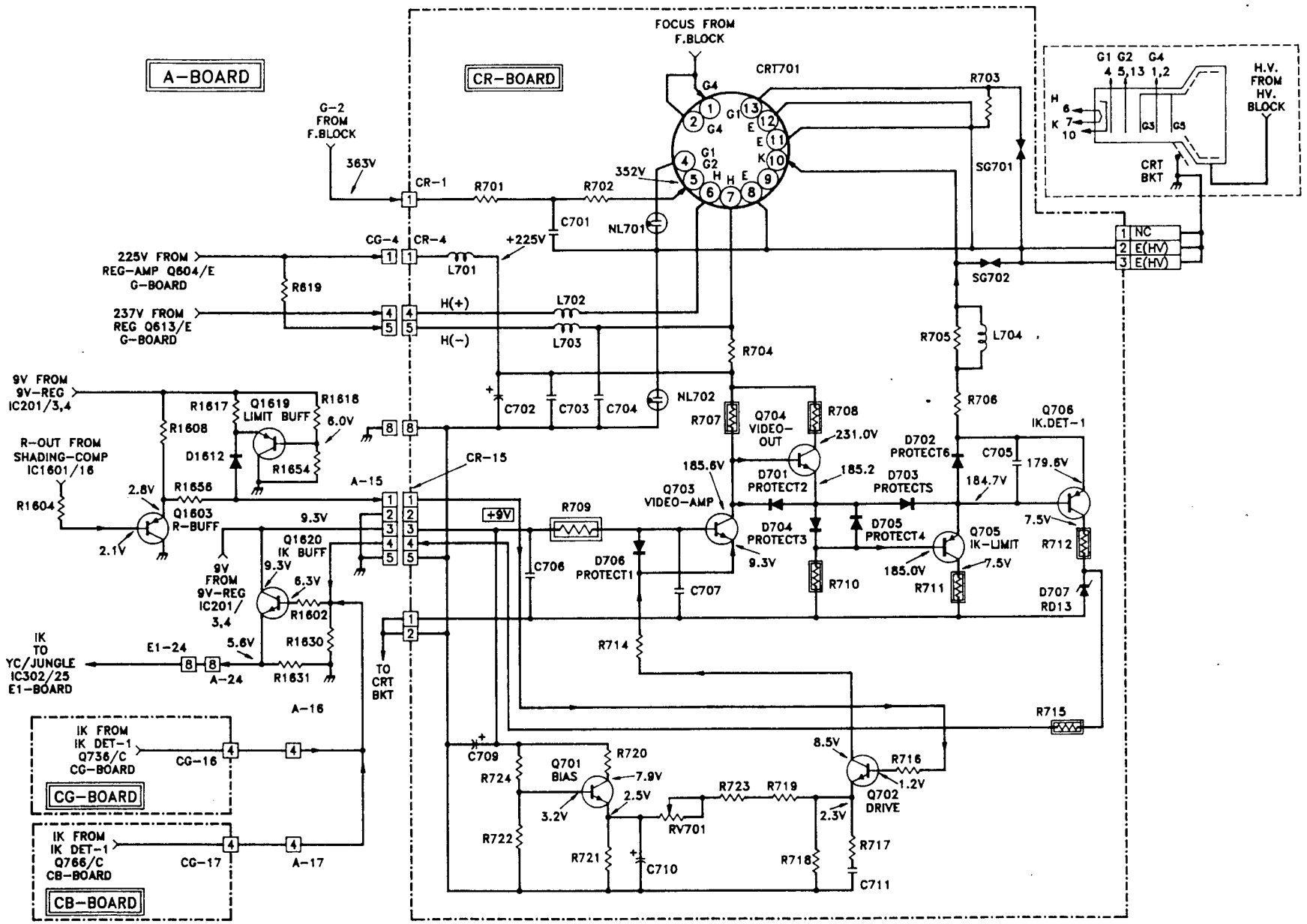
If the problem is a lack of raster, check if the filaments are lit. If not, check for 237Vdc at CR701/pin 6. If okay, suspect the filaments for opens.


A-BOARD
CR-BOARD
FOCUS FROM F.BLOCK
CRT701
G-2 FROM F.BLOCK
363V
352V
CR-1
R701
R702
C701
NL701
R703
SG701
SG702
H.V. FROM HV. BLOCK
CRT BKT
G1 G2 G4
4 5,13 1,2
G3
G5
1 NC
2 E(HV)
3 E(HV)
CG-4
CR-4
+225V
L701
225V FROM REG-AMP Q604/E G-BOARD
R619
237V FROM REG Q613/E G-BOARD
H(+)
H(-)
L702
L703
R704
R705
L704
R706
9V FROM 9V-REG IC201/3,4
R1617
Q1619 LIMIT BUFF
R1618
6.0V
R1608
D1612
R1654
R-OUT FROM SHADING-COMP IC1601/16
R1604
2.8V
R1656
Q1603 R-BUFF
2.1V
9.3V
A-15
CR-15
C702
C703
C704
NL702
R707
Q704 VIDEO-OUT
R708
231.0V
185.6V
185.2
Q703 VIDEO-AMP
D701 PROTECT2
D703 PROTECTS
D702 PROTECT6
C705
179.6V
184.7V
Q706 IK.DET-1
7.5V
+9V
R709
D704 PROTECT3
D705 PROTECT4
Q705 IK-LIMIT
R712
185.0V
7.5V
R711
R710
D707 RD13
C706
D706 PROTECT1
C707
9.3V
9V FROM 9V-REG IC201/ 3,4
Q1620 IK BUFF
9.3V
6.3V
R1602
R1630
5.6V
E1-24
A-24
R1631
IK TO YC/JUNGLE IC302/25 E1-BOARD
TO CRT BKT
A-16
R714
R715
IK FROM IK DET-1 Q736/C CG-BOARD
CG-16
CG-BOARD
IK FROM IK DET-1 Q766/C CB-BOARD
CG-17
A-17
CB-BOARD
C709
R724
Q701 BIAS
R720
7.9V
2.5V
3.2V
RV701
R723
R719
8.5V
R716
1.2V
Q702 DRIVE
2.3V
R722
R721
C710
R718
R717
C711

RGB CR DRIVE

If okay, check for the presence of 1Vp-p IK pulses at the emitter of Q1620 and for 2Vp-p pulses at CR15/pin 1. Synchronize the oscilloscope to the vertical scan in order to view the IK pulses. If any pulses are missing, troubleshoot that circuit. If the pulses are present at the C-Board input stage but missing at the emitter of Q705, suspect the CRT.

If the problem is poor focus, check CRT701/pin 5 for 352Vdc. If missing, check at CR1/pin 1 for 363Vdc. If missing troubleshoot back to the focus block. If okay, check the resistors leading to CRT701/pin 5. If okay, suspect the CRT.


A-BOARD
CR-BOARD
FOCUS FROM F.BLOCK
CRT701
G-2 FROM F.BLOCK
363V
352V
CR-1
R701
R702
C701
NL701
+225V
225V FROM REG-AMP Q604/E G-BOARD
CG-4
CR-4
L701
R619
237V FROM REG Q613/E G-BOARD
H(+)
H(-)
L702
L703
R703
SG701
SG702
G1 G2 G4
4 5,13 1,2
H.V. FROM HV. BLOCK
CRT BKT
1 NC
2 E(HV)
3 E(HV)
R704
R705
L704
R706
9V FROM 9V-REG IC201/3,4
R1617
Q1619 LIMIT BUFF
R1618
6.0V
R1608
D1612
R1654
R-OUT FROM SHADING-COMP IC1601/16
R1604
2.8V
R1656
Q1603 R-BUFF
2.1V
A-15
CR-15
C702
C703
C704
NL702
R707
Q704 VIDEO-OUT
R708
231.0V
185.6V
D701 PROTECT2
185.2
D703 PROTECT5
184.7V
D702 PROTECT6
C705
179.6V
Q706 IK.DET-1
7.5V
Q703 VIDEO-AMP
9.3V
+9V
R709
D704 PROTECT3
D705 PROTECT4
Q705 IK-LIMIT
R712
185.0V
7.5V
R711
R710
D707 RD13
C706
D706 PROTECT1
C707
9V FROM 9V-REG IC201/ 3,4
Q1620 IK BUFF
9.3V
6.3V
R1602
R1630
5.6V
IK TO YC/JUNGLE IC302/25 E1-BOARD
E1-24
A-24
R1631
A-16
TO CRT BKT
R714
R715
IK FROM IK DET-1 Q736/C CG-BOARD
CG-16
CG-BOARD
IK FROM IK DET-1 Q766/C CB-BOARD
CG-17
A-17
CB-BOARD
C709
Q701 BIAS
R720
7.9V
R724
2.5V
3.2V
R722
R721
C710
RV701
R723
R719
8.5V
R716
1.2V
Q702 DRIVE
2.3V
R718
R717
C711

RGB CR DRIVE

Vertical Drive

Overview

The vertical drive circuit provides the necessary 60Hz sawtooth signal to the red, green and blue vertical deflection output stages. The vertical drive circuits also provide the vertical size, linearity, centering and parabola offset corrections to the vertical drive signal.

Operation

The operation for the red and blue vertical drive circuits are the same. Therefore, only the circuits pertaining to the red and green vertical drive stage will be discussed. The vertical blanking signal (V.BLK) is coupled through connectors A-14, A-24 and D-14/pins-1 to wave generator IC902/pin 5. The wave generator produces positive sawtooth signals from IC902/pin 9(+V.SAW), negative sawtooth signals from IC9023/pin 10(-V.SAW) and the positive vertical parabola signals from IC902/pin 11(+V.SAW) in order to drive the vertical deflection stage. The vertical parabola signal, from IC902/pin 11, is inverted by 180 degrees by IC901, producing the negative parabola (-V.PARA) signals.

From IC902, the +V.SAW and -V.SAW signals are connected to opposite ends of vertical size control RV910. The resulting V.SAW signal from the wiper terminal of RV910 is sent through R914 and applied to IC1710/pin 6. The adjustment of this control has the effect of stretching the overall height of the picture.

The V.SAW signal is also coupled through R906 to vertical centering control RV904. The centering control, in turn, is connected to both the regulated +5Vdc and -5Vdc line voltage sources. This provides an adjustable dc offset to the V.SAW signal. This allows the picture to be shifted up and down on the screen

The Bus Decoder from IC506/pin 7 (not show) also applies a DC offset through R1817, to the V.SAW signal. This also centers the picture. Normally, this circuit applies an offset voltage to the V.SAW signal when performing color registration adjustments via the user remote control unit. Therefore, this circuit must be electrically set to its center voltage range when doing the mechanical registration adjustments.

The V.SAW signal is also coupled through R926 to linearity control RV917. The adjustment corrects for the asymmetry of the picture at the top and bottom of the screen. RV905 is the centering adjustment control for the green vertical drive circuits. R1761 and R1764 couples the V.SAW correction signals from the red and blue circuits to the green vertical deflection stage. As a result, the V.SAW, red and blue signals combine to form the green V.SAW output signal.

Troubleshooting

Symptoms of vertical drive problems fall under the following categories:

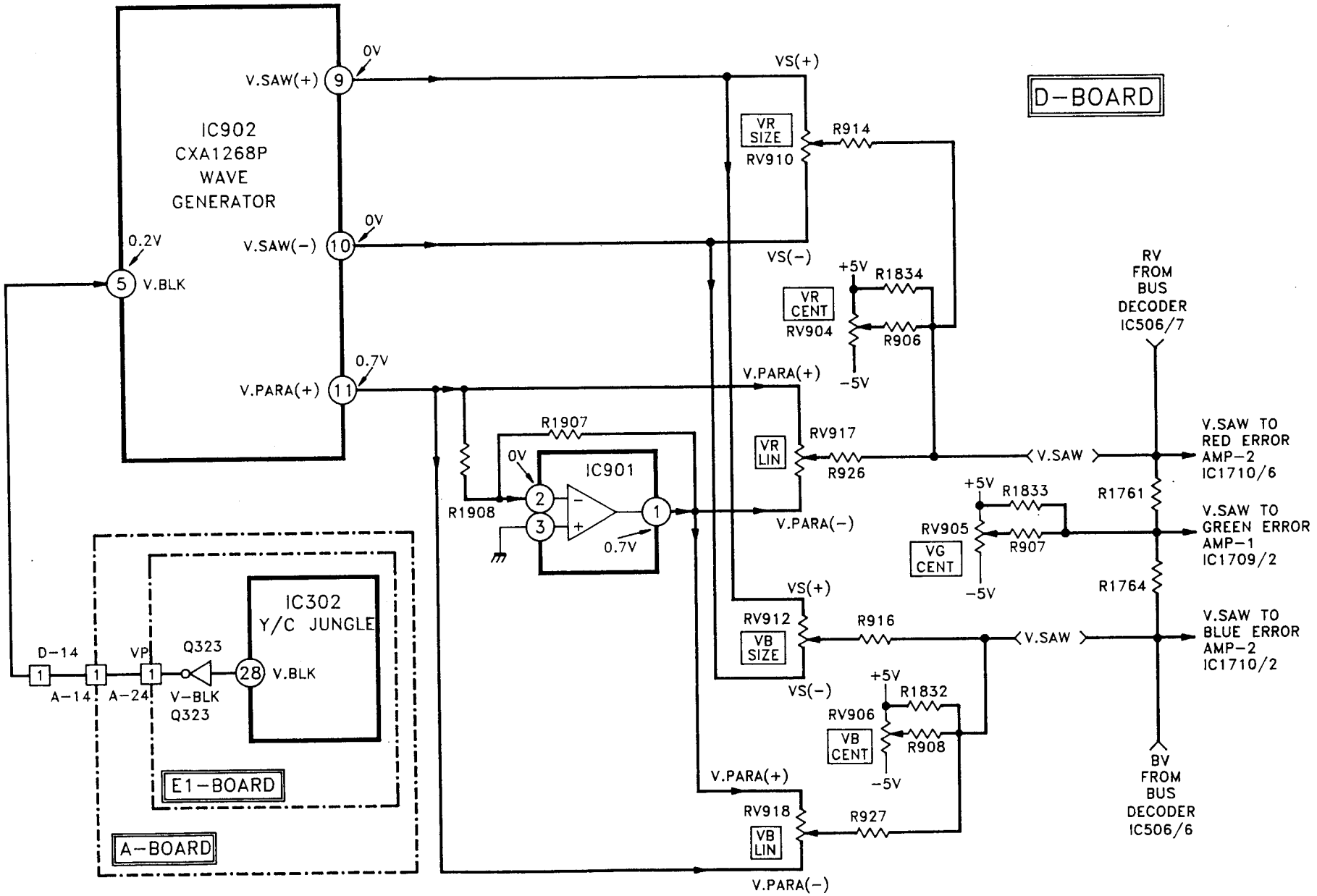
1. Loss of vertical deflection (video is muted). This problem is mainly due to the loss of the V.Blk signal at IC902/pin 5. Since the set is protected during complete loss of vertical beam deflection, the video picture is muted by removing RGB outputs to the CRT drive circuits.

2. Horizontal line across the screen. This problem is mainly due to the loss of the +V.SAW signal output from IC902/pin 9. Since this does not cause a complete loss of beam deflection, the video picture is not muted. In this case, check for PCB trace breaks, cold solder joints at the RV910 control and suspect IC902.

3. Linearity distortion. This problem is mainly due to the loss of the -V.SAW signal output from IC902/pin 10. In this case, check for PCB trace breaks, cold solder joints at RV910, and suspect IC902.

4. Severe linearity distortion of the projected picture. This problem is mainly due to the loss of +V.SAW signals from IC902/pin 9. In this case, check for PCB trace breaks, cold solder joints at the RV910 control and suspect IC902.

5. Picture fold-over at the center of the screen coupled with stretching at the top and bottom halves of the projected image. This problem is mainly due to the loss of the -V.SAW signal at the input of IC901/pin 2. In this case, check for PCB trace breaks around IC901 and suspect IC901.



VERTICAL DRIVE

Blue/Red Vertical Centering Control

Overview

The purpose of the blue and red vertical centering circuits is to allow the customer to adjust registration using the remote control unit. In order to respond to remote control SIRCS inputs, this circuit utilizes a Bus Decoder IC, and a DC Amplifier in order to apply a dc correction voltage to the vertical sawtooth deflection (V.SAW) signal. The dc voltage acts on the deflection signals by shifting the blue and red horizontal picture up or down until it converges with the green.

Operation

Acting on data at IC506/pin 14, the IC outputs a blue vertical dc offset voltage at IC506/pin 6 to the blue vertical V.SAW signal. In a similar manner, a red vertical dc offset voltage is output from IC506/pin 7, to the red vertical V.SAW signal.

These offset voltages, from either IC506/pin 6 and pin 7, are adjusted by selecting a red or blue horizontal convergence symbol from the convergence screen menu, using the SIRCS remote control unit.

Selecting one of the horizontal convergence symbols and then pressing the remote A/V Window +/- keys will generate data and clock signals from the control IC, to IC506/pin 14(DAT) and pin 15(CLK). The voltage output from IC506/pin 6 or pin 7 will swing up or down, depending on the key pressed. As a result, a dc offset voltage is applied to the V.SAW signal through the appropriate dc amplifier circuit.

The blue and red horizontal centering circuits are similar to the vertical centering circuit. They send dc offset voltages from IC506/pin 4 and pin 5 respectively through buffers Q504 and Q509, to IC1552 on the V-Board. This circuit is discussed later on.

Troubleshooting

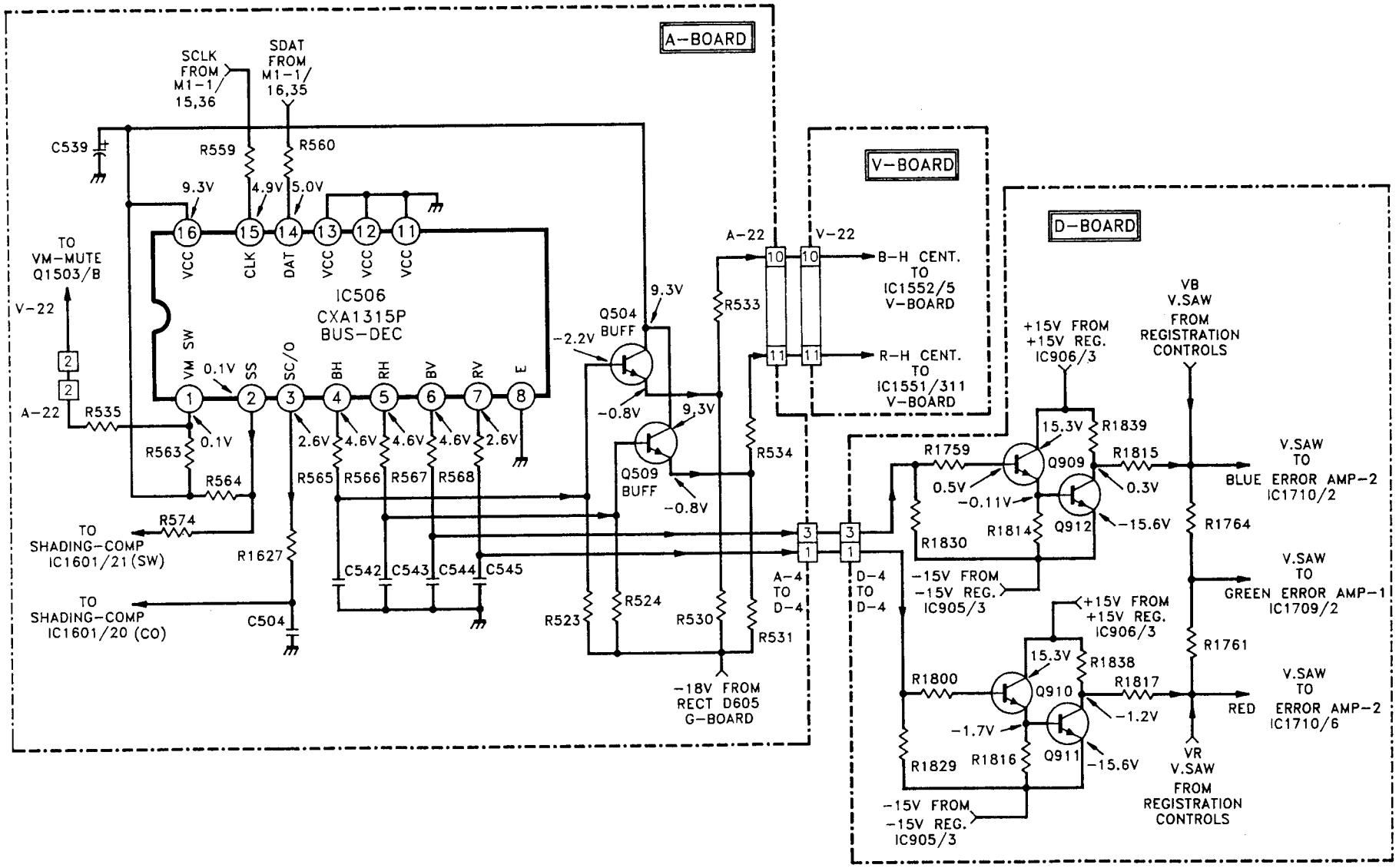
The symptom of a faulty blue or red centering circuit is poor convergence of the overall picture. The amplifier circuits are dc coupled so a problem with one of the transistors will affect the entire stage. If the voltages are not at specs, suspect the transistors for PN junction failure or leakage problems.

If the problem is such that either the red, the blue or both cannot be centered, verify that the voltages at IC506/pin 6 and pin 7 do change when performing the appropriate blue or red color registration adjustment. If the voltages at pin 6 and pin 7 do not change then suspect the Bus Decoder IC 506.

The voltages listed below are the maximum and minimum ranges for the blue and red outputs.

IC506/pin No.	Minimum Vdc	Maximum Vdc
4	0.38Vdc	8.56Vdc
5	0.40Vdc	8.56Vdc

N O T E :
Since the vertical centering circuits are basically in parallel with the registration control circuits, both will affect the convergence of the overall picture. Therefore, the dc voltages for IC506/pins 4, 5, 6 and 7 must first be set to their electrical center dc values before attempting any adjustment to the mechanical controls. To arrive at the center dc electrical values, for each stage, add the minimum and maximum dc voltages from the above list and divide the result by 2. Then, set the control to the calculated dc voltages, by adjusting the customer convergence using the remote control unit.



BLUE/RED VERTICAL CENTERING CONTROL

Green Vertical Deflection

Overview

The Green Vertical Deflection stage provides the proper signals to trace the beam from the top to the bottom on the CRT screen. The vertical deflection circuit consists of two sections:

1. Vertical Error Amplifier (feedback control) IC1709.

2. Vertical Output IC1707 (UPC1498H).

Operation

Since the operation of the red and blue vertical deflection stages are the same, only the operation pertaining to the green vertical stage will be covered.

The V.SAW signal from the registration circuits is coupled through R1765 to Green Error Amp IC1709/pin 2. From IC1709, the vertical sawtooth signal (V.SAW) is output from IC1709/pin 1 and coupled through R1772 to the Vertical Output IC1707/pin 4. From IC1707/pin 4, the vertical sawtooth signal is coupled to an internal vertical deflection voltage boost stage. From there, the vertical sawtooth deflection signal is output to IC1707/pin 2.

Normally, the sawtooth signal applied to IC1707/pin 4 is 838mVp-p. The signal output from IC1707/pin 2 is 62.3Vp-p. To bring the output pulses up to 62.3Vp-p, C1721 is charged by a 31.1Vp-p pulses output from IC1707/pin 7 during the vertical retrace period. During the vertical trace time only the power supply voltage is applied to the internal vertical deflection output stage. However, during the vertical retrace time, the power supply voltage plus the charge stored in C1731, are added to the vertical output deflection stage, thus allowing the output deflection signal to reach the 62.3Vp-p level. Since the high power voltage to the output stage IC is developed only during the vertical retrace interval, peak power consumption is greatly reduced.

The output sawtooth deflection signal from IC1701/pin 2 is coupled through connectors D-2 and ZG-2 pins-7 to the vertical deflection coils, through connectors D-2 and ZG-2 pins-6, and through resistor R1784, R985 and R1783 to ground. R1769 provides negative feedback, thus stabilizing this stage.

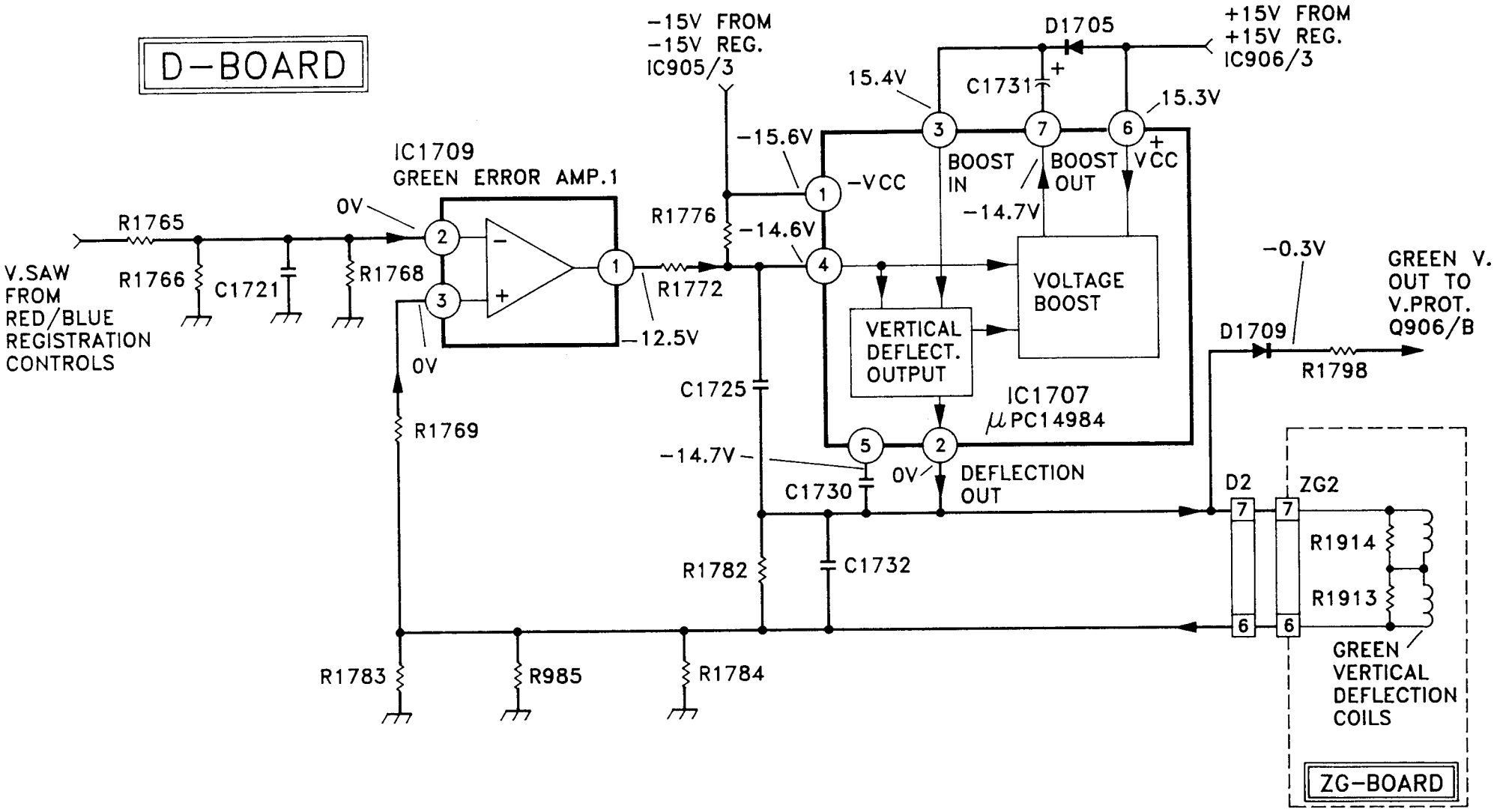
The output sawtooth deflection signal from IC1701/pin 2 is also coupled through D1709 and R1789 to the base of Vertical Protect Q906 (not shown). The Vertical Protect circuits are used to protect the CRTs from phosphor burns in the event that vertical deflection is lost.

Troubleshooting

The symptom of no vertical deflection is a blanked raster (no video). However, if the vertical deflection coil opens, a horizontal line will be displayed at the center of the screen.

In the event of a green circuit failure, verify the presence of an 838mVp-p deflection signal at IC1707/pin 4. If missing, troubleshoot around the input circuits of the IC. If the input signal is present, check for a 62.3Vp-p sawtooth signal at IC1707/pin 2. If missing or low in amplitude, check for a 31.1Vp-p boost signal from IC1707/pin 7. If this signal is present, check the voltages and components around the IC, and if okay, suspect the IC. If the vertical deflection signal is present at IC1707/pin 2, check the components associated with the vertical deflection coil.

NOTE: Vertical linearity or fold-over problems may be caused by the vertical feedback and biasing circuits. The symptom of an opened C1731 is a fold-over picture that does not reach the top of the screen. IC1707 may also be damaged by prolonged operation with an open C1731.



GREEN VERTICAL DEFLECTION

Vertical Protect

Overview

The purpose of the Vertical Protect circuit is to prevent damage to the CRT phosphors in the event vertical deflection is lost. To do this, the vertical protection circuits monitor the vertical deflection output signals from the vertical output stages. If missing, the protection circuit is triggered to remove RGB outputs from the Y/C Jungle IC.

Operation

The operation of the protection circuit centers around the red vertical deflection signal so we will discuss this first. The vertical protect circuit, in the diagram below, is comprised of Q906 and Q907. The red vertical output deflection signal, from IC1706/pin 2, is coupled through R1775, voltage divider R1795 and R1791 to the base of Vertical Protect buffer Q906. During normal operation the signal applied to the base of Q906 is reduced from 62Vp-p to 13Vp-p through voltage divider network R1795 and R1791.

From the base of Q906, the deflection signal is output from its emitter at a 8.9Vp-p level. D1708 and C1739 rectify and filter the deflection signal to 7.2Vdc. This voltage is coupled through R1797 and R1789 to the base of Q907. The voltage at the base of Q907 is reduced to 0.7Vdc through voltage divider network R1797 and R1789.

With 0.7Vdc applied at its base, Q907 will turn ON. When 907 turns ON, its collector voltage goes LOW (0Vdc). Q907's collector voltage is coupled through D1707, connectors D-4 and A-4 pin-4, D1608, connector E2-1/pin 3 to the input of inverter Q326. Since the input voltage to the inverter is LOW, its output will go HIGH (open circuit). The inverter output is connected to the Y/C Jungle IC302/pin 27(FILTER). As a result IC302/pin 27 is held to approximately 7.9Vdc.

In the event that red vertical deflection is lost, the base of Q907 will go LOW and its emitter will go HIGH (8.3Vdc). A HIGH will also be applied through D1707, connectors D-4 and A-4 pin-4, D1608, connector E2-1/pin 3 to the inverter Q326. The input voltage to the inverter is HIGH, so its output will go LOW (0Vdc). The inverter output is connected to the Y/C Jungle IC302/pin 27(FILTER). As a result IC302/pin 27 will be brought to LOW (0Vdc), which triggers an internal muting to remove RGB outputs to the CRTs.

Normally, the blue and green vertical deflection signals prevent D1709 and D1710 from forward biasing. However, if either deflection signal or both is lost, the red deflection signal will forward bias and pass through the respective diode. As a result, the red signal level, at the base of Q906, will go below the threshold level necessary to keep Q907 turned ON and the effect is the same as having no red vertical deflection.

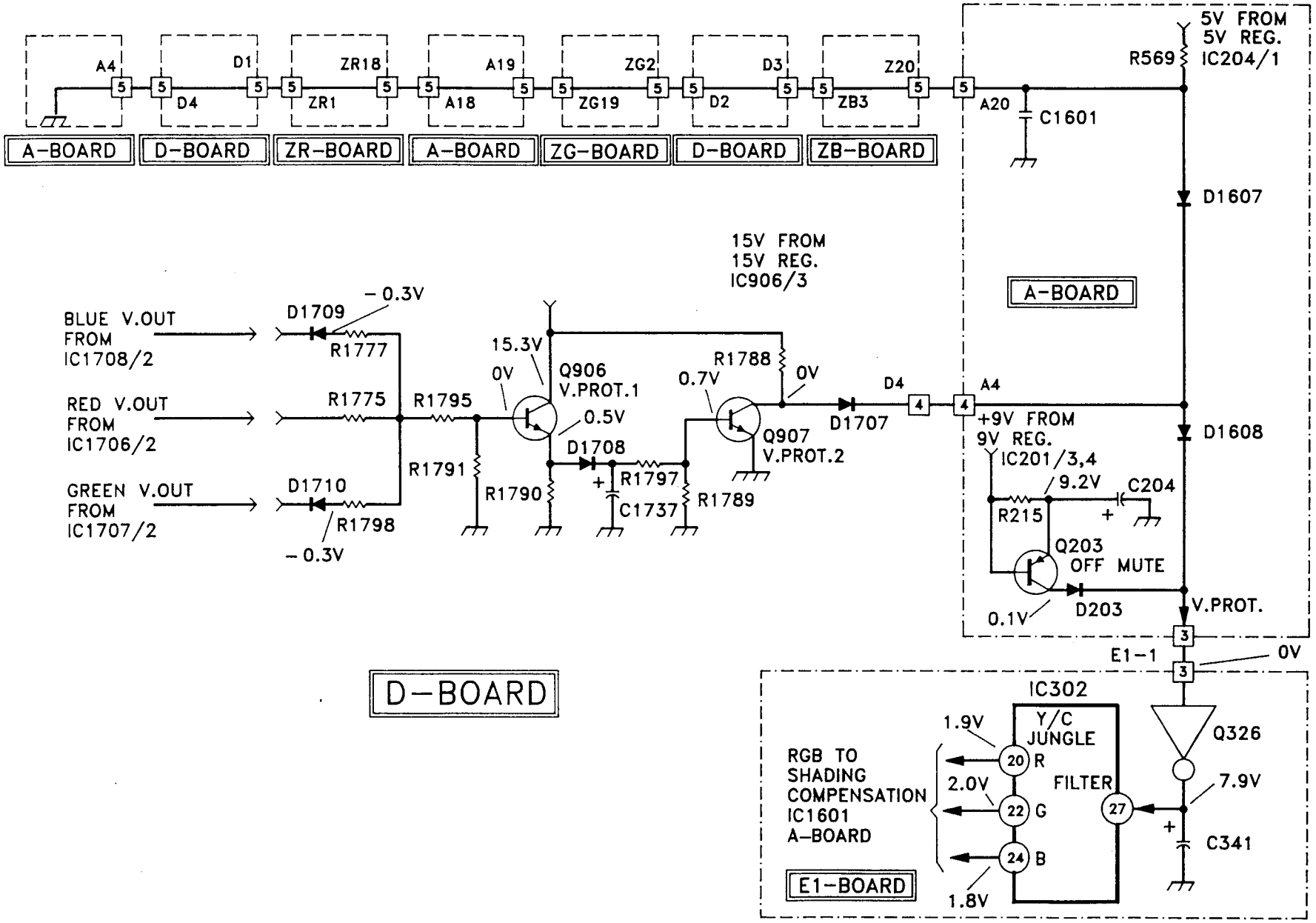
Yoke Ground Interrupt Detection

The deflection yokes are monitored by the vertical protect circuit to ensure that they are connected to the CRTs. All three deflection yokes are connected through harness wiring, in series, to ground. The other end is connected to the anode of D1706 and through a series resistor, R569, to the regulated +5Vdc line at IC204/pin 1. As long as the path to ground is not interrupted (broken), the anode of the D1607 will remain grounded. If any yoke is unplugged, the ground path connection will be broken. As a result, D1607 will have +5Vdc applied to its anode and the effect is the same as having no vertical deflection.

Power OFF CRT Burn Protect

Q203, R215 and C204 is a CRT burn prevent circuit. This circuit operates when main power to the set is turned OFF by removing RGB outputs to the CRTs.

When main power is applied to the set, C204 will charge from ground through R205 and the regulated +9Vdc line. At this time Q203 remains OFF because its emitter voltage will be less than its base voltage. When the set's main power is turned OFF, the regulated +9Vdc supply will be cut off and Q203's base voltage will go to 0Vdc. C204 will now discharge through R215 and the +9Vdc supply to ground. As a result, Q203 will be forward biased by the voltage drop across R215 and will turn ON. When Q203 turns ON, it will couple a 4.2Vdc discharge voltage through D203 to inverter Q326. The result is the same as having no vertical deflection.



VERTICAL PROTECT

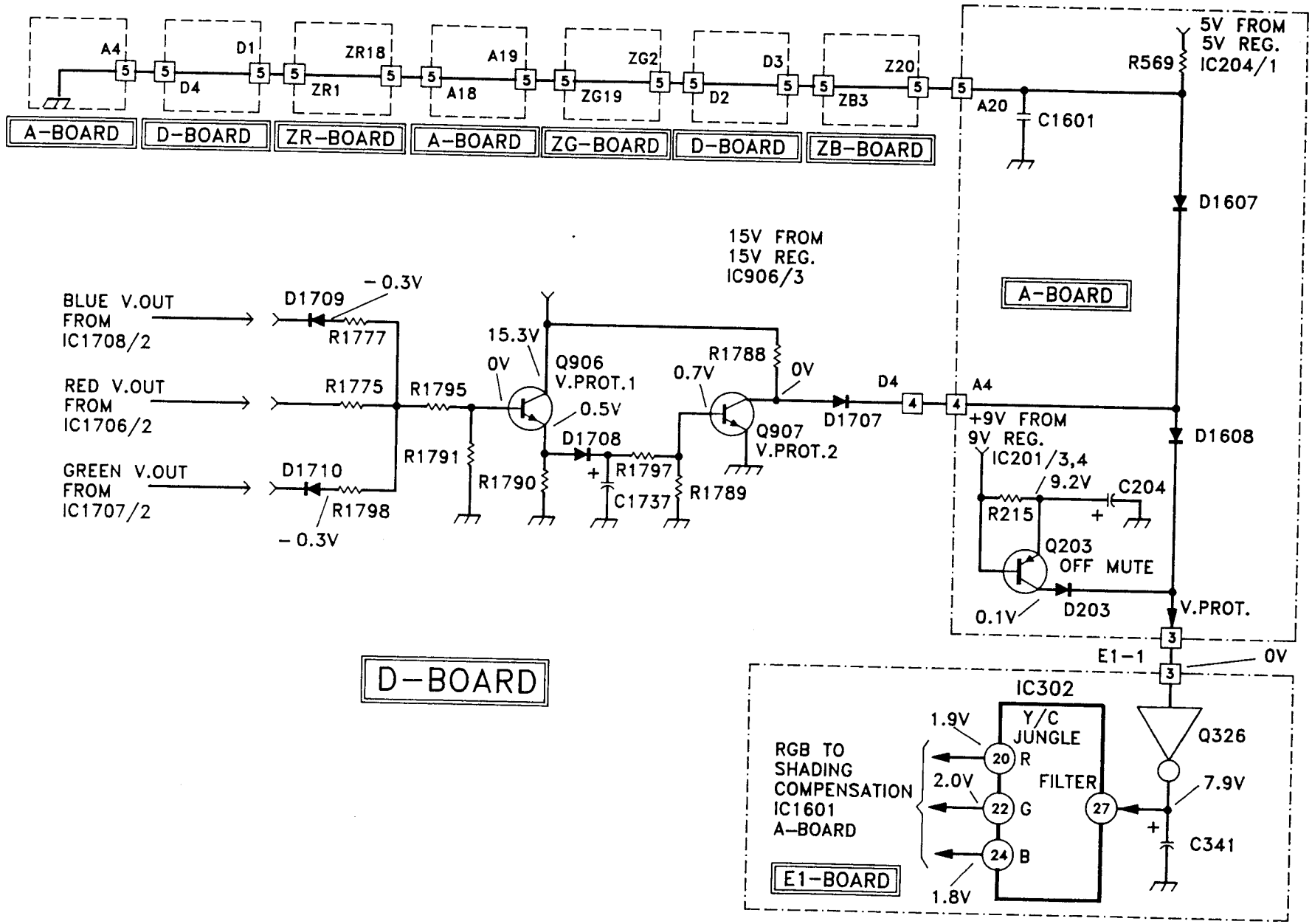
Troubleshooting

When servicing the set for no raster conditions, you should verify the operation of the Vertical Protect circuitry. To do this do the following:

1. Check for 0Vdc at E1-1/pin 3. If greater than 0Vdc, check at the collector of Q203 for -0.1Vdc. If greater than -0.1Vdc suspect Q203 for PN junction failure.

2. If okay, check for 0Vdc at the anode of D1607. If 5Vdc, check for continuity through the respective circuit board interlock connections.

3. If okay, check for 0Vdc at the collector of Q907. If missing, check for an 8.9Vp-p vertical deflection signal at the emitter of Q906 and for a 13Vp-p vertical deflection signal at the base of Q906. If missing, troubleshoot the individual vertical deflection output stages.



VERTICAL PROTECT

Horizontal Deflection

Operation

The horizontal drive signal (H.D.) from the jungle IC is input to horizontal drive transistor Q501. Q501 drives the primary of coupling transformer T502. The secondary of T502 drives H-OUT transistor Q502, via D503 and R508. R508 limits the base current to the horizontal output transistor. D503 is a speed up diode.

The output of Q502 drives the three deflection coils via R509 and L501. L501 is the horizontal linearity coil.

In this circuit, damper diode D507 is not part of the horizontal output transistor package.

The horizontal output circuit uses a negative power supply. Horizontal output transistor Q502 emitter is connected to a -109 Vdc potential which is provided by pincushion output transistor Q508. The collector of Q502 is connected to ground through linearity coil L501 and the primary of horizontal output transformer (H.O.T.) T501/pins 2 and 4.

From the horizontal output transistor, the horizontal deflection signal is sent to three parallel connected horizontal deflection coils, of the CRT yokes, and to the horizontal output transformer T501.

The center tapped secondary winding of the horizontal output transformer supplies positive and negative 15 volt power, via rectifiers D501 and D502, to the horizontal centering circuit on the V-Board (not shown). It also supplies an H blanking signal to waveform generator IC902 (not shown). The blanking signal is taken from pin 8 of the H.O.T. and coupled through R521, buffer Q510, R526, to IC902/pin 24.

Protection

The horizontal deflection circuit is monitored by the main protection circuit. If the horizontal deflection circuit stops operating, the unit will shut off. The monitoring circuit operates as follows:

1. During normal operation an AC signal, at the horizontal rate, is output from H.O.T. T501/pin 8.

2. The AC signal is fed through R521, to the junction of zener diode D504, D509 to the base of Q510.

3. The zener diode shunts the negative segments of the ac signal to ground, and clips the positive segments at 5.1Vdc.

4. The positive signal segments are fed through isolation diode D509, filter capacitor C513 and R570 to the base of Q511 in the protection circuit (not shown). The capacitor filters the positive waveforms into a 4.9Vdc level.

5. The configuration of the protection circuit (not shown) is such, that a 4.9Vdc potential at the cathode of D509 will not trigger the protection circuit. In the event the horizontal deflection circuit fails, the 4.9Vdc potential will disappear, the protection will trigger, and the unit will shut off.

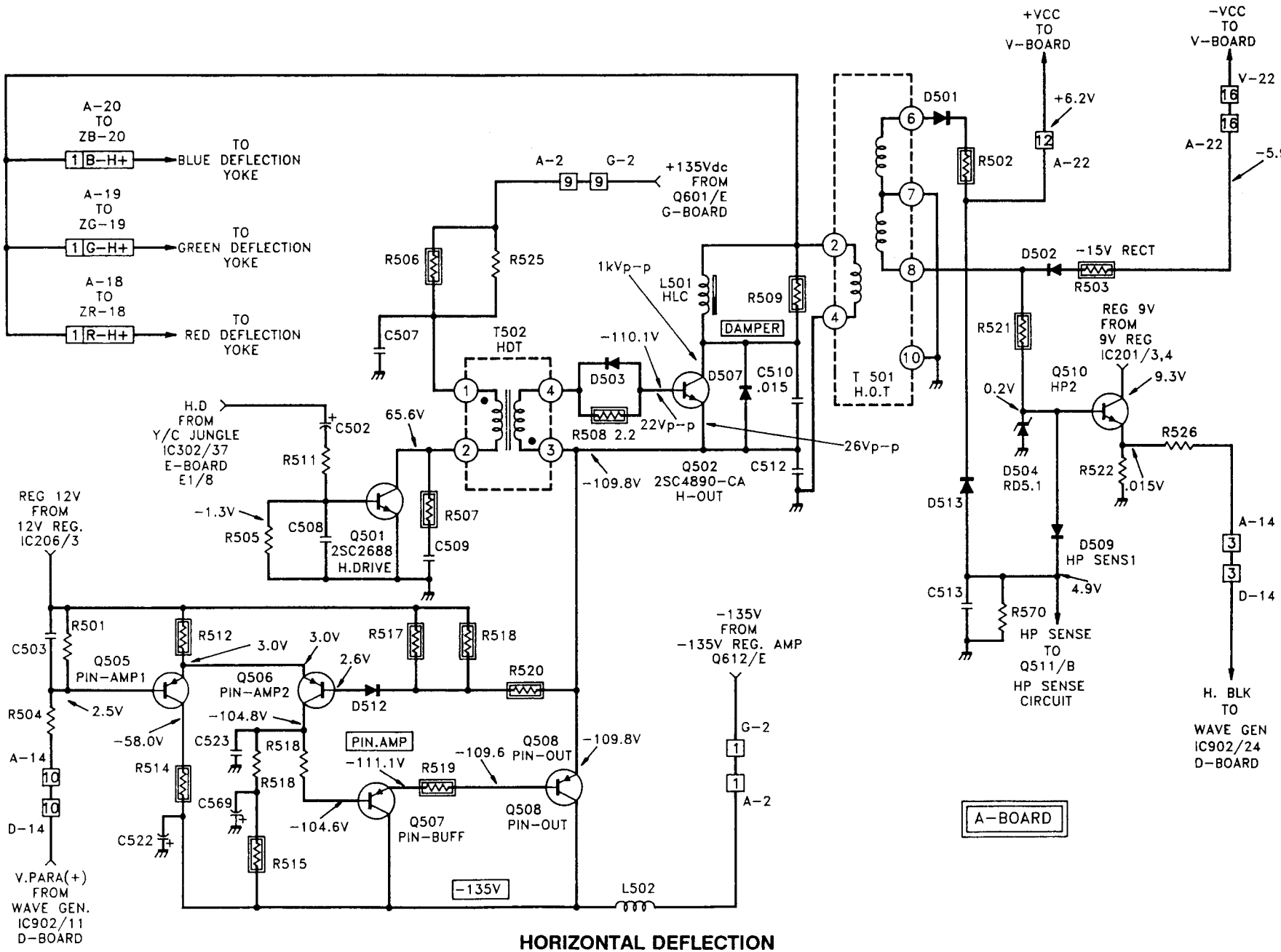
Pincushion Circuit

Transistors Q505 through Q508 form the pincushion correction circuit. This circuit corrects the bowing effect on the left and right sides of the picture caused by the CRTs. The circuit operates in the following manner:

1. Transistors Q505 and Q506 are a differential amplifier pair. A parabola signal, which is the pincushion correction signal, is input from wave generator IC902 (not shown), through R504, to Q505 base.

2. The differential output is taken from the collector of Q506, and sent to emitter followers Q507 and Q508. The two emitter followers are connected in a darlington pair configuration. This provides unity voltage gain and extremely high current gain.

3. Q508 is connected in series with the power supply line of the horizontal deflection output transistor. This causes the parabola circuit to modulate the power supplied to the deflection output and independently vary the yoke drive current. The parabola signal is timed with the vertical deflection so that deflection current is maximized when scanning the center of the CRTs, and progressively reduced when the tops and bottoms of the CRTs are scanned.



HORIZONTAL DEFLECTION

Troubleshooting

A lack of horizontal deflection causes the main system protection circuit to trigger and shut down the unit. Shutdown can also be caused by defects in many other circuits. Therefore, in order to isolate the problem to a particular circuit, the technician should first follow the troubleshooting procedure outlined in the power supply section. If the shutdown problem is isolated to the horizontal deflection circuit, the procedures outlined here should be followed:

1. Prior to turning power ON, check Q502 with an ohmmeter. If it is defective, also check Q508, and Q611 and Q612 on the G-Board. Replace the defective components as necessary.

2. Bypass the protection shutoff by following the procedure outlined in the power supply troubleshooting procedure.

3. Remove connector N-4. This disables the HV and prevents a CRT burn due to a lack of deflection.

4. Check at connector N-10 on the N-Board for HD signals from Jungle IC302/pin 37 (not shown). This connector provides an easy access point to the HD signals. A lack of HD signals will prevent the horizontal deflection circuit from operating. If HD signals are missing then repair that problem before proceeding further.

5. A. Connect an oscilloscope probe to the collector of Q502.

   B. Connect the AC line to a variac having both a voltmeter and an ammeter.

   C. Slowly turn up the variac voltage from 0Vac to 33Vac, simultaneously checking that the ac current does not exceed 2 amperes. At this input ac voltage a properly operating deflection circuit will have a deflection signal at Q502 collector in excess of 460V p-p. The signal frequency will vary from 12kHz to 16kHz. Proceed with the next step if the ac current is not excessive and HD pulses are still not correct at the collector of Q502.

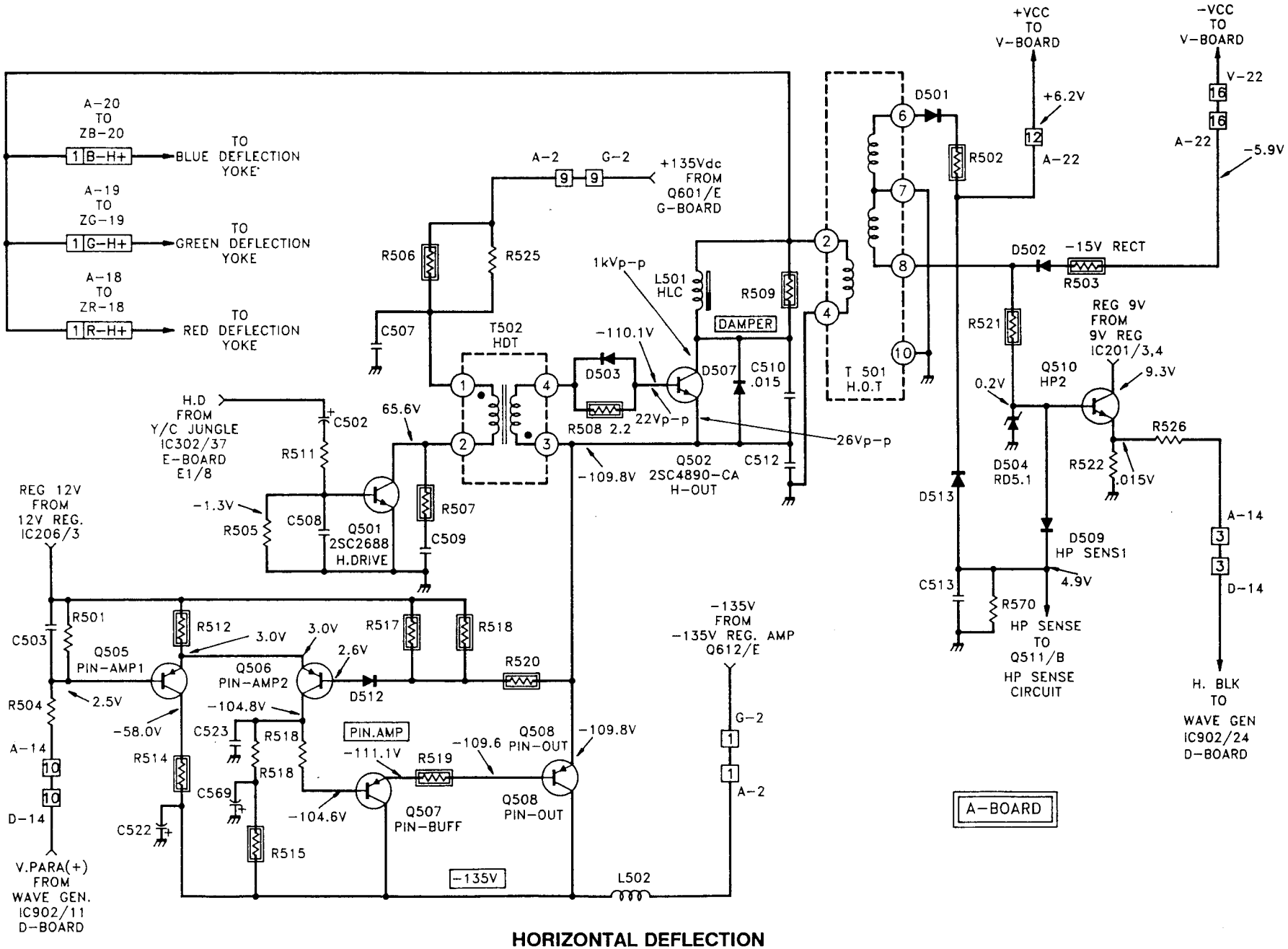
6. Increase the ac line voltage to 117Vac. Check for -109Vdc at the emitter of Q502. A convenient point to access this voltage is at the anode of damper diode D507.

   * If -109Vdc is present, signal trace the deflection circuit. Start at coupling capacitor C502 and continue down stream to the deflection coil connectors (A-18, A-19, A-20). Also check the circuits down stream of the secondary of T501. A missing signal in this area can trigger the protect circuit or prevent the centering circuit (not shown) from operating.

   * If -109Vdc is not present, check the collector of Q508 for -135Vdc.

     A. If -135Vdc is present, a problem may exist in the pincushion circuit.

     B. If -135Vdc is not present, check the power supply board and repair the missing -135Vdc problem.



HORIZONTAL DEFLECTION

Red Horizontal Centering

Overview

The purpose of the blue and red horizontal centering circuits is to allow for customer registration adjustments utilizing the set's SIRCS remote unit. To respond to SIRCS inputs, this circuit utilizes a Bus Decoder IC and DC Amplifier circuit to apply a dc correction voltage to the horizontal return deflection signal. The dc voltage acts on the deflection signal by shifting the blue and red horizontal picture left or right until it converges with the green center picture.

Operation

The circuits for the blue and red horizontal centering circuits are the same so the red circuit is used to explained operation for both. The Bus Decoder outputs a red horizontal dc offset voltage from IC506/pin 5 (not shown) through R566, buffer Q509, R534, connectors A-22 and V-22/pin 11, R1582 to red centering operational amplifier IC1551/pin 3. The input dc voltage at pin 3 is compared to the voltage at pin 2. The resulting dc voltage is output from IC1551/pin 1 and coupled through R1553 to the bases of the Red Horizontal Output Drives Q1551 and Q1552.

The Red Horizontal Output Drives, Q1551 and Q1552, are connected as push pull dc amplifiers with their collectors connected to positive and negative supplies. Basically, both Q1551 and Q1552 act as series variable resistors with their emitters serving as output center taps. If for instance, less positive output is wanted, from the emitter junctions, Q1551 is turned ON less (higher resistance) and Q1552 is turned ON more (less resistance). As a result, the voltage from the emitter junctions will swing more negative. The reverse happens if more positive voltage is wanted at the output.

The output voltage, at the emitter junction, is coupled through R1555, R1556 and R1557 to the return side of the horizontal deflection coil. The horizontal deflection signal must pass through R1555, R1556 and R1557 and through R1558 and R1559 to ground. As a result, the horizontal picture will be shifted to the left, with a greater positive dc offset voltage and to the right, with a greater negative dc offset voltage, from the center of the screen.

The horizontal red centering dc voltage coupled to IC1551/pin 3, from horizontal registration centering control RV901, via R1578 will also influence the position of the picture on the screen. Negative feedback is applied through R1554 to IC1551/pin 6 and through R1558 to IC1551/pin 5. The output from IC1551/pin 7 is applied to IC1551/pin 2 where it is compared to the input dc offset voltage input to IC1551/pin 3 to stabilize the circuit.

The dc offset voltage, output from IC506/pin 4 and pin 5 are normally changed by selecting a red or blue vertical convergence symbol, from the convergence screen menu display, using the SIRCS remote control unit. Selecting one of the vertical convergence symbols and then pressing the remote A/V Window +/- keys will generate data and clock signals, from the control IC, to IC506/pin 14(DAT) and pin 15(CLK). The voltage output from IC506/pin 4 or pin 5 will swing up or down depending on the key pressed. As a result, a dc offset voltage is applied to the horizontal deflection signal through the appropriate dc amplifier circuit.

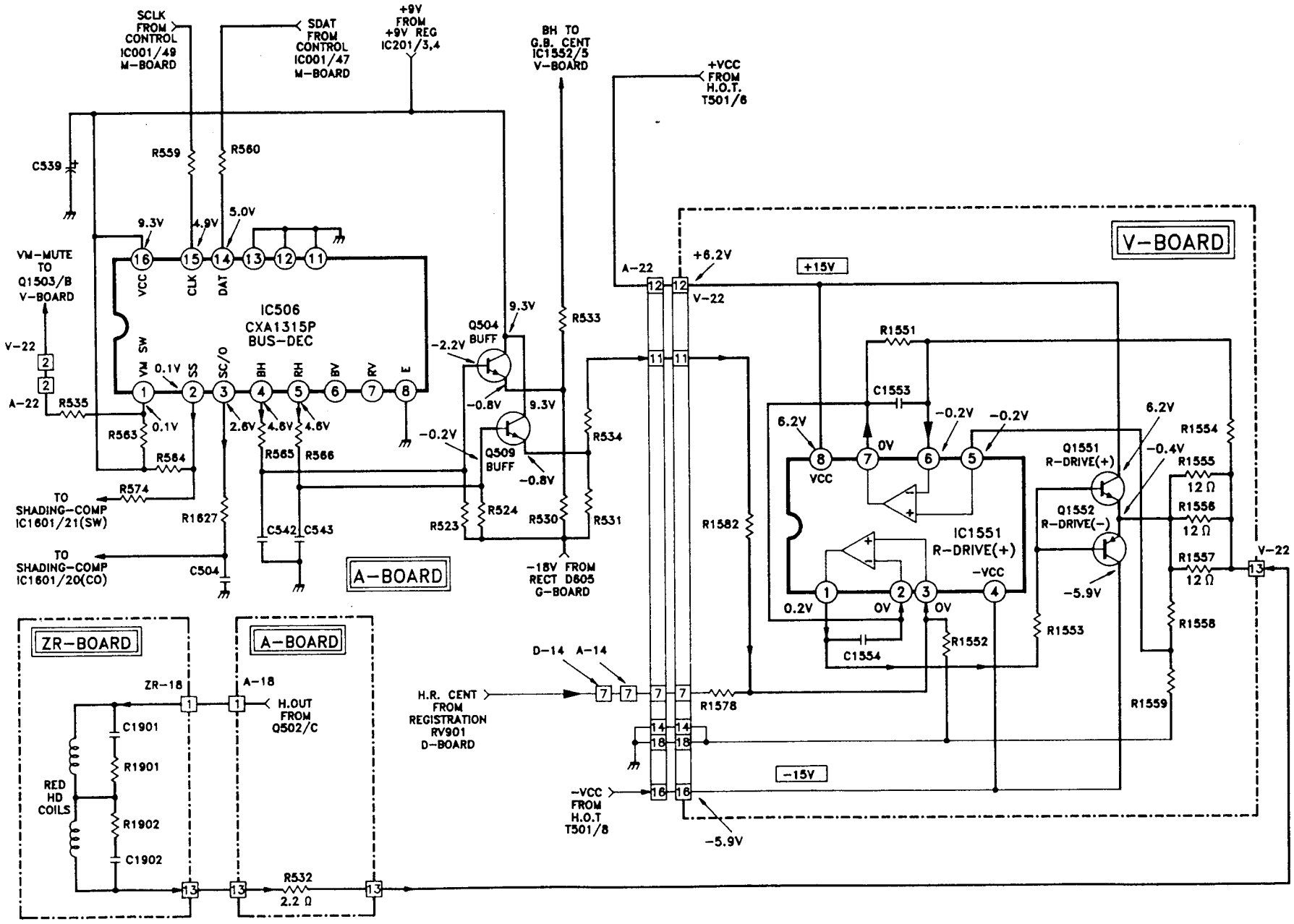
Troubleshooting

The symptom of a faulty blue or red centering circuit is poor convergence of the overall picture. The dc amplifier circuits are dc coupled so a problem with one of the transistors will affect the entire stage. If the voltages don't measure as they should, suspect the transistors for PN junction failure and for leakage problems.

If the problem is one where only one adjustment or both is not possible, then verify that the voltages at IC506/pin 6 and pin 7 do change when performing the appropriate blue or red color registration adjustment. If the voltages at pin 6 and pin 7 do not change then suspect the Bus Decoder IC 506. The voltages listed below are the maximum and minimum ranges for the blue and red outputs.

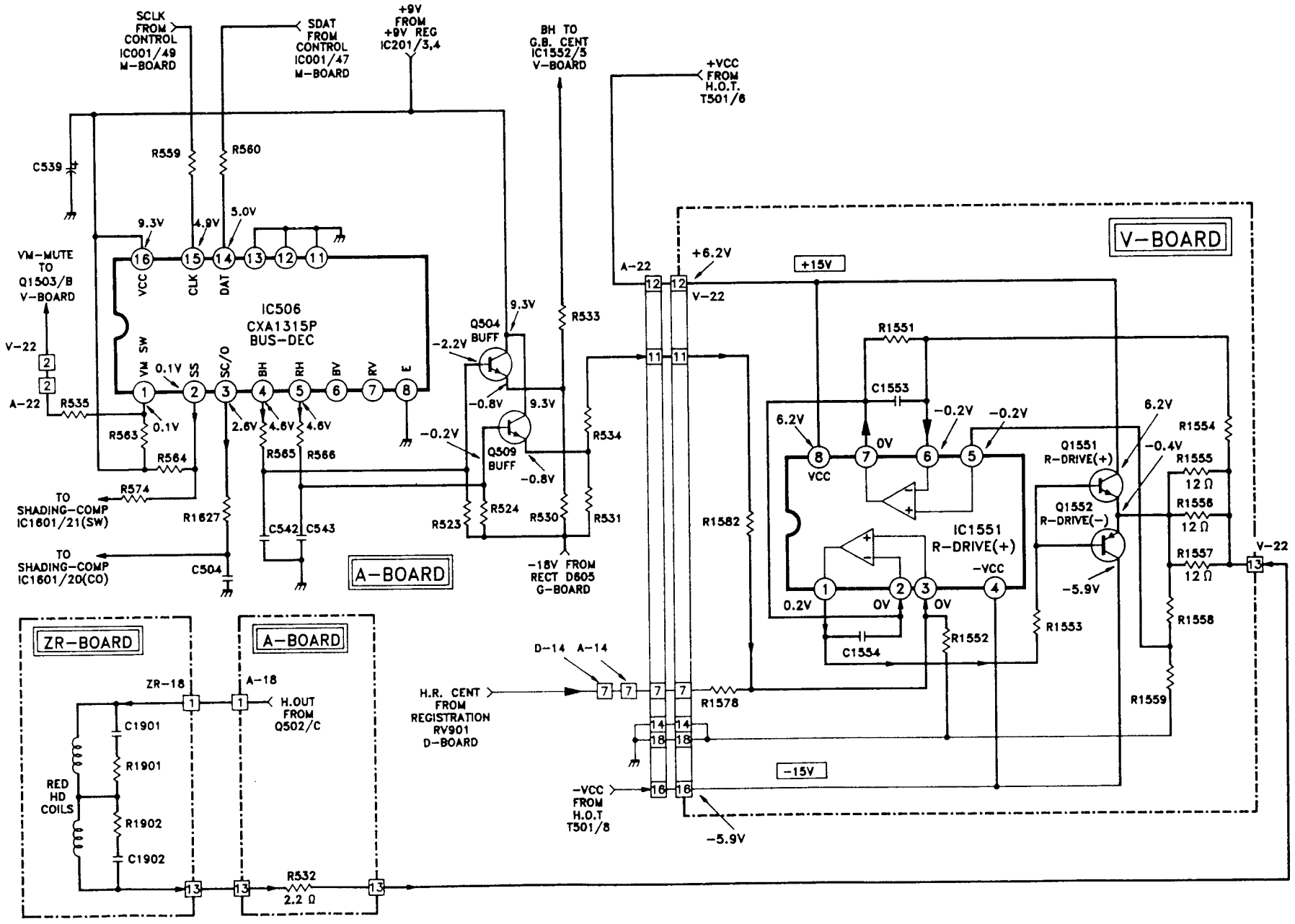
IC506/pin No.	Minimum Vdc	Maximum Vdc
6	0.38Vdc	8.57Vdc
7	0.42Vdc	8.57Vdc

NOTE: Since the vertical centering circuits are basically in parallel with the



RED HORIZONTAL CENTERING

registration control circuits, both will affect the convergence of the overall picture. Therefore, the dc voltages for IC506/pins 4 and 5 must first be set to their electrical center dc values before attempting any adjustment to the set's registration mechanical controls. To arrive at the center dc electrical values, for each stage, add the minimum and maximum dc voltages from the above list and divide the result by 2. Then set to the arrived calculated dc voltages, for each stage, by adjusting the customer convergence using the remote control unit



RED HORIZONTAL CENTERING

HV Block

Overview

The high voltage section consists of three circuits. These are:

1. A converter circuit for generating the high voltage.
2. A regulator circuit for maintaining high voltage regulation.
3. A protection circuit which shuts down the high voltage in cases of high voltage, over voltage, or over current conditions.

Converter

The high voltages for the CRT anodes are formed in the following manner. The horizontal drive signal (HD) from jungle IC302 (not shown) is amplified by the HD circuit, and then transformer coupled to the HV converter. The HV converter drives the flyback transformer (FBT) which provides the high voltage. The high voltage rectifiers are encased within the FBT. The high voltage output from the FBT is fed to HV block. The HV block distributes the high voltage to the CRT anodes.

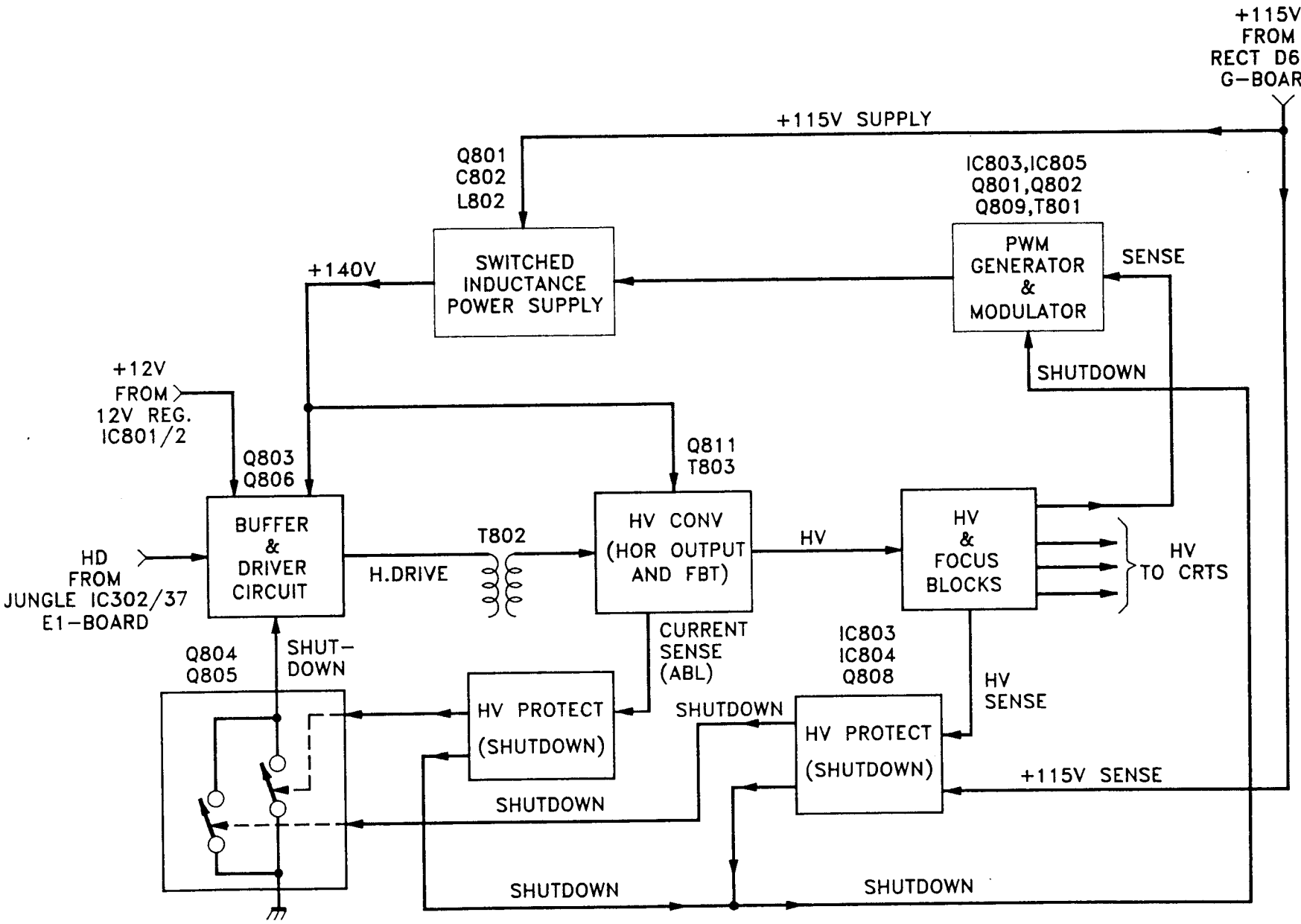
Regulator

High voltage regulation is accomplished by boosting the B+ voltage which powers the HV converter, then regulating the amount of boost. The B+ boost increases when the high voltage drops, and decreases when the high voltage goes up, thus providing regulation.

The HV boost circuit consists of a switched inductor PWM power supply which boosts the B+ voltage level. The PWM signals are produced by a PWM generator circuit, then fed to the boost circuit. The PWM generator monitors the high voltage level by sampling it at a low voltage tap on the HV block, then adjusting the pulse width of the PWM generator according to the level of the sampled signal.

Protection

High voltage shutdown protection is provided by two protect circuits. One protect circuit senses HV over current conditions via the ABL circuit. The other protect circuit senses over voltage conditions. In the event of an over voltage or over current condition, the protect circuits will shut down the high voltage converter. This is done by shorting the horizontal drive signals to ground via Q804 and Q805 and also by shutting down the PWM generator, thus disabling the B+ boost in the HV regulator.


+115V
FROM
RECT D603
G-BOARD
+115V SUPPLY
Q801
C802
L802
IC803,IC805
Q801,Q802
Q809,T801
SWITCHED
INDUCTANCE
POWER SUPPLY
+140V
PWM
GENERATOR
&
MODULATOR
SENSE
SHUTDOWN
+12V
FROM
12V REG.
IC801/2
Q803
Q806
Q811
T803
BUFFER
&
DRIVER
CIRCUIT
T802
HV CONV
(HOR OUTPUT
AND FBT)
HV
HV
&
FOCUS
BLOCKS
HV
TO CRTS
HD
FROM
JUNGLE IC302/37
E1-BOARD
H.DRIVE
CURRENT
SENSE
(ABL)
Q804
Q805
SHUT-
DOWN
IC803
IC804
Q808
HV SENSE
HV PROTECT
(SHUTDOWN)
SHUTDOWN
HV PROTECT
(SHUTDOWN)
+115V SENSE
SHUTDOWN
SHUTDOWN
SHUTDOWN

HV BLOCK

HV Converter

Overview

The high voltage converter provides the high voltages for the CRT anodes and focus grids. The high voltage is developed from the horizontal drive signals which are produced by the jungle IC (not shown). In the HV converter, these signals are amplified, waveshaped, and fed to a flyback transformer. The secondary output of the flyback is rectified, then distributed to the CRT anodes.

Operation

From the jungle IC, the horizontal drive signals are buffered by Q803, then capacitive coupled by C811 to H drive transistor Q806, where they are amplified. From the collector of Q806, the HD signals are transformer coupled to the base of HV converter transistor Q811. After amplification by Q811, the signals are sent to the primary of high voltage transformer T803.

T803 has two high voltage secondary windings. The upper winding, labeled HV, supplies high voltage to the HV block. The HV block then distributes the high voltage to the CRT anodes. The lower winding, labeled MV, supplies the high voltage focus voltage to the focus block. The focus block distributes this voltage to the CRT focus grids.

Power Supply

This circuit is powered by the following power supplies:

* Buffer Q803 is powered by 12 volt regulator IC801. This regulator also supplies power to the pincushion and HP protect circuits (not shown).
* H drive transistor Q806 and HV converter transistor Q811 are powered by the 115Vdc supply line. This voltage is boosted to 140Vdc by the HV regulator circuit before being applied to these transistors. The HV regulator circuit is explained in the HV regulator chapter.

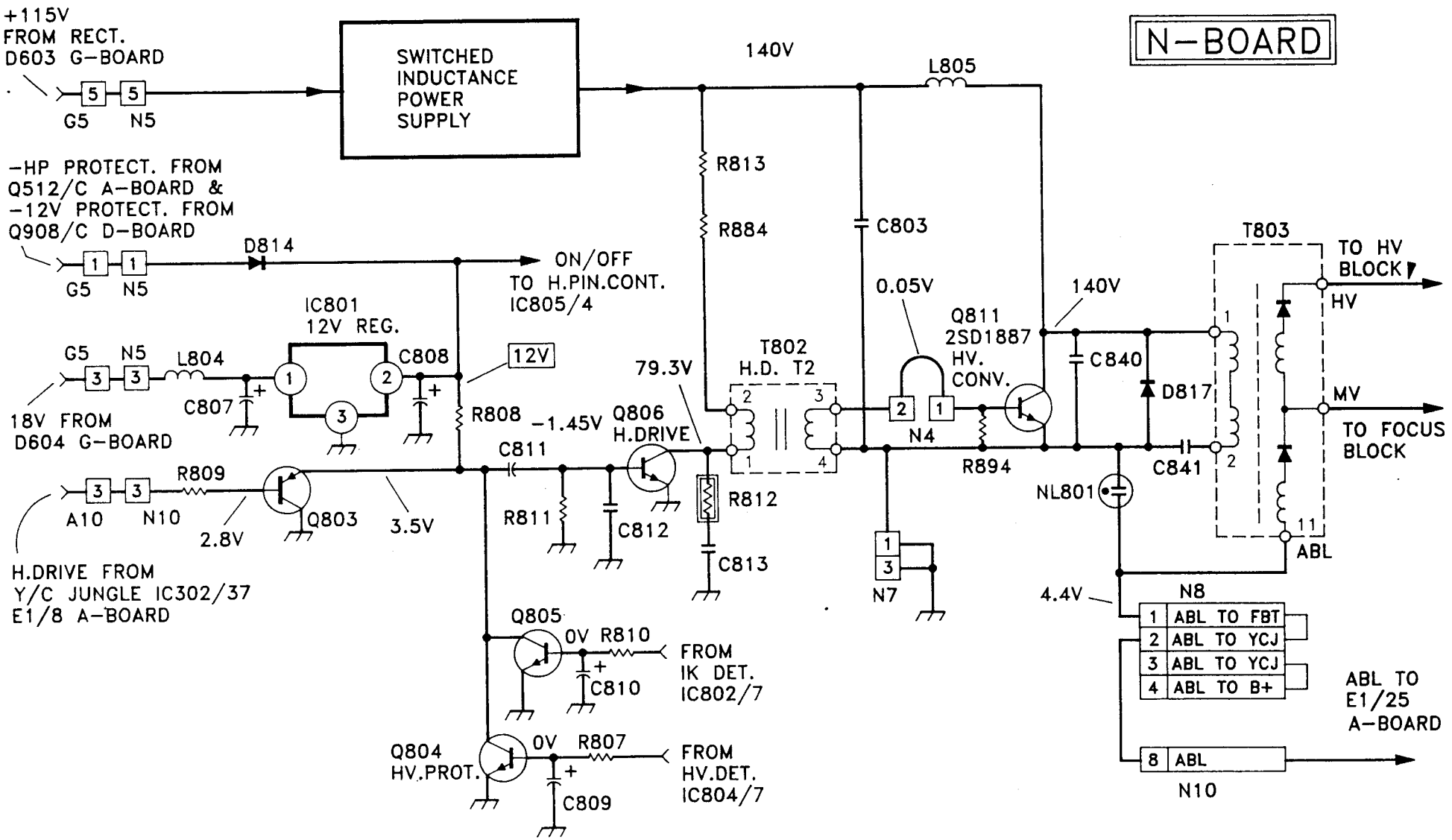
HV Shutdown

Transistors Q804 and Q805 will shut down the HV converter circuit in the event the HV shutdown circuit is triggered. Both of these transistors are connected to the collector of buffer Q803. When the protection circuit (not shown) turns ON, one or both of these transistors will turn ON, shunting the H drive signals at Q803/E to ground. This prevents the high voltage from being generated.

Troubleshooting

When high voltage is not produced, the first step is to determine which circuit is the cause of the problem. It can be in the converter, in the power supplies powering the converter, or in the protection shutdown circuits.

A shorted 115Vdc power supply line in the HV converter will cause the main system protection to trigger and shut down the unit. This shutdown can also be triggered by many other circuits. Therefore, in case of a main power shutdown, the problem should first be isolated to a specific circuit. This is done by following the procedure outlined in the power supply section. If the shutdown problem is isolated to a shorted +115Vdc line in this circuit, the following components should be checked for shorts. Q811, D817, C840, C841, and C803.



HV CONVERTER

To diagnose a problem other than a shorted 115Vdc line, use this method:

1. Determine if the HV protection is shutting down this circuit. With a DVM, check the voltage at the base of Q804 and Q805. They should both be approximately 0Vdc. A voltage of greater than 0.6Vdc, on either or both transistors, indicates an HV protect shutdown. This can be caused by either a defective HV regulator or a defective HV protect circuit. To repair this problem, follow the troubleshooting procedure outlined in the HV regulator section.

2. Determine if a defective power supply is preventing high voltage operation.
   A. Check for 12Vdc at regulator IC801/pin 2.

   B. Check for a minimum of 115Vdc at HV converter Q811 collector. Although the normal level is approximately 140Vdc, high voltage will still be produced at the 115Vdc level. In such an event, check out the HV regulator which is supposed to boost the 115Vdc to 140Vdc.

If 115Vdc is not present at Q811/C, check for 115Vdc at connector CN-5/pin 5:

* If 115Vdc is present, check L803, L801, L802, D801, L805, making sure they are not open.

* If 115Vdc is not present, check the power supply board and repair the problem.

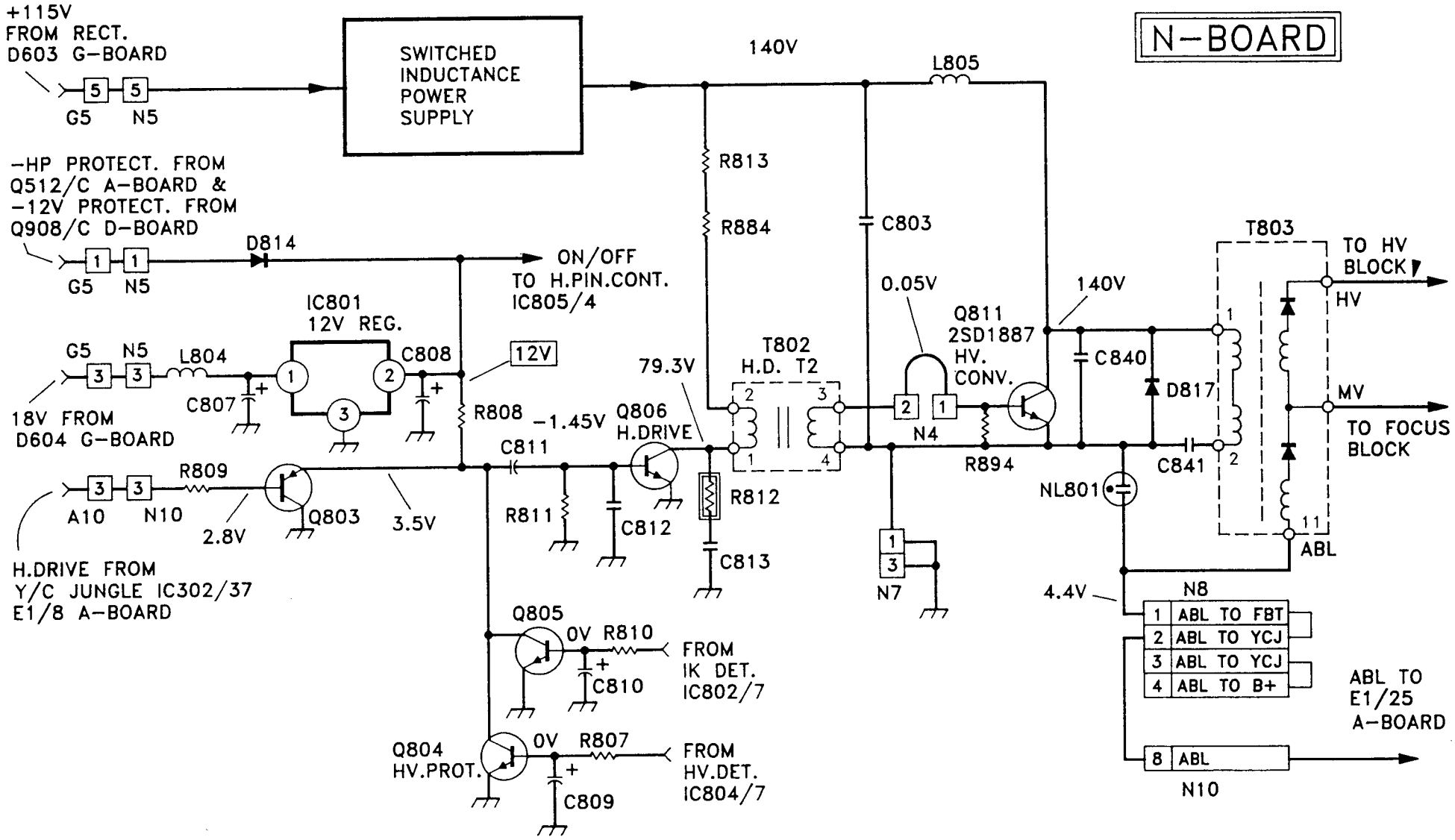
3. Now, check the HV converter circuit for proper operation, using the following procedure:

   A. Check for an H drive signal at buffer Q803 base. If it is not present, a problem may exist in the jungle IC on the A-Board (not shown).

   B. Check for an H drive signal at connector N-4/pins 1 or 2. If the H drive signal is not present the following parts may be defective:

☞ Q803; Q804 or Q805 (collector leakage); C811 (open); Q806 or T802.

   C. Check HV converter transistor Q811 collector for a proper waveform. A missing waveform can be caused by a defective Q811 transistor, by an open T803 primary winding, or by an open L805 coil.



HV CONVERTER

HV Regulation

Overview

The HV regulator circuit regulates the high voltage circuit so as to produce a constant high voltage level. Regulation is maintained by controlling the voltage level of the power supply to the HV converter. This voltage level can be measured at D801 cathode. With the regulator circuit not operating, this voltage level is approximately 117Vdc. Its source is the 115Vdc line from the G-Board, through L803, L801, L802 and D801. With the regulator circuit operating, a switched inductor circuit boosts this voltage to approximately 140Vdc. The switched inductor consists of L802, D801, C803, and Q801.

Operation

The heart of the regulator circuit is IC805. This IC generates a PWM signal at pin 7 which is used to drive the switched inductor circuit. Regulation is maintained by sensing the high voltage level and using it to vary the PWM modulation level. The circuit operates in the following manner:

1. The high voltage level is sensed by tapping off a small portion of the high voltage (7.6Vdc) from the H.V. block and using it to regulate IC805. The output of this sense line, labeled HV REG in the schematic diagram, is buffered by IC803. Its level is reduced by voltage divider R825 and R828 to approximately 3.2Vdc, then input to IC805/pin 1.

2. At IC805/pin 1, the sense voltage is sent to the non-inverting input of an op-amp. Since the input level to the op-amp inverting input pin 14 is fixed at a 3.2 Vdc reference, the op-amp output at pin 13 is controlled only by pin 1.

3. The PWM modulation level at IC805/pin 7 depends on the dc voltage level at pin 13. The higher this voltage, the greater the modulation time (higher duty cycle). Therefore, a change in the high voltage level will result in a change in the PWM duty cycle.

4. From IC805/pin 7 the PWM signal is sent to the base of buffer Q809, then to Q802. This transistor drives the primary of transformer T801.

5. The secondary of T801 drives the base of Q801, which is the switch for the switched inductor circuit. When Q802 conducts, pin 4 of T801 goes negative. This reverse biases Q801, preventing it from conducting. When T802 opens, the collapsing magnetic field of T801 forward biases Q801 into conduction. The longer Q801 is allowed to conduct, the greater the boost voltage will be.

The configuration of the HV regulator circuit is such, that a high voltage increase raises the voltage level at IC805/pin 1. This also raises the voltage level at pin 13, which in turn increases the PWM duty cycle at pin 7. The increased PWM ON time causes Q802 to keep the primary of transformer T801 ON for longer periods, reverse biases Q801 for longer periods, and reduces the boost voltage. The reduced boost voltage lowers the high voltage level. The opposite effect occurs when the high voltage level drops.

IC805 Sub Circuits

IC805/pin 10 syncs the PWM frequency to the horizontal signal. A -HP signal from the horizontal output transformer feeds this pin via C839.

IC805/pin 4 is the ON/OFF control for this IC. A voltage level of 2.3 Vdc or lower shuts off the IC, preventing any voltage boost or regulation.

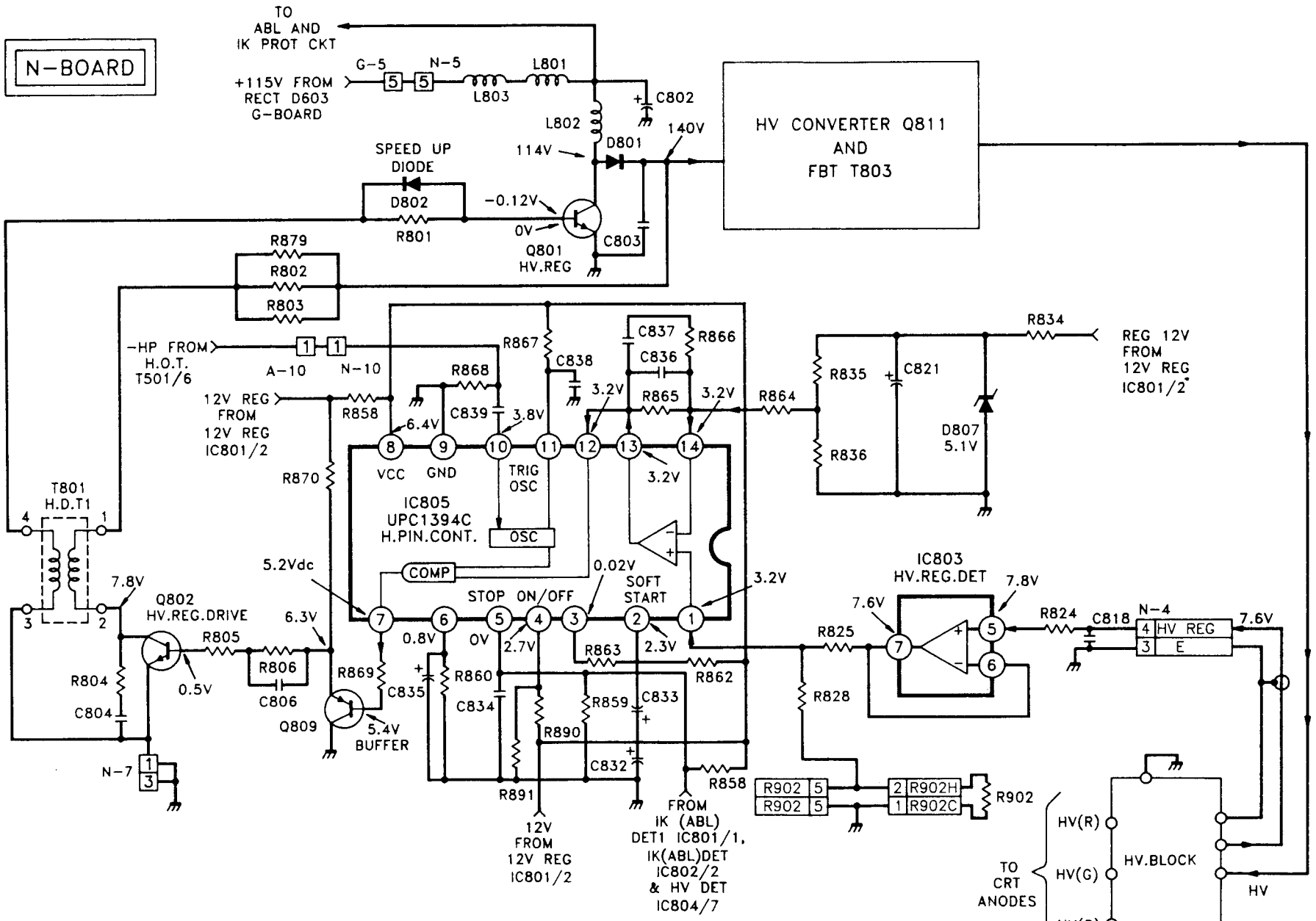
IC805/pin 5 is the STOP pin. This pin is connected to the protect line. It is normally at 0Vdc. A HIGH at this pin shuts off PWM output pulses from pin 7.

C806 and R806, between Q809 and Q802, are waveshapers. D802, at the base of Q801 is a speed up diode. It increases the efficiency of the switched inductor circuit by speeding up the negative pulses to the base of Q801. This cuts off Q801 faster, causing the magnetic field of L802 to collapse faster, thus providing a higher counter EMF.

Power Supply

Buffer transistor Q809 is powered by +12Vdc from IC802 (not shown).

Driver Q802 is powered by the boosted high voltage. The dc path is through the primary of T801.



HV REGULATION

Troubleshooting HV Regulation

A defective HV regulator circuit can cause the following major problems:

1. The brightness level from all three CRTs will be low. This problem may be caused by low or complete absence of high voltage boost.

2. The high voltage protect triggers, shutting off high voltage. When this occurs, audio and video from the monitor terminals will still operate. This problem may be caused when the HV regulator circuit produces excessive high voltage boost, or by other circuits such as the HV converter or the HV protection circuits.

3. The high voltage may not go on. Again, audio and video from the monitor terminal will still operate. This problem may be caused by a defective regulator circuit, by the power supply, or by the HV converter

4. The unit shuts off. This can be caused by a shorted Q801 HV REG transistor. This will cause a short on the power supply +115 line, shutting off the unit.

Low Brightness Checkouts

When the problem is low brightness from all CRTs, the HV regulator should be suspect and checked out. The first step is to determine if the HV boost is operating. Check the voltage level at the cathode end of D801 on the N-Board. If it is between 138 and 150Vdc, then the HV boost is working and is not likely to be the cause of the problem. In this case check the HV converter. If the voltage at the cathode of D801 is between 115 and 138Vdc, then the regulator circuit may be defective. To pin point the problem, the following steps should be taken:

NOTE: (All of the following steps are on the N-Board and the values listed are with the high voltage boost disabled).

1. Unsolder one leg of R802. This breaks the closed loop of the regulator circuit and still allows the regulator and high voltage circuits to operate. (High voltage boost will not occur until the leg has been resoldered) The listed instrument readings should occur.

2. Check IC805/pin 7. It should have a PWM output of 7Vp-p and a voltage level of 3.7Vdc. This indicates that the circuits from the low voltage tap of the HV block through the IC are working properly. In this event go to step 8. A lack of PWM signals, or a higher DC voltage level will prevent the boost from operating. In this event, continue with the next steps. A lower dc level cannot occur with this symptom, as it will normally cause excessive HV boost and trigger the protect circuit.

3. Check the low voltage tap from the HV block at connector N-4/pin 4. It should be 6Vdc. A higher value can be caused by a defective HV block. It will prevent normal boosting. A lower value cannot occur with this symptom, as it will cause excessive boost and trigger the protection.

4. Check the voltage at IC805/pin 1. It should be 2.5Vdc. A higher voltage may be caused by a defect in IC805 or IC803, or in voltage divider R825, R828, R902. It will prevent normal boosting. A lower value will cause excessive boost and trigger the protection.

5. Check the voltage at IC805/pin 14. It should be 2.84Vdc. If it is different, check the values of R864, R835 and R836, and the voltage at zener D807. The zener voltage should be 5.1Vdc. If the resistors and zener are OK, IC805 may be defective.

6. Check the voltage at IC805/pins 12 or 13. The voltage should be approximately 0.13V dc. If it differs, the IC may be defective.

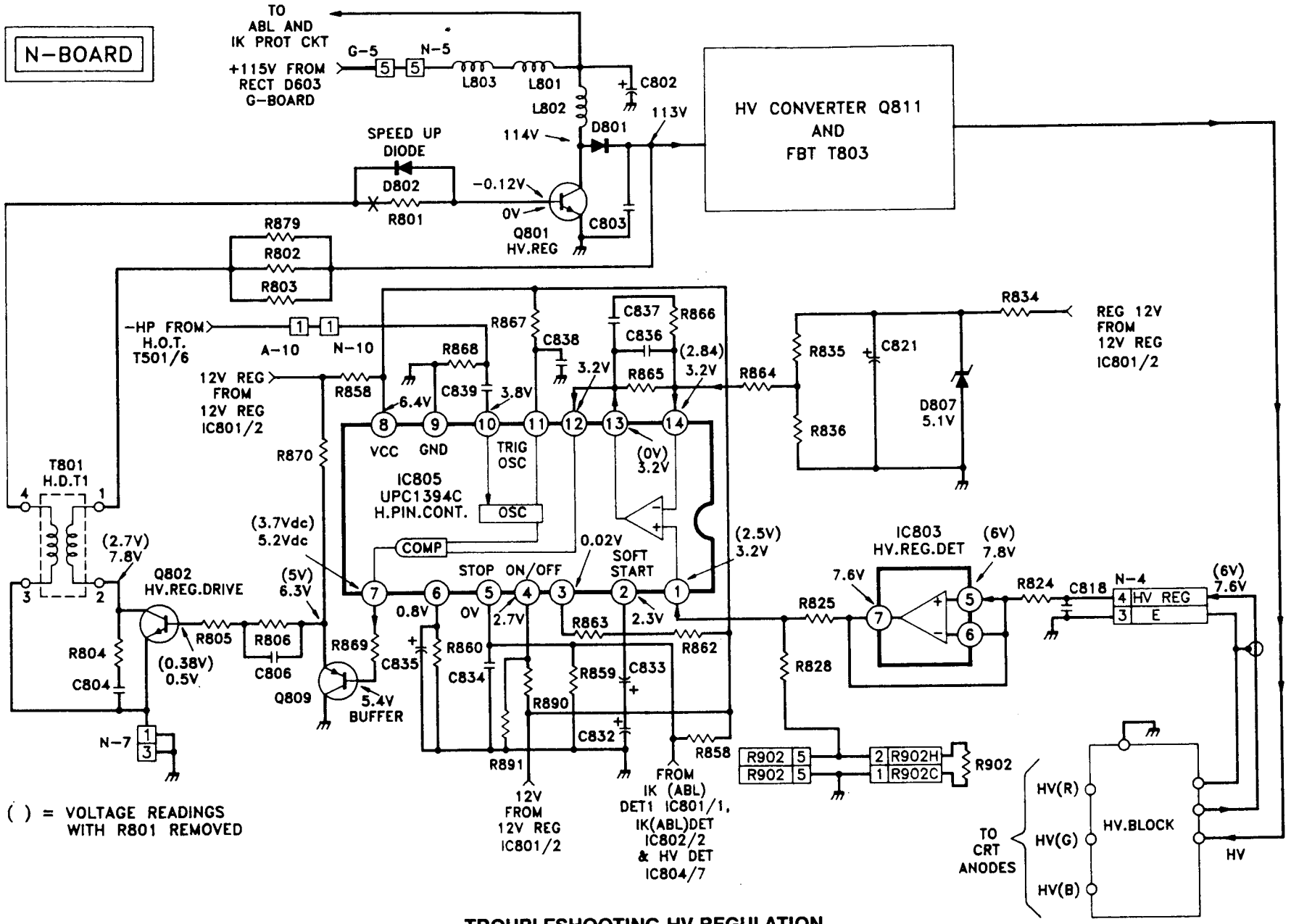
7. Check the rest of IC805 for correct voltages. They should be as indicated in the diagram. If they are incorrect, either the IC or the circuit at the respective pin may be defective.

8. If PWM signals are present at IC805/pin 7 and the DC voltage is as indicated, then do the following:

   A. Reconnect R801 on the N-Board.

   B. With an oscilloscope, signal trace the PWM signals to the point where they are lost. The signals should appear as shown in the diagram. The components to follow are:

* Buffer Q809, waveshapers R805, R806 and C806, Q802, T801, R801 and D802, Q801.



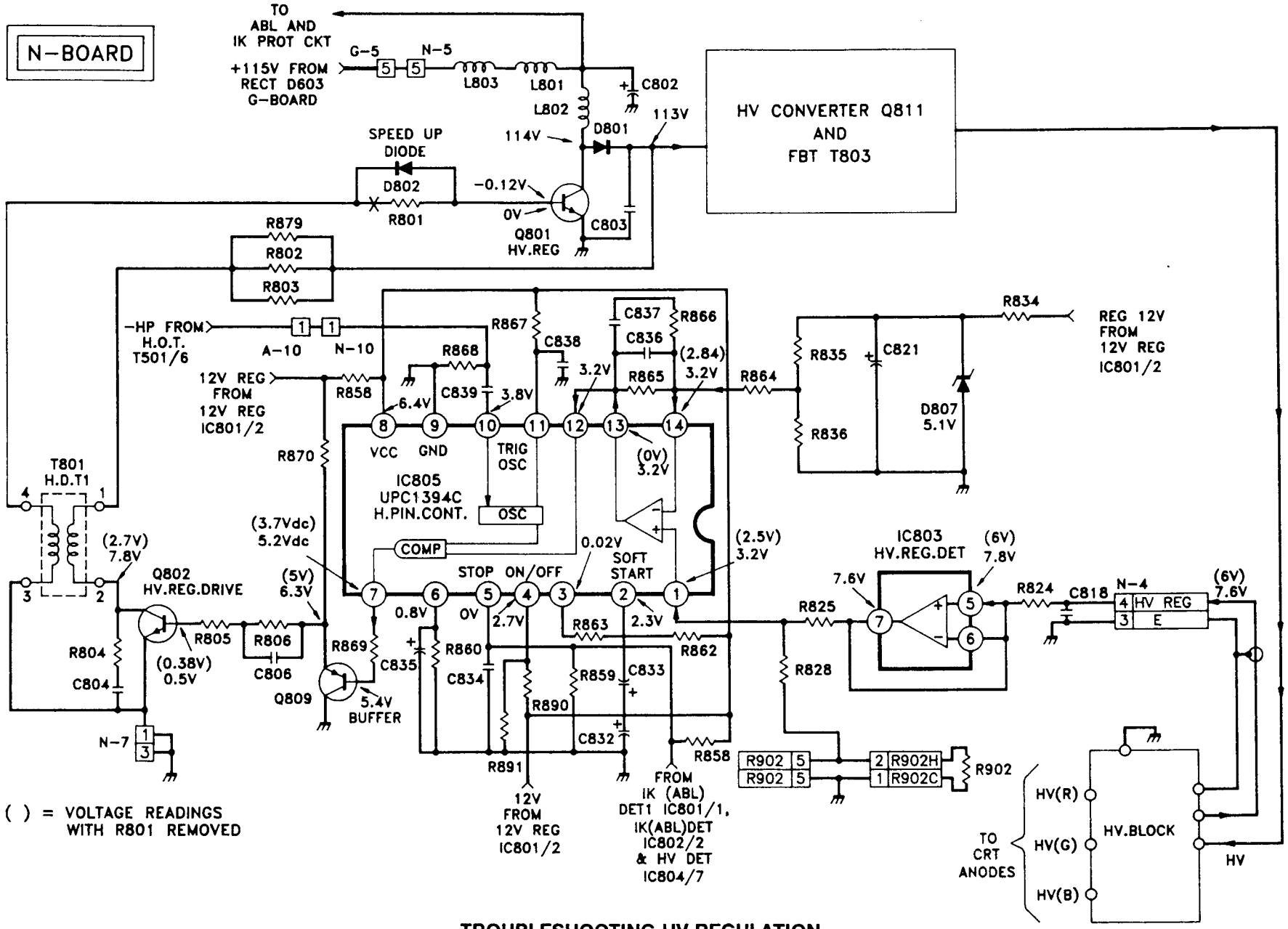
TROUBLESHOOTING HV REGULATION

Unlit CRTs

Use the following procedure to determine if unlit CRTs are caused by the HV regulator circuit or by another circuit:

1. Measure the voltage at the cathode of D801. If 115Vdc is missing, the problem may be an open L803, L801, L802, or D801 on the N-Board, or a defective power supply.
2. If 115Vdc is present, check IC805/pin 5 for 0.7Vdc. If present, the problem is HV protection triggering. If 0.7Vdc is missing, the HV converter may be defective.

A short in the +115 power supply line may be caused by a shorted Q801 HV regulator transistor in this circuit.



TROUBLESHOOTING HV REGULATION

HV Shutdown

The HV shutdown circuit monitors the high voltage circuit for dangerous conditions. In the event these conditions occur, the HV shutdown circuit will shut down the high voltage.

The following high voltage conditions are sensed: Excessive high voltage from the HV block, excessive boost voltage from the HV booster, and excessive HV current. The operation of each of these shutdown circuits will be explained separately.

Operation

Excessive High Voltage

Normal high voltage is 31.5kV. The high voltage level is sense by monitoring the HV protect pin of the HV block at IC804/pin 3. The voltage at this pin consists of the HV divided down to a low level. During normal operation the voltage at this point is 7.7Vdc. The voltage is buffered by IC803 (1/2), and reduced by voltage divider R893, R829, R900 and R901 to 4.8Vdc, and input to comparator IC804 (1/2)/pin 3. Since this voltage is less than the comparator threshold level (5.1Vdc), the comparator output (pin 1) will be LOW. The output of comparator IC804 (2/2) will also be LOW.

When the HV level exceeds 33.5kV, the voltage level at comparator IC804 (1/2)/pin 3 will rise above the 5.1Vdc comparator threshold level, causing the comparator output (pin 3) to go HIGH (12Vdc). The HIGH is sent to another comparator, IC804 (2/2)/pin 5. Since the 12Vdc HIGH is greater than the threshold of this comparator, its output (pin 7) will also go HIGH. This HIGH affects two circuits:

* It turns ON switch Q804. This shunts to ground the HD signals at Q803/C, preventing the HV converter from operating.

* It forward biases D810, sends the HIGH to the STOP pin of PWM generator IC805, cutting off the IC and preventing any HV boost operation.

D808 across comparator IC804 (2/2) acts as a latch. When pin 5 of the comparator goes above 5.1Vdc, pin 7 will go to 12Vdc. This forward biases D808, forcing pin 5 to a 11.4Vdc potential. This condition is maintained by the diode until power shut off. Therefore, once the high voltage protect is triggered, it will remain so until power is shut off.

Excessive Boost +B

The boost +B voltage is sensed by comparator IC802/ (1/2). The boosted +B voltage is sent through voltage divider R816 through R820. During normal boost operation the voltage at IC802/pin 3 is approximately 3.4Vdc. Since this is below the comparator threshold level (5.1Vdc), the comparator output (pin 1) will be LOW.

If the boost level exceeds 225Vdc, the voltage at comparator IC802/pin 3 will exceed the threshold level, causing pin 1 to go HIGH (12Vdc). This forward biases D804, and sends the HIGH through R860 to the STOP pin of PWM generator IC805, cutting off the IC and preventing any HV boost operation.

The boost +B protect does not latch.

Over Current Protect

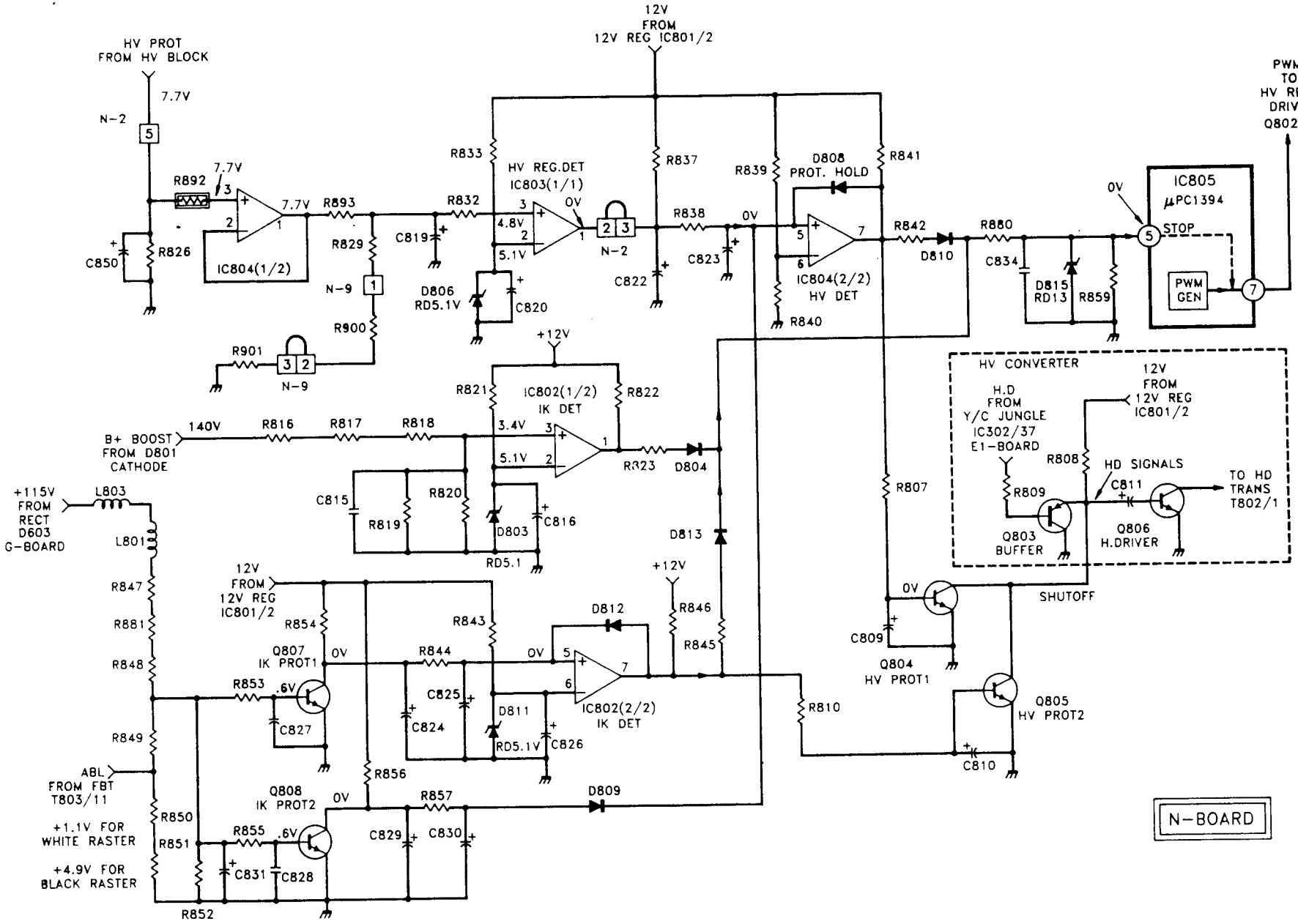
Excessive HV anode current is sensed by Q807 and Q808. The base bias for these two transistors is set by the fixed +115Vdc line, by the variable ABL line, and by the voltage divider consisting of R847 through R851 and R881. During normal operation, the ABL voltage level varies from 4.9Vdc for a dark screen to 1.1Vdc for a bright screen. The bias configuration is such, that during normal operation Q807 and Q808 are always biased ON. If the HV current exceeds 3.4mA, the ABL line will go sufficiently negative for Q707 and Q708 to turn OFF. These transistors trigger shutdown in different areas of the shutdown circuit. The effect of Q807 will be described first, then the effect of Q808.

Q807 Effect:

1. When an over-current condition cuts Q807 OFF, its collector is pulled HIGH (12Vdc) by R854.

2. The HIGH goes through the pi filter consisting of C824 C825 and R844 to the non-inverting input (pin 5) of comparator IC802 (2/2). Normally, the 5.1Vdc threshold level of the comparator keeps its output (pin 7) LOW.

3. When over-current condition places a 12Vdc potential on the non-inverting input of the comparator, the threshold voltage is exceeded, and its output toggles HIGH. D812 latches the comparator output HIGH.


HV PROT
FROM HV BLOCK
7.7V
N-2
5
R892
7.7V
3
2
1
IC804(1/2)
7.7V
R893
R829
N-9
1
R900
C850
R826
C819
R832
R833
HV REG.DET
IC803(1/1)
3
4.8V
2
5.1V
1
0V
2 3
N-2
R837
R838
0V
C822
C823
R839
D808
PROT. HOLD
R841
5
6
7
IC804(2/2)
HV DET
R840
R842
D810
R880
C834
D815
RD13
R859
0V
5
IC805
μPC1394
STOP
PWM
GEN
7
PWM
TO
HV REG
DRIVE
Q802/B
12V
FROM
12V REG IC801/2
D806
RD5.1V
C820
+12V
R901
3 2
N-9
R821
IC802(1/2)
IK DET
R822
140V
R816
R817
R818
B+ BOOST
FROM D801
CATHODE
3.4V
3
5.1V
2
1
R823
D804
C815
R819
R820
D803
C816
RD5.1
+115V
FROM
RECT
D603
G-BOARD
L803
L801
R847
R881
R848
R849
ABL
FROM FBT
T803/11
+1.1V FOR
WHITE RASTER
+4.9V FOR
BLACK RASTER
R850
R851
R852
12V
FROM
12V REG
IC801/2
R854
Q807
IK PROT1
0V
R853
.6V
C827
R843
R844
0V
C825
C824
D811
RD5.1V
C826
D812
5
6
7
IC802(2/2)
IK DET
+12V
R846
R845
R856
Q808
IK PROT2
0V
R855
.6V
C831
C828
R857
C829
C830
D809
D813
R807
R810
HV CONVERTER
H.D
FROM
Y/C JUNGLE
IC302/37
E1-BOARD
12V
FROM
12V REG
IC801/2
R808
HD SIGNALS
C811
TO HD
TRANS
T802/1
R809
Q803
BUFFER
Q806
H.DRIVER
SHUTOFF
0V
C809
Q804
HV PROT1
Q805
HV PROT2
C810
N-BOARD

HV SHUTDOWN

4. The HIGH at the comparator output is routed in two directions. These are:

    1. Through R845, D813 and R860 to the STOP pin of IC805. This turns cuts off the PWM pulses and the +B boost voltage.

    2. Through R810 to the base of Q805. This turns Q805 ON, shunting the HD signals from the emitter of Q803 to ground, preventing the HV converter from operating.

Q808 Effect:

1. When an over current condition cuts Q808 OFF, its collector is pulled HIGH (12Vdc) by R856.

2. The HIGH goes through the pi filter consisting of C829 C830 and R857, through D809, to the non-inverting input pin 5 of comparator IC804 (2/2). Normally, the 5.1Vdc threshold level of the comparator keeps its output (pin 7) LOW.

3. When an over-current condition places a 12Vdc potential on the non-inverting input of the comparator, the threshold voltage is exceeded, and its output toggles HIGH. D808 latches the comparator output HIGH.

4. The HIGH at the comparator output is routed in two directions. These are:

    1. Through R842 D810 and R860 to the STOP pin 5 of IC805. This turns cuts off the PWM pulses and the +B boost voltage.

2. Through R807 to the base of Q804. This turns Q804 ON, shunting the HD signals from the emitter of Q803 to ground, preventing the HV converter from operating.

Troubleshooting

Warning: Do not tamper with the unit in a manner which will override the HV shutdown protection. Doing so defeats the purpose of shutdown and can result in dangerous conditions to the technician and user. Determine if the defect is in the HV protect circuit, or if it is operating normally and being triggered by excessive HV voltage or current conditions. Then do the following:

1. Shut the unit OFF and disconnect connector N-4. Shutting the unit OFF reset's the HV shutdown circuit. Removing the connector shuts down the HV circuit.

2. Turn the unit ON and check the base of Q807 and Q808 for 0Vdc or 0.6Vdc.

    A. 0Vdc indicates that the HV shutdown is working properly and that the problem is excessive HV or current. In this case:

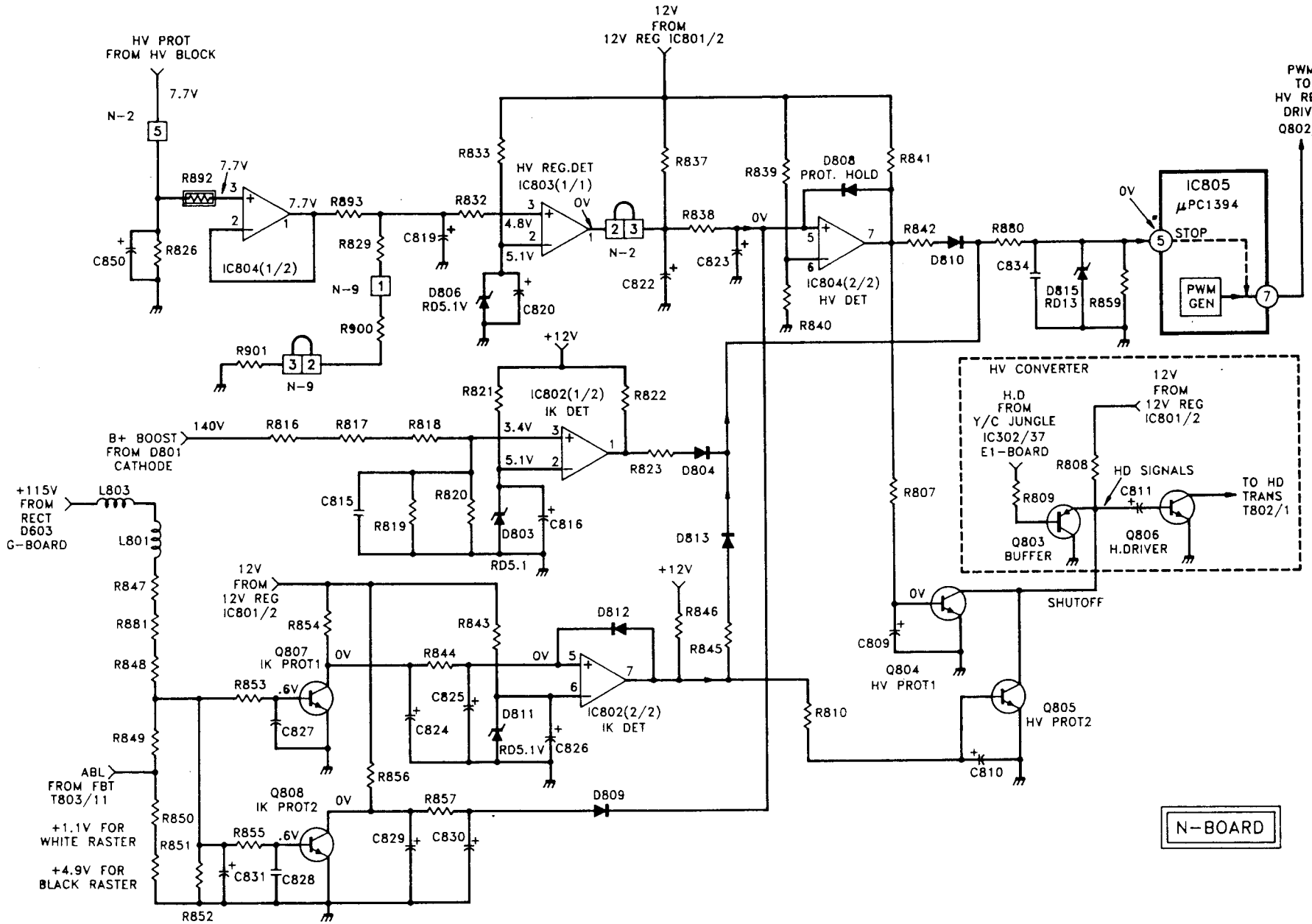
        1. Turn OFF the unit, reconnect the connector, then turn ON the unit.

        2. Check the base voltages of Q804 and Q805 for either 0Vdc or 0.6Vdc, then refer to the table below to determine which circuit is triggering protection.

        3. Refer to the appropriate troubleshooting section.

    B. 0.6Vdc at the base of either or both Q807 and Q808 indicates that the HV shutdown circuit in not working properly. In this case, use standard troubleshooting techniques and work backwards from these transistors to determine the defective component.

Q804 Base	Q805 Base	Protect Trigger Cause
0Vdc	0Vdc	IC802
0Vdc	0.6Vdc	Q807, IC802
0.6Vdc	0Vdc	Excessive HV, HV Regulator or Converter
0.6Vdc	0.6Vdc	Excessive current, ABL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R892
7.7V
3
2
IC804(1/2)
7.7V
R893
R829
N-9
1
R900
C850
R826
C819
R832
R833
HV REG.DET
IC803(1/1)
4.8V
5.1V
0V
2
3
1
N-2
D806
RD5.1V
C820
12V
FROM
12V REG IC801/2
R837
R838
0V
C822
C823
R839
D808
PROT. HOLD
R841
IC804(2/2)
HV DET
R840
R842
D810
R880
C834
D815
RD13
R859
0V
IC805
μPC1394
STOP
PWM
GEN
PWM
TO
HV REG
DRIVE
Q802/B
R901
3
2
N-9
+12V
R821
IC802(1/2)
IK DET
R822
140V
R816
R817
R818
B+ BOOST
FROM D801
CATHODE
3.4V
5.1V
R823
D804
C815
R819
R820
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HV CONVERTER
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E1-BOARD
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12V REG
IC801/2
R808
HD SIGNALS
C811
TO HD
TRANS
T802/1
R809
Q803
BUFFER
Q806
H.DRIVER
SHUTOFF
+115V
FROM
RECT
D603
G-BOARD
L803
L801
R847
R881
R848
R849
ABL
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+4.9V FOR
BLACK RASTER
R850
R851
R852
12V
FROM
12V REG
IC801/2
R854
Q807
IK PROT1
0V
R853
.6V
C827
R843
R844
0V
C825
C824
D811
RD5.1V
C826
D812
+12V
R846
R845
IC802(2/2)
IK DET
D813
R807
R810
0V
C809
Q804
HV PROT1
Q805
HV PROT2
C810
R856
Q808
IK PROT2
0V
R855
.6V
C831
C828
R857
C829
C830
D809
N-BOARD

HV SHUTDOWN

POWER DISTRIBUTION