FILE NO. SM-CTV-O-228

TV/DVD COMBO

SERVICE MANUAL

MODEL NO. MTV-DV05

CHASSIS NO. CN-12DV

Please read this manual carefully before service.

TABLE OF CONTENTS

SERVICE SAFETY INSTRUCTIONS

WARNING: BEFORE SERVICING THIS CHASSIS, READ THE "X-RAY RADIATION PRECAUTION", "SAFETY PRECAUTIONS" AND "PRODUCT SAFETY NOTICE" INSTRUCTION BELOW.

X-RAY RADIATION PRECAUTION

1. The EHT must be checked every time the TV is serviced to ensure that the CRT does not emit X-ray radiation as result of excessive EHT voltage. The maximum EHT voltage permissible in any operating circumstances must not exceed the rated value. When checking the EHT, use the High Voltage Check procedure in this manual using an accurate EHT voltmeter.
2. The only source of X-RAY radiation in this TV is the CRT. The TV minimizes X-RAY radiation, which ensures safety during normal operation. To prevent X-ray radiation, the replacement CRT must be identical to the original fitted as specified in the parts list.
3. Some components used in this TV have safety related characteristics preventing the CRT from emitting X-ray radiation. For continued safety, replacement component should be made after referring the PRODUCT SAFETY NOTICE below.
4. Service and adjustment of the TV may result in changes in the nominal EHT voltage of the CRT anode. So ensure that the maximum EHT voltage does not exceed the rated value after service and adjustment.

SAFETY PRECAUTION

WARNING: REFER SERVICING TO QUALIFIED SERVICE PERSONNEL ONLY.

1. The TV has a nominal working EHT voltage. Extreme caution should be exercised when working on the TV with the back removed.

1.1 Do not attempt to service this TV if you are not conversant with the precautions and procedures for working on high voltage equipment.

1.2 When handling or working on the CRT, always discharge the anode to the TV chassis before removing the anode cap in case of electric shock.

1.3 The CRT, if broken, will violently expel glass fragments. Use shatterproof goggles and take extreme care while handling.

1.4 Do not hold the CRT by the neck as this is a very dangerous practice.

2. It is essential that to maintain the safety of the customer all power cord forms be replaced exactly as supplied from factory.
3. Voltage exists between the hot and cold ground when the TV is in operation. Install a suitable isolating transformer of beyond rated overall power when servicing or connecting any test equipment for the sake of safety.
4. When replacing ICs, use specific tools or a static-proof electric iron with small power (below 35W).
5. Do not use a magnetized screwdriver when tightening or loosing the deflection yoke assembly to avoid electronic gun magnetized and decrement in convergence of the CRT.
6. When remounting the TV chassis, ensure that all guard devices, such as nonmetal control buttons, switch, insulating sleeve, shielding cover, isolating resistors and capacitors, are installed on the original

place.

7. Replace blown fuses within the TV with the fuse specified in the parts list.
8. When replacing wires or components to terminals or tags, wind the leads around the terminal before soldering. When replacing safety components identified by the international hazard symbols on the circuit diagram and parts list, it must be the company-approved type and must be mounted as the original.
9. Keep wires away from high temperature components.

PRODUCT SAFETY NOTICE

CAUTION: FOR YOUR PROTECTION, THE FOLLOWING PRODUCT SAFETY NOTICE SHOULD BE READ CAREFULLY BEFORE OPERATING AND SERVICING THIS TV SET.

1. Do not slap or beat the cabinet or CRT, since this may result in fire or explosion.
2. Never allow the TV sharing a plug or socket with other large-power equipment. Doing so may result in too large load, thus causing fire.
3. Do not allow anything to rest on or roll over the power cord. Protect the power cord from being walked on, modified, cut or pinched, particularly at plugs.
4. Do not place any objects, especially heavy objects and lightings, on top of the TV set. Do not install the TV near any heat sources such as radiators, heat registers, stove, or other apparatus that produce heat.
5. Service personnel should observe the SAFETY INSTRUCTIONS in this manual during use and servicing of this TV set. Otherwise, the resulted damage is not protected by the manufacturer.
6. Many electrical and mechanical components in this chassis have special safety-related characteristics. These characteristics are often passed unnoticed by a visual inspection and the X-ray radiation protection afforded by them cannot necessarily be obtained by using replacements rated at higher voltages or wattage, etc. Components which have these special safety characteristics in this manual and its supplements are identified by the international hazard symbols on the circuit diagram and parts list. Before replacing any of these components read the parts list in this manual carefully. Substitute replacement components which do not have the same safety characteristics as specified in the parts list may create X-ray radiation.

SAFETY SYMBOL DESCRIPTION

The lightning symbol in the triangle tells you that the voltage inside this product may be strong enough to cause an electric shock. Extreme caution should be exercised when working on the TV with the back removed.

This is an international hazard symbol, telling you that the components identified by the symbol have special safety-related characteristics.

FDA This symbol tells you that the critical components identified by the FDA marking have special safety-related characteristics.

UL This symbol tells you that the critical components identified by the UL marking have special safety-related characteristics.

SERVICE SAFETY INSTRUCTIONS FOR DVD UNIT

1. Never allow unqualified personnel to remove and service the DVD130A modules.
2. The unit will generate static. Extreme care should be taken when servicing the modules DVD130A modules.
3. Never touch the laser pickup head.
4. When this unit is connected to the mains, do not bring your eyes into the laser pickup head or try to look into the disc tray of any of the opening. Looking into a laser may cause eyes damaged.
5. Ensure that leads of DVD130A are connected correctly.
6. When the unit is powered on, do not connect or disconnect the leads of DVD130A
7. Before power on, ensure each operating voltage coincides with the marking on the PCB and make sure no short circuit exits on PCB.
8. Do not use scratched, warped or repaired discs.

MAINTENANCE

1. Place the unit on a stable stand or base that is of adequate size and strength to prevent the is from being accidentally tipped over, pushed off, or pulled off. Do not place the set near or over a radiator or heat register, or where it is exposed to direct sunlight.
2. Do not install the unit set in a place exposed to rain, water, excessive dust, mechanical vibrations or impacts.
3. Allow enough space (at least 10cm) between the unit and wall or enclosures for proper ventilation.
4. Slots and openings in the cabinet should never be blocked by clothes or other objects.
5. Please power off the unit set and disconnect it from the wall immediately if any abnormal phenomenon occurs, such as bad smell, belching smoke, sparkling, abnormal sound, no picture/sound/raster. Hold the plug firmly when disconnecting the power cord.
6. Unplug the unit set from the wall outlet before cleaning or polishing it. Use a dry soft cloth for cleaning the exterior of the unit set or CRT screen. Do not use liquid cleaners or aerosol cleaners.

ADJUSTMENTS

SET-UP ADJUSTMENTS

The following adjustments should be made when a complete realignment is required or a new picture tube is installed.

Perform the adjustments in the following order:

1. Color purity
2. Convergence
3. White balance

Notes:

① The purity/convergence magnet assembly and rubber wedges need mechanical positioning.

② For some picture tubes, purity/convergence adjustments are not required.

1. Color Purity Adjustment

Preparation:

Before starting this adjustment, adjust the vertical sync, horizontal sync, vertical amplitude and focus.

1.1 Face the TV set north or south.

1.2 Connect the power plug into the wall outlet and turn on the main power switch of the TV set.

1.3 Operate the TV for at least 15 minutes.

1.4 Degauss the TV set using a specific degaussing coil.

1.5 Set the brightness and contrast to maximum.

1.6 Counter clockwise rotate the R/B low brightness potentiometers to the end and rotate the green low brightness potentiometer to center.

1.7 Receive green raster pattern signals.

1.8 Loosen the clamp screw holding the deflection yoke assembly and slide it forward or backward to display a vertical green zone on the screen. Rotate and spread the tabs of the purity magnet around the neck of the CRT until the green zone is located vertically at the center of the screen.

1.9 Slowly move the deflection yoke assembly forward or backward until a uniform green screen is obtained.

1.10 Tighten the clamp screw of the assembly temporarily. Check purity of the red raster and blue raster until purity of the three rasters meets the requirements.

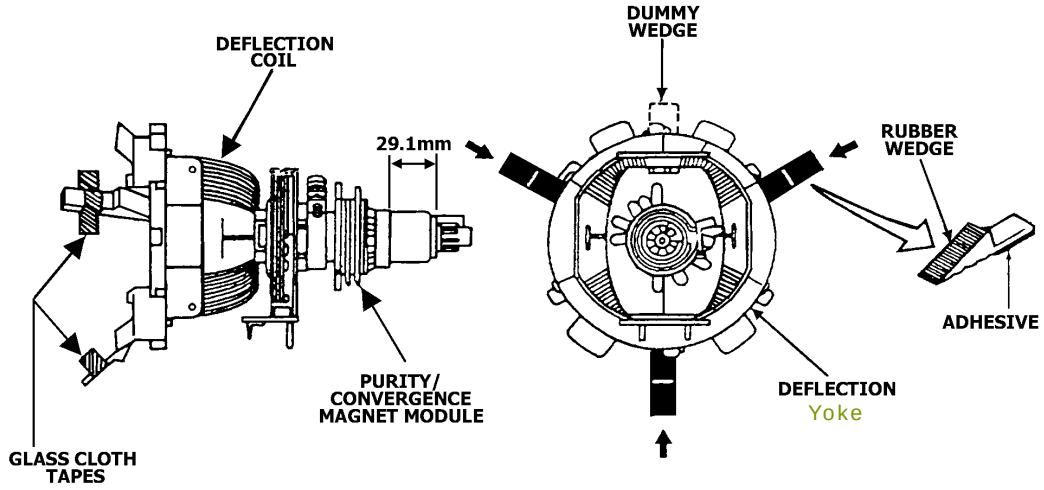


Fig. 1

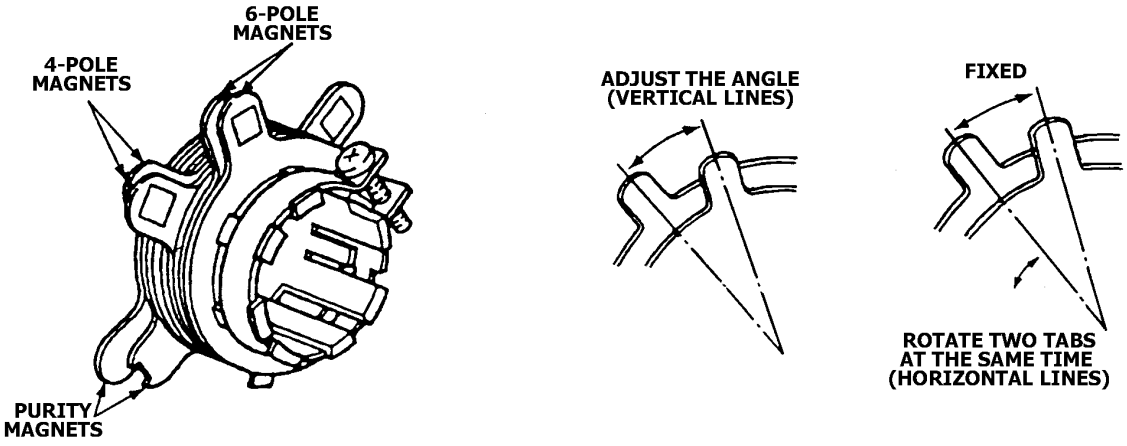


Fig. 2

2. Convergence Adjustment

Preparation:

Before attempting any convergence adjustment, the TV should be operated for at least 15 minutes.

2.1 Center convergence adjustment

2.1.1 Receive dot pattern.

2.1.2 Adjust the brightness/contrast controls to obtain a sharp picture.

2.1.3 Adjust two tabs of the 4-pole magnet to change the angle between them and red and blue vertical lines are superimposed each other on the center of the screen.

2.1.4 Turn both tabs at the same time keeping the angle constant to superimpose red and blue horizontal on the center of the screen.

2.1.5 Adjust two tabs of the 6-pole magnet to superimpose red/blue line and green line.

2.1.6 Remember red and blue movement. Repeat steps 2.1.3～2.1.5 until optimal convergence is obtained.

2.2 Circumference convergence adjustment

2.2.1 Loosen the clamp screw holding the deflection yoke assembly and allow it tilting.

2.2.2 Temporarily put the first wedge between the picture tube and deflection yoke assembly. Move front of the deflection yoke up or down to obtain better convergence in circumference. Push the mounted wedge in to fix the yoke temporarily.

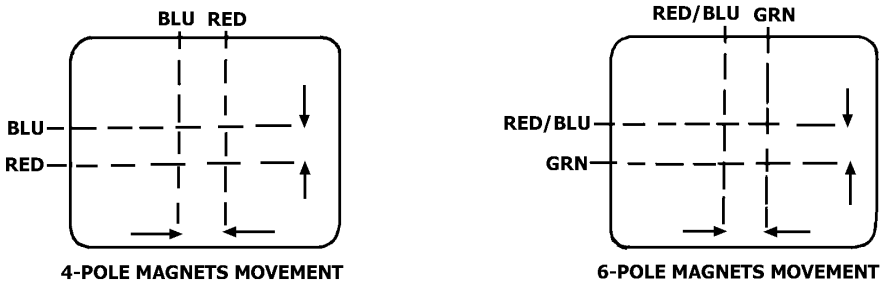
2.2.3 Put the second wedge into bottom.

2.2.4 Move front of the deflection yoke to the left or right to obtain better convergence in circumference.

2.2.5 Fix the deflection yoke position and put the third wedge in either upper space. Fasten the deflection yoke assembly on the picture tube.

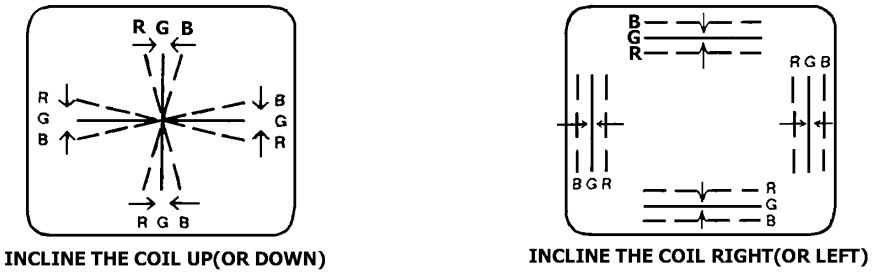
2.2.6 Detach the temporarily mounted wedge and put it in either upper space. Fasten the deflection yoke assembly on the picture tube.

2.2.7 After fastening the three wedges, recheck overall convergence and ensure to get optimal convergence. Tighten the lamp screw holding the deflection yoke assembly.



4-pole Magnet Movement 6-pole Magnet Movement

Center Convergence by Convergence Magnets



Incline the Yoke Up (or Down) Incline the Yoke Right (or Left)

Circumference Convergence by DEF Yoke

Fig.3

3. White Balance Adjustment

Generally, white balance adjustment is made with professional equipment. It's not practical to get good white balance only through manual adjustment. For TVs with I^2C bus control, change the bus data to adjust white balance.

CIRCUIT ADJUSTMENTS

Preparation:

Circuit adjustments should be made only after completion of set-up adjustments.

Circuit adjustments can be performed using the adjustable components inside the TV set. For TVs with I^2C bus control, first change the bus data.

1. Degaussing

A degaussing coil is built inside he TV set. Each time the TV is powered on, the degaussing coil will automatically degauss the TV. If the TV is magnetized by external strong magnetic field, causing color spot on the screen, use a specific degausser to demagnetize the TV in the following ways. Otherwise, color distortion will be exist on the screen.

1.1 Power on the TV set and operate it for at least 15 minutes.

1.2 Receive red full-field pattern.

1.3 Power on the specific degausser and face it to the TV screen.

1.4 Turn on the degausser. Slowly move it around the screen and slowly take it away from the TV.

1.5 Repeat the above steps until the TV is degaussed completely.

2. Supply Voltage Adjustment

Caution: +B voltage has close relation to high voltage. To prevent X-ray radiation, set +B voltage to the rated voltage.

2.1 Make sure that the supply voltage is within the range of the rated value.

2.2 Connect a digital voltmeter to the +B voltage output terminal VD891 of the TV set. Power on the TV and set the brightness and sub-brightness to minimum.

2.3 Regulate voltage adjustment components on the power PCB to make the voltmeter read 115±1V .

3. High Voltage Inspection

Caution: No high voltage adjustment components inside the chassis. Please perform high voltage inspection in the following ways.

3.1 Connect a precise static high voltmeter to the second anode (inside the high voltage cap) of the picture tube.

3.2 Plug in the supply socket (120V, AC) and turn on the TV. Set the brightness and contrast to minimum (0 μA).

3.3 The high voltage reading should be less than the EHT limitation.

3.4 Change the brightness from minimum to maximum, and ensure high voltage not beyond the limitation in any case.

Nominal EHT voltage: 22±1KV Limited EHT voltage: 25KV

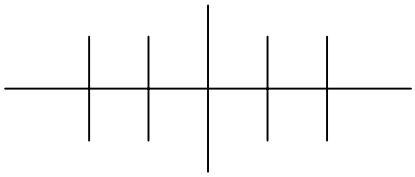
4. Focus Adjustment

Caution: Dangerously high voltages are present inside the TV. Extreme caution should be exercised when working on the TV with the back removed.

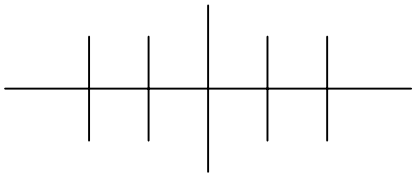
4.1 After removing the back cover, look for the FBT on the main PCB. There should be a FCB on the FBT.

4.2 Power on the TV and preheat it for 15 min.

4.3 Receive a normal TV signal. Rotate knob of the FCB until you get a sharp picture.



Before Adjusting



After Adjusting

5. Safety Inspection

5.1 Inspection for insulation and voltage-resistant

Perform safety test for all naked metal of the TV. Supply high voltage of 3000V AC, 50Hz (limit current of 10mA) between all naked metal and cold ground. Test every point for 3 seconds. and ensure no arcing and sparking.

5.2 Requirements for insulation resistance

Measure resistance between naked metal of the TV and feed end of the power cord to be infinity with a DC-500 high resistance meter and insulation resistance between the naked metal and degaussing coil to be over 20MΩ.

6. DESIGN/SERVICE mode

6.1 To enter the DESIGN/USER SERVICE (S) mode

Set the volume to 0. Then press the MUTE key on the remote control and on the TV at the same time for over 2 seconds. In the S mode, press the POWER key to quit the S mode.

6.2 Adjustments and bus data

Table 1 Bus Data

Item	Symbol Description	Bus Data
MENU.00		
V.POSITION	VERTICAL POSITION	40
H.PHASE	HORIZONTAL PHASE	15
V.SIZE	VERTICAL SIZE	60
V.SC	VERTICAL S-CORRECTION	18
V.LINE	VERTICAL LINE	19
V.SIZE CMP	VERTICAL SIZE COMPENSATION	7
MENU.01		
SUB.BIAS	SUB-BRIGHT	63
SUB.CONT	SUB-CONTRAST	31
V.KILL	VERTICAL KILL	0

(continued)

RF.AGC	RF AGC	20
R.BIAS	RED BIAS	130
G.BIAS	GREEN BIAS	130
B.BIAS	BLUE BIAS	130
R.DRIVE	RED DRIVE	75
G.DRIVE	GREEN DRIVE	15
B.DRIVE	BLUE DRIVE	75
MENU.02		
SECAM B DC	SECAM B-Y	0
SECAM R DC	SECAM R-Y	0
H.APC GAIN	HORIZONTAL APC GAIN	0
SYNC.KIL	SYNC KILL	0
H.BLK.L	HORIZONTAL BLANKING LEFT	4
H.BLK.R	HORIZONTAL BLANKING RIGHT	4
CROS.B/W	CROSSHATCH BLACK/WHITE	0
VIDEO.LVL	VIDEO LEVEL	7
FM.LEVEL	FM LEVEL	16
MENU.03		
FM.MUTE	FM MUTE	0
AUDIO.MUTE	AUDIO MUIE	0
VIDEO.MUTE	VIDEO MUTE	0
DEEM.TC	DE-EMPHASIS TIME CONSTANT	0
SND.TRAP	SOUND TRAP	0
MENU.04		
SUB.COLOR	SUB COLOR	63
SUB.TINT	SUB TINT	32
SUB.SHARP	SUB SHARP	63
AUTO FLESH	AUTOMATIC FLESH	0
CORING.GAN	CORING GAIN	1
C.EXT	EXTERNAL CHROMA	0
C.BYPASS	CHROMA　BAND-PASS BYPASS	0
C.KILL ON	COLOR KILL ON	0
MENU.05		
FIL.SYS	FILTER SYSTEM：SELECT Y/C FILTER MODE	1
COLOR.SYS	COLOR SYSTEM	5
VOL.FIL	VOLUME FILTER	0
VIF.SYS	VIF SYSTEM	0
SIF.SYS.SW	SIF SYSTEM SWITCH	0
VIDEO.SW	VIDEO SWITCH	1
MENU.06		
R/B G.BAL	R-Y/B-Y GAIN BALANCE	7
R/B ANGLE	R-Y/B-Y ANGLE	9
CD MODE	VERTICAL COUNTDOWN MODE	0

(continued)

GREY MODE	GREY MODE	0
V.SETUP	VERTICAL SETUP	1
MENU.07		
BLANK.DEF	BLANK DEFEAT	0
BRT.ABL.TH	BRIGHT ABL THRESHOLD	7
RGB TEMP	RGB TEMPERATURE SWITCH	1
BRT.ABL.DF	BRIGHT ABL DEFEAT	0
MID.STP.DF	BRIGHT MID STOP DEFEAT	0
FBP.BLK.SW	FLYBACK PULSES（HORIZONTAL）BLANKING SWITCH	0
MENU.08		
DIGITAL.OSD	DIGITAL OSD MODE	0
OSD.CONT	OSD CONTRAST CONTROL	10
OSD.CONTST	OSD CONTRAST TEST	0
OSD.H.POS	OSD HORIZONTAL POSITION	22
MENU.09		
H.FREQ	HORIZONTAL FREQUENCY	46
FM.GAIN	FM GAIN	0
C.KILL.OFF	COLOR KILL OFF	0
AUDIO.SW	AUDIO SWITCH	0
T.DISBLE	TEST MODE SWITCH DISABLE	1
MENU.10		
G/Y ANGLE	G/Y ANGLE	0
COL KIL OP	COLOR KILLER OPERATIONAL LEVEL	5
CBCR-IN	YC_BC_R INPUT	1
Y-APF	YC_BC_R MODE，ALL PASS FILTER MODE	0
PRE SHOOT	PRE-SHOOT WIDTH	0
WPL OPE	WHITE PEAK LIMITER LEVEL OPERATE	0
DC REST	LUMA DC RESTORATION	0
BK STR STA	BLACK STRETCH START POINT	1
BK STR GAN	BLACK STRETCH START GAIN	1
MENU.11		
OVER MD SW		1
Y GAMMA	Y GAMMA START POINT	0
FSC C.SYNC	f_{SC} C-SYNC OUTPUT	1
VBLK SW	VERTICAL BLANKING CONTROL SWITCH	0
SND TRAP	SOUND TRAP	1
HALF TONE	HALF TONE LEVEL	3
HALF T SW	HALF TONE ON/OFF SWITCH	1
TST VERSET		0
MENU.12		
E/W DC	E/W（EAST/WEST）	32
E/W AMP	E/W	32

(continued)

E/W TILT	E/W	32
E/W C TOP	E/W	5
E/W C BOTM	E/W	5
MENU.13		
E/W TEST	E/W TEST	7
HSIZE COMP	HORIZONTAL SIZE COMPENSATION	7
IF TEST 3B	3dB IF TEST	0
V.LEV ADJ	VIDEO LEVEL ADJUSTMENT	0
OV MOD LEV		5
PRE/OVER	PRE/OVER-SHOOT ADJUSTMENT	0
C.VCO SW	CHROMA VCO（VOLTAGE CONTROLLED OSCILLATOR）SWITCH	0
C.VCO ADJ	CHROMA VCO ADJUSTMENT	0
MENU.14		
VNSYNC		0
TINT.THROU	TINT THROUGH	0
HLOCK.VDET		0
MENU.15		
OPT.1CHIP	OPTION 1CHIP	1
OPT.VIDEO	OPTION VIDEO	1
OPT.DVD	OPTION DVD	1
OPT.AV1AV2	OPTION AV1/AV2	1
OPT.AV3	OPTION AV3	0
OPT.S-VHS	OPTION S-VHS	1
OPT.YUV	OPTION YUV	0
OPT.COMB	OPTION COMB	0
OPT.BYPASS	OPTION BYPASS	0
MENU.16		
OPT. VM	OPTION VM	0
OPT.BLUEBK	OPTION BLUEBK	1
OPT.V-CHIP	OPTION V-CHIP	1
OPT.CCD	OPTION CCD	1
OPT.CLOCK	OPTION CLOCK	1
OPT.P-ON	OPTION	0
SRCH.SPEED	SEARCH SPEED	0
ROM .CORREC	ROM CORRECTION	0
MENU.17		
OPT.BTSC	OPTION BTSC	1
OPT.AV-INP	OPTION AV-INP	0
OPT.BBE	OPTION BBE	0
OPT. DVD-IN	OPTION DVD-IN	0
SUB.BASS	SUB BASS	3
SUB.TREBLE	SUB TREBLE	3

(continued)

MENU.18		
LOUNDNESS	LOUDNESS	9
FM/AM.PRES	FM/AM PRESETTING	63
SCART.PRES	SCART PRESETTING SCART VOLUME	39
SCART.VOL	SCART VOLUME	117
OPT.AVC	OPTION AVC	1
AVC.DECAY		2
BBE.BASS	BBE BASS	32
BBE.TREBLE	BBE TREBLE	32

Notes:

① The data sheet may differ dependent on different models.

② The data sheet may differ dependent on different CRTs for the same model.

ADJUSTMENTS FOR DVD UNIT

1. Power on the unit only after ensuring DVD130A modules is connected correctly in accordance with the wiring diagram.
2. If the unit fails to play after power-on, repair the DVD130A according to the service illustration until it can read discs and has corresponding AV output.
3. Inspect audio output of the DVD130A in the following ways.
   a. Inspect digital audio output: When playing a disc, connect a signal cable to the coaxial output terminal. Press the SETUP button on the remote control and set “ AUDIO OUT ” in the SETUP menu to “ SPDIF/SOURCE CODE ”. Then start playback with the PLAY button and the following diagram will be displayed with waveform amplitude of 0.75±0.25Vpp on the oscilloscope. After inspection, set “ AUDIO OUT ” to “ ANALOG ”.
   b. Connect the OUT terminal on the DVD130A to the IN terminal on the TV and shift the TV to the DVD mode. After power-on for several seconds, the TV should display the preset LOGO picture on the screen, which should be smooth and distort-free with normal color. Press the OPEN/CLOSE button on the remote control to open the disc tray. Place the disc on the disc tray. Press the PLAY button and play should begin after several seconds. The color and sound should be normal, and picture should be smooth and distortionless.
   c. With a CD disc played, the TV should display the preset LOGO picture on the screen. The color and sound should be normal, and picture should be smooth and distortionless.

STRUCTURE AND CHASSIS FUNCTION DESCRIPTION

1. STRUCTURE BLOCK DIAGRAM (For CPU CH04T1224 Only)

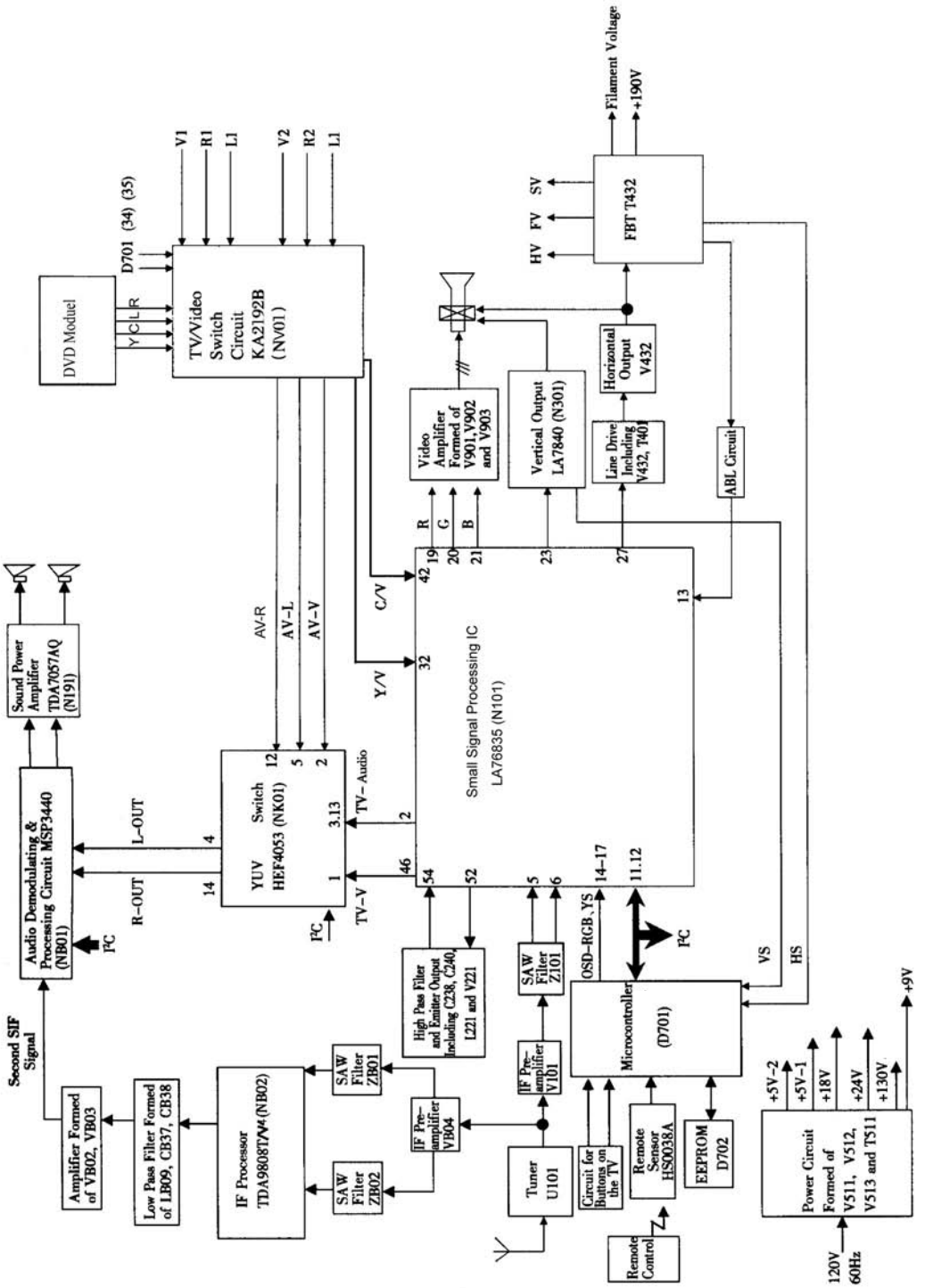


Fig. 4 Structure Block Diagram for CN-12DV Chassis

3.BLOCK DIAGRAM OF SUPPLY VOLTAGE SYSTEM

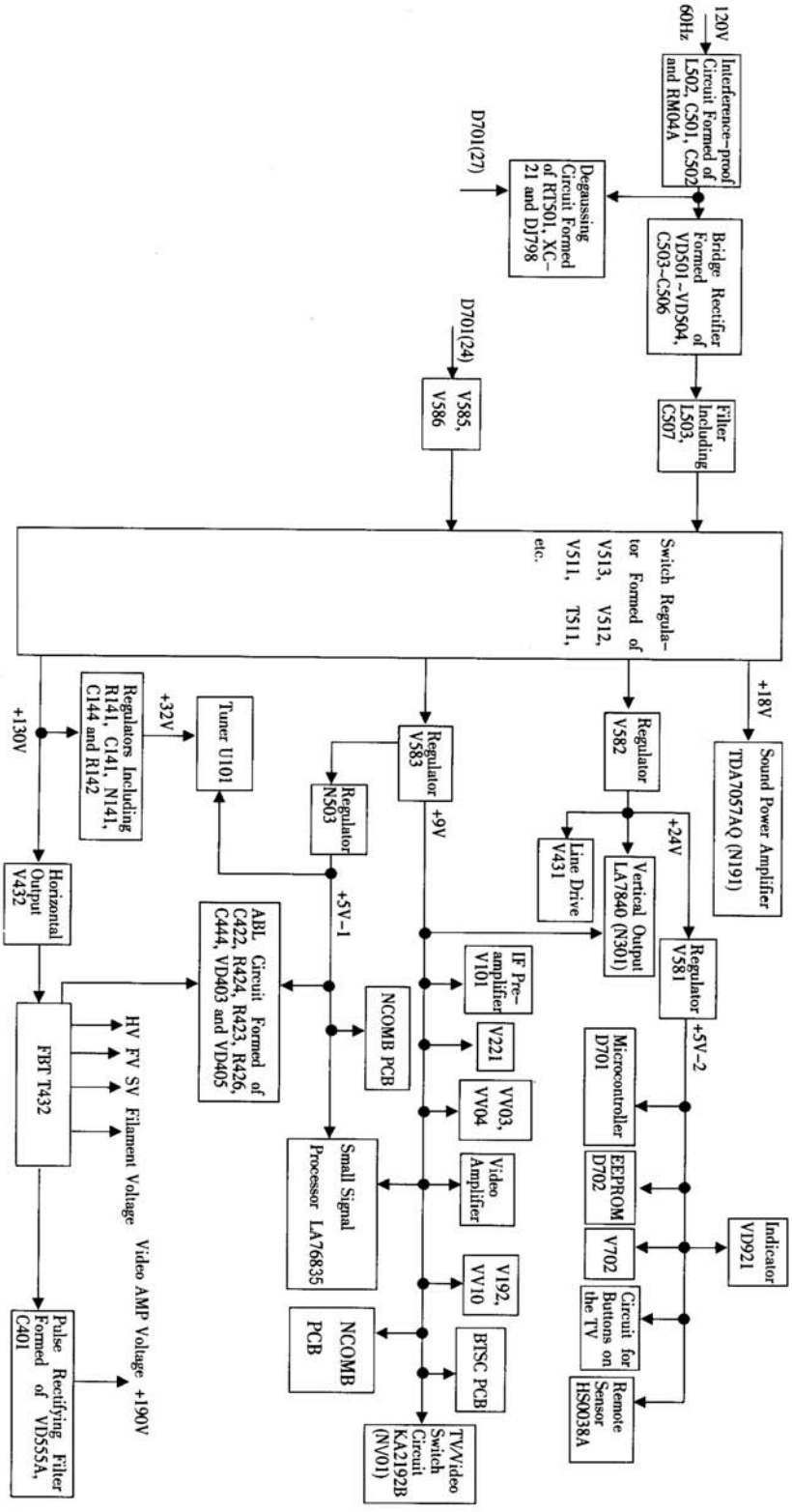


Fig. 6 Block Diagram for CN-12DV Supply Voltage System

4. BLOCK DIAGRAM OF REMOTE CONTROL SYSTEM

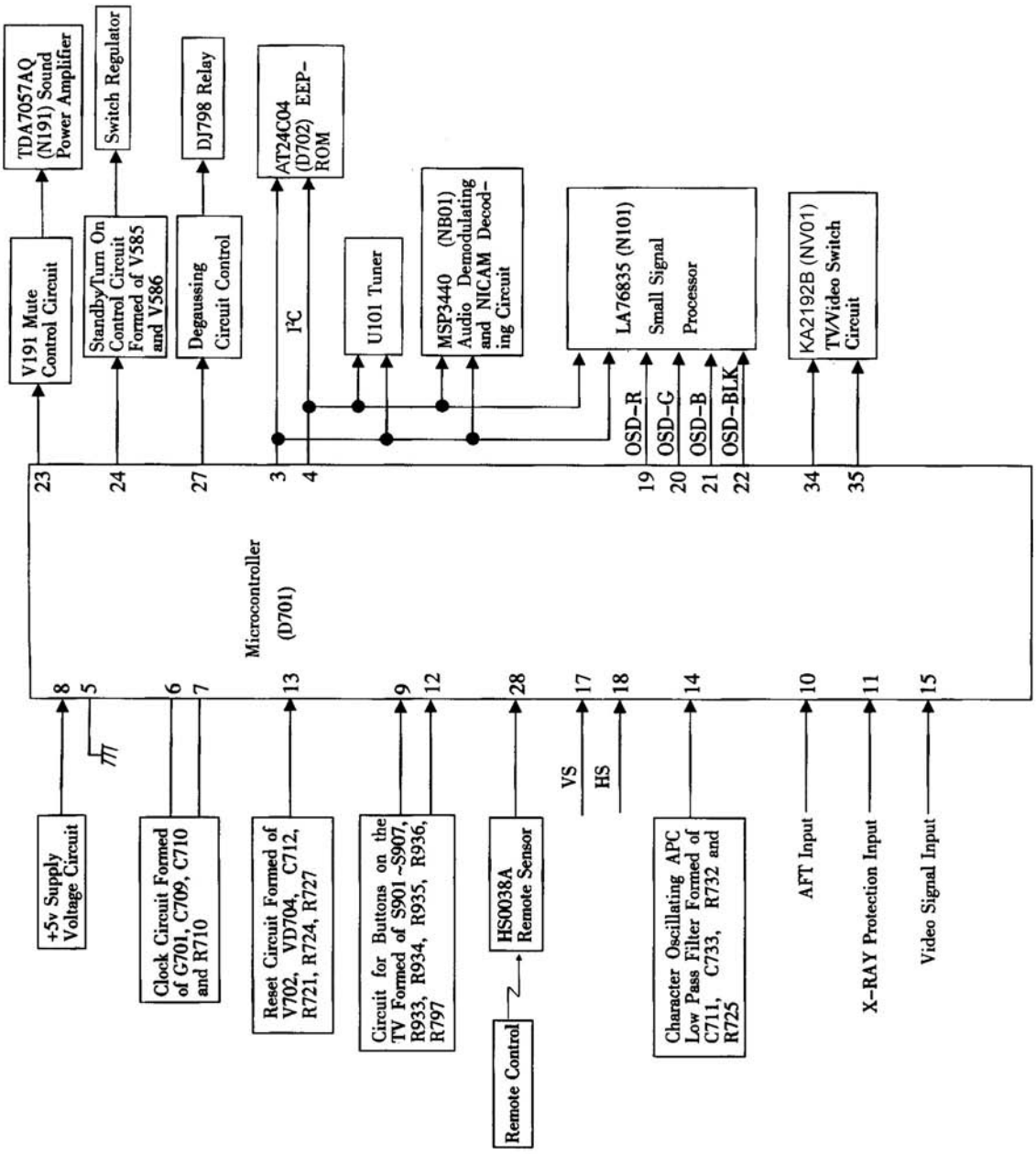


Fig. 7 Block Diagram for CN-12DV Remote Control Structure

4. STRUCTURE BLOCK DIAGRAM FOR DVD130A

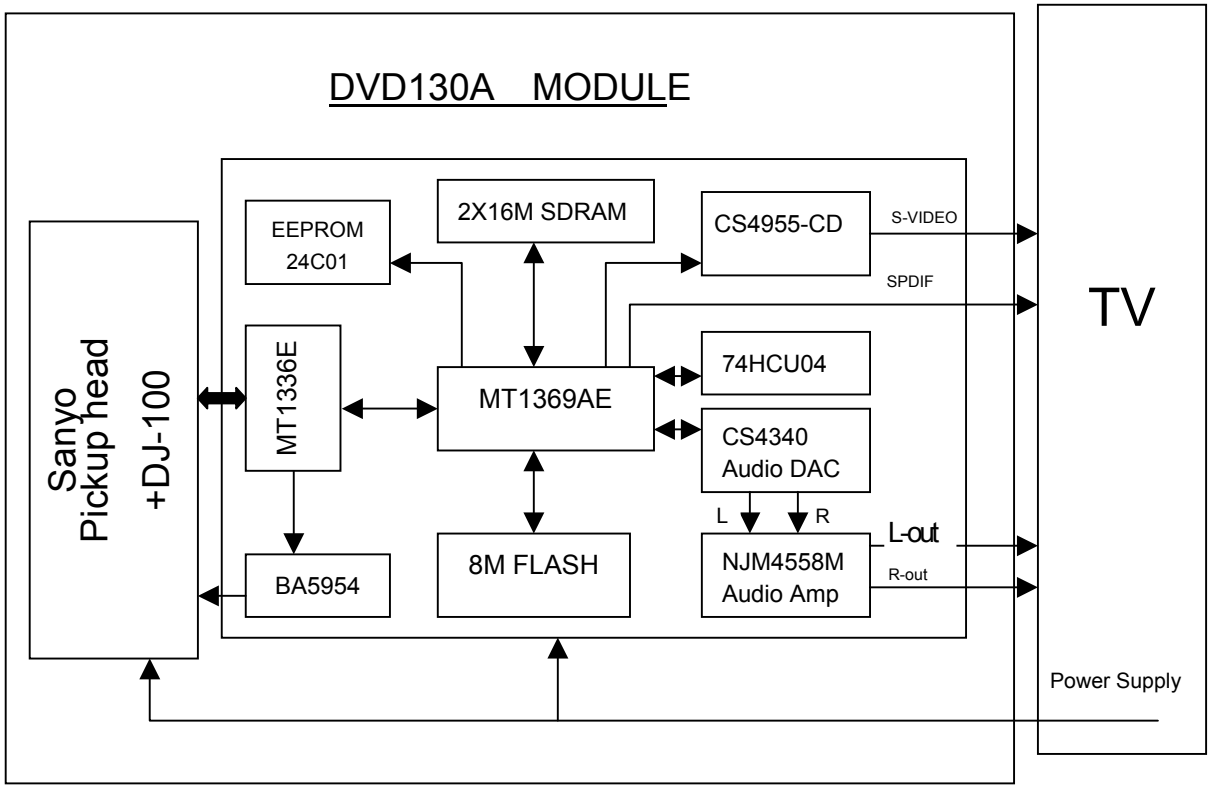


Fig. 8 Structure Block Diagram for DVD130A

5. CHASSIS FUNCTION DESCRIPTION

5.1. General Description

MTV-DV05 TV/DVD combo has combined function of TV signal reception and DVD discs playback, of which TV unit uses CN-12C2 chassis and DVD unit uses loader DVD 130A.

CN-12C2 chassis applies a single chip IC LA76835 of Japan-based Sanyo for small signal processing, featuring multi system reception. The applied I^2C bus control technology can automatically adjust and control the TV for much convenience of operation and servicing. Refer to Fig.4 about the chassis' structure block diagram.

Compatible with DVD, CD, VCD, SVCD, MP3, and KODAR Picture CD, DVD130A, high-quality modules with various functions, features multi angle, multilingual and multi captions. With Dolby dual channel amplifying and DTS coaxial cable, the DVD audio system offers astonishingly high-quality audio output.

DVD130A consists of a disc tray (including DJ-100 assembly and small loader DV-33FS) and analog signal processor/servo control/MPEG decoding board MT1369AE+MT1336E. The servo control/MPEG decoding board MT1369AE, developed by MEDIATEK, is designed for use in signal control, decoding, data processing, etc., featuring servo control, AV decoding, analog front end, DPU (DATA PATH UNIT), main axis control, CSS/CPPM module, system analysis program, video output unit, audio terminals and system control. MT1336E, also

developed by MEDIATEK, is a high-performance CMOS analog signal processor with servo amplifying and DPD tracking error signal for use in CD-ROM drive and DVD-RAM. For DVD-RAM, MT1336E also uses DPP for developing tracking signal and DAD for processing focus signal. Meanwhile, the IC, programmable, is equipped with a separate DVD-ROM, CD-ROM two-way automatic laser power control circuit and reference voltage generator.

5.2 Key ICs and Assemblies

5.2.1 The CN-12C2 chassis mainly uses the following ICs and assemblies.

Table 2 Key ICs and Assemblies of CN-12C2 Chassis

Serial No.	Position	Type	Function Description
1	D701	CH04T1227	Microcontroller
2	D702	AT24C08	EEPROM
3	N101	LA76835	Small signal processor
4	NV01	KA2192B	TV/Video switch circuit
5	N301	LA7840	Vertical output circuit
6	N191	TDA7057AQ	Sound power amplifier
7	NN01	TDA9808T	Audio IF demodulator
8	NN02	MSP3410G	NICAM audio processor
9	N503	LM7805	Tri-pin regulator
10	NK01	HEF4053	Electronic switch circuit
11	U101	TDQ-3B8/136	Tuner

5.2.2. The DVD130A mainly uses the following ICs and assemblies.

Table 3 Key ICs and Assemblies of DVD130A

Serial No.	Position	Type	Function Description
		MPEG board	Drawing No. JUV2.033.071-1MX
1	U1	MT1336E	RF amplifier
2	U2	BA5954FM	Focus/tracking coil and feed motor drive
3	U3	MT1369AE	MPEG decoder
4	U5	74HCU04	Enhancement drive
5	U7	8M FLASH	Flash memory
6	U9	NJM4558M	Sound amplifier
7	U10	24C01	1K EEPOM
8	U13	CS4340	Audio D/A controller
9	U14	CS4955-CD	Video encoder
10	U17	16M SDRAM	Dynamic EEPROM
		DJ-100	Disc tray assembly

SERVICE DATA
SERVICE DATA FOR TV UNIT

TECHNICAL DATA OF KEY ICS
CH04T1227 (D701)

8-Bit Single Chip Microcontroller

1. Overview

The LC86F344BA are 8-bit single chip microcontrollers with the following on-chip functional blocks:
-CPU:Operable at a minimum bus cycle time of 0.424μs
-On-chip ROM capacity
Program ROM:32K/28K/24K/20K/16K bytes
CGROM:16K bytes
-On-chip ROM capacity: 512 bytes
-OSD RAM: 352×9 bits
-Closed-Caption TV controller and the on-screen display controller
-Closed-Caption data slicer
-Four channels×6-bit AD Converter
-Three channels×7-bit PWM
-16-bit timer/counter,14-bit base timer
-IIC-bus compliant serial interface circuit (Multi-master type)
-ROM correction function
-11-source 8-vectored interrupt system
-Integrated system clock generator and display clock generator
Only one X'tal oscillator (32.768kHz) for PLL reference is used for both generators
TV control and the Closed Caption function
All of the above functions are fabricated on a single chip.

2. System Block Diagram

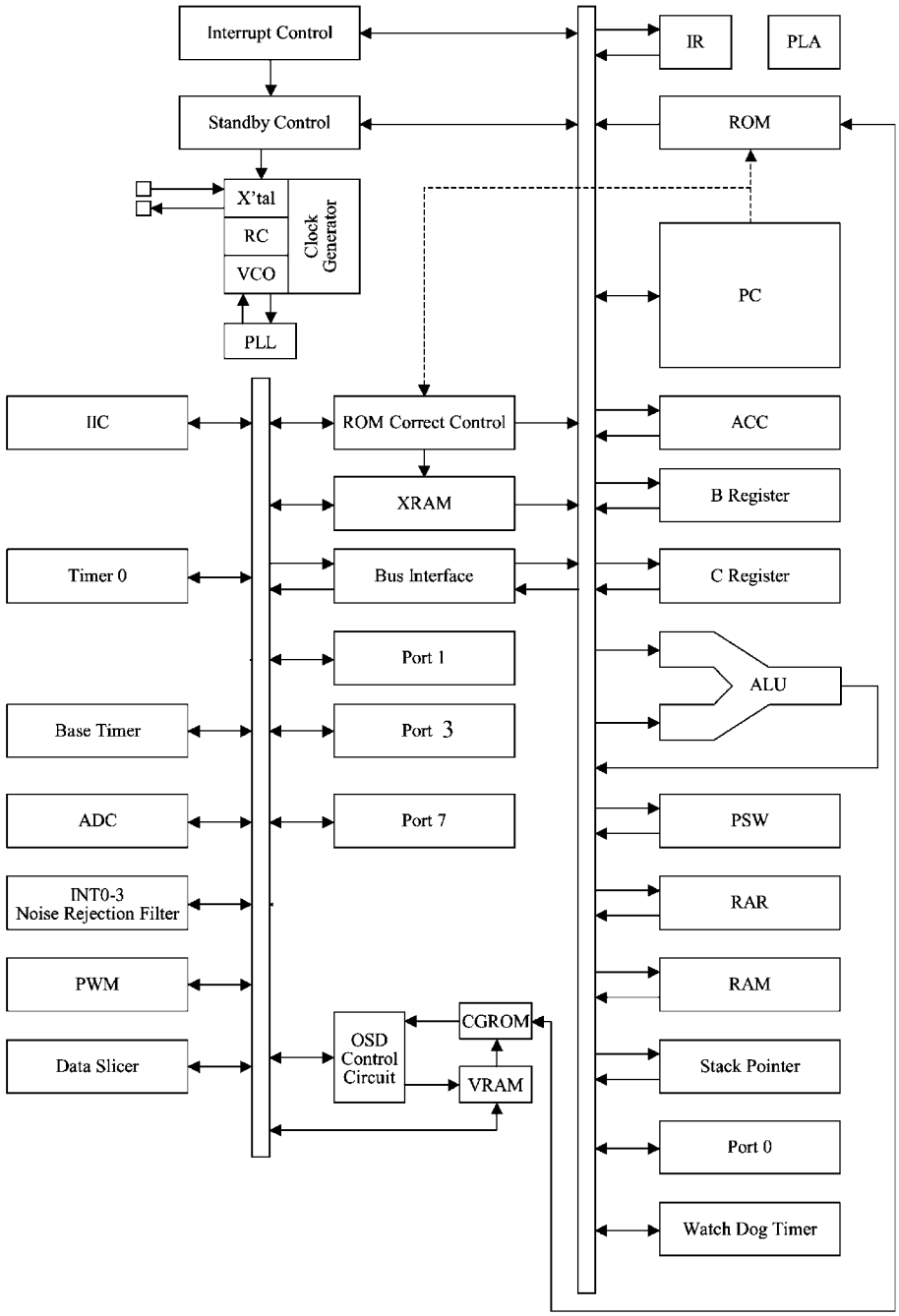


Fig. 9

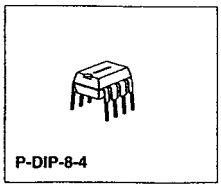
3. Refer to Table 4 about Functions and Service Data of the IC's Pins.

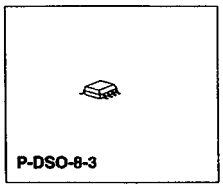
AT24C08 (D702)
EEPROM

1. Features

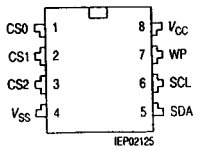
- · Data EEPROM internally organized as 1024/2048 bytes and 64/128 pages×16 bytes
- · Page protection mode, flexible page-by-page hardware write protection
- - Additional protection EEPROM of 64/128 bits, 1 bit per data page
- - Protection setting for each data page by writing its protection bit
- - Protection management without switching WP pin
- · Low power CMOS
- · Vcc=2.7 to 5.5V operation
- · Two wire serial interface bus, I^2C-Bus compatible
- · Filtered inputs for noise suppression with Schmitt trigger
- · Clock frequency up to 400 kHz
- · High programming flexibility
- - Internal programming voltage
- - Self timed programming cycle including erase
- - Byte-write and page-write programming, between 1 and 16 bytes
- - Typical programming time 6 ms(<10ms) for up to 16 bytes
- · High reliability
- - Endurance 10^6 cycles[1)]
- - Data retention 40 years[1)]
- - ESD protection 4000 V on all pins
- · 8 pin DIP/DSO packages
- · Available for extended temperature ranges
- - Industrial: -40°C to +85°C
- - Automotive: -40°C to +125°C

2. Pin Configuration

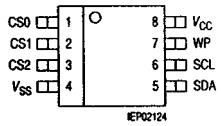




P-DIP-8-4



P-DSO-8-3



3. Block Diagram

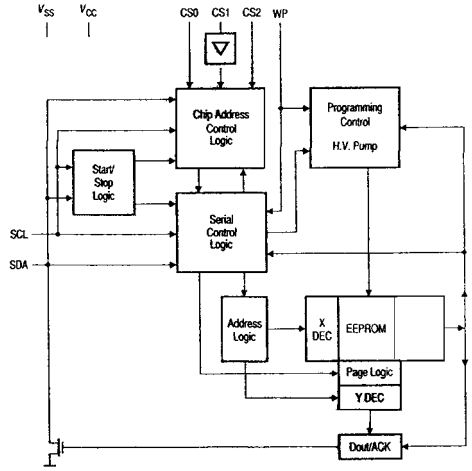


Fig.10

4. Refer to Table 5 about Functions and Service Data of AT24C08's Pins.

KA2192B (NV01)

TV/Video Switch Circuit

1. Features

The TV/Video switch circuit KA2192B (NY01) is an electronic switch circuit controlling four sets of audio signal inputs, three sets of video signal inputs, two sets of Y/C separation signals inputs, one set of video signal output, one set of Y/C separation signal output and one set of audio signal output.

2. Block Diagram

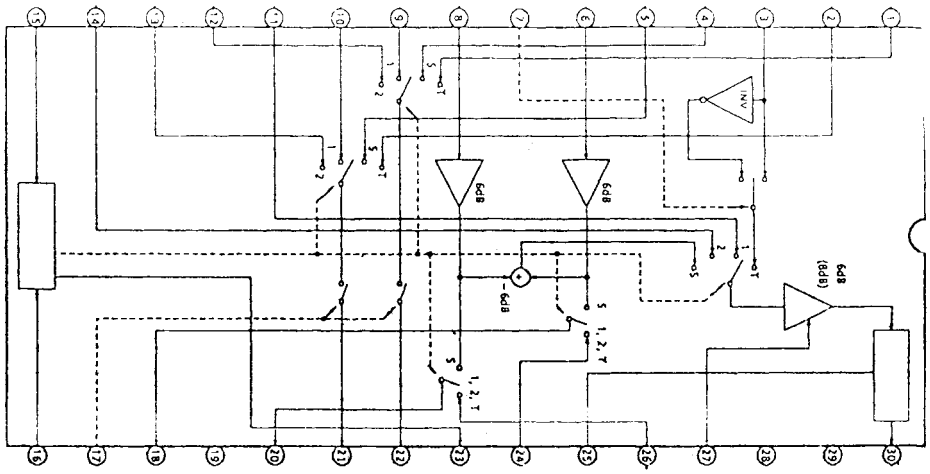


Fig.11

3. Value Table

Level for Control Terminal		Switchover Mode
(15)	(16)	
H	H	TV
H	L	AV1
L	H	SVHS
L	L	AV2

4. Refer to Table 6 about Functions and Service Data of KA2192B's Pins.

LA7840 (N301)

Vertical Deflection Output Circuit

1. Features

·Low power dissipation due to built-in pump-up circuit

·Vertical output circuit

·Thermal protection circuit built in

·Excellent crossover characteristics

·DC coupling possible

2. Block Diagram

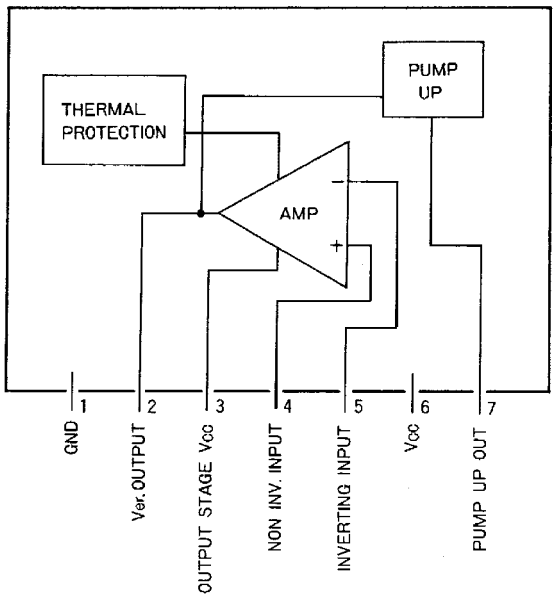


Fig. 12

3. Refer to Table 7 about Functions and Service Data of LA7840's Pins.

TDA7057AQ (N191)

2×8W Stereo BTL Audio Output Amplifier with DC Volume Control

1. Features

·DC volume control
·Few external components
·Mute mode
·Thermal protection
·Short-circuit proof
·No switch-on and switch-off clicks
·Good overall stability
·Low power consumption
·Low HF radiation
·ESD protected on all pins.

2. General Description

The TDA7057AQ is a stereo BTL output amplifier with DC volume control. The device is designed for use in TVs and monitiors, but is also suitable for battery-fed portable recorders and radios.

Missing Current Limiter (MCL)

A MCL protection circuit is built-in. The MCL circuit is activated when the difference in current between the output terminal of each amplifier exceeds 100mA (typical 300 Ma). This level of 100mA allows for single-ended headphone applications.

3. Block Diagram

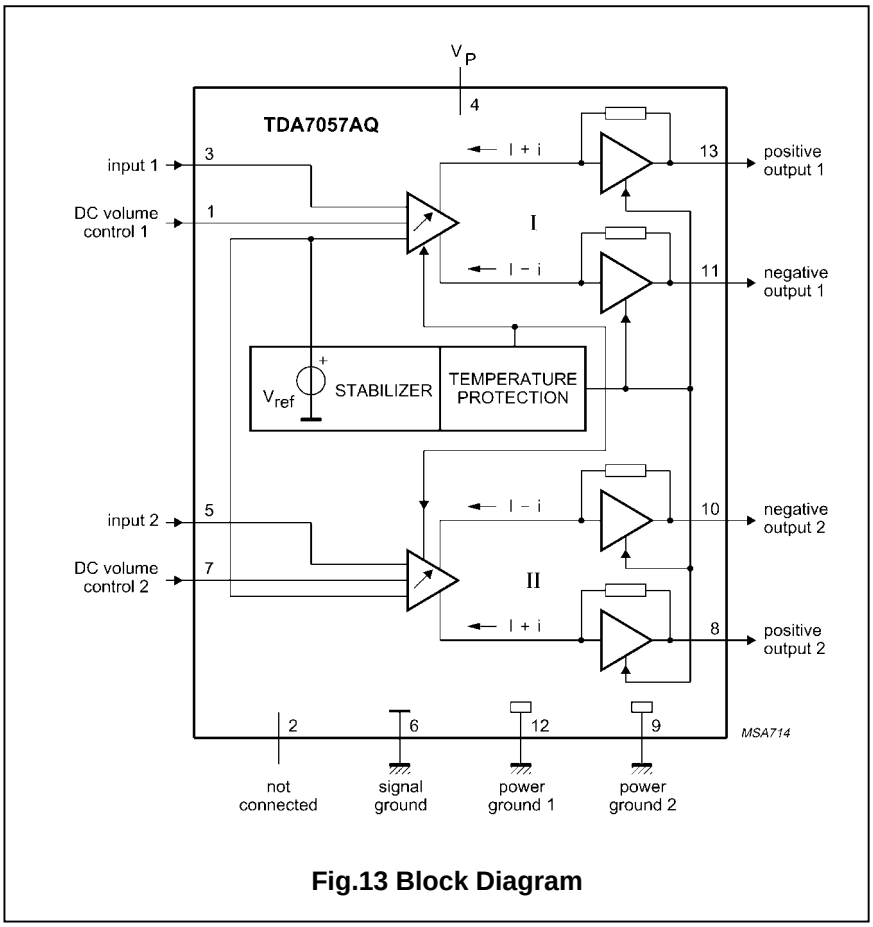


Fig.13 Block Diagram

4. Refer to Table 8 about Functions and Service Data of TDA7057AQ' s Pins.

HEF4053 (NK01)

Triple 2-channel Analog Multiplexer/Demultiplexer

1. Description

The HEF4053 is a triple 2-channel analog multiplexer/demultiplexer with a common enable input (E). Each multiplexer/ demultiplexer has two independent inputs/ outputs (Y_0 and Y_1), a common input/ output (Z), and select inputs (Sn). Each also contains two-bidirectional analog switches, each with one side connected to an independent input/output (Y_0 and Y_1) and the other side connected to a common input/output(Z).

With ($\overline{E}$) LOW, one of the two switches is selected (low impedance ON-state) by Sn. With E HIGH, all switches are in the high impedance OFF-state, independent of S_A to S_C.

V_{DD} and V_{SS} are the supply voltage connections for the digital control inputs (S_A to S_C and E). The V_{DD} to V_{SS} range is 3 to 15V.The analog inputs/outputs (Y_0,Y_1 and Z) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. V_{DD}-V_{EE} may not exceed 15 V.

For operation as a digital multiplexer/ demultiplexer, V_{EE} is connected to V_{SS} (typically ground).

2. Block Diagram

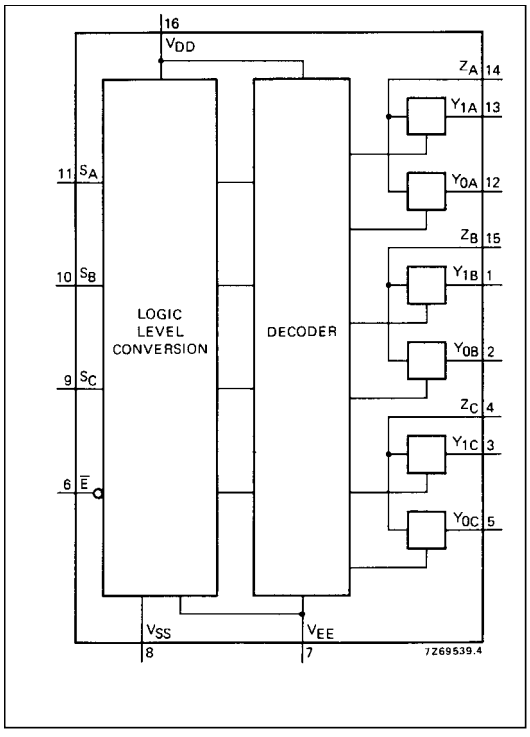


Fig. 14 Functional Diagram

3. Function Table

Inputs		Channel On
$\overline{E}$	Sn	
L	L	Y_{on}-Zn
L	H	Y_{in}-Zn
H	X	none

Notes

H=HIGH state (the more positive voltage)

L=LOW state (the less positive voltage)

X=STATE is immaterial

4. Refer to Table 11 about Functions and Data of HEF4053's Pins.

TDA9808T

SINGLE STANDARD VIF-PLL WITH QSS-IF AND FM-PLL DEMODULATOR

1. Features

·5V supply voltage (9V supply voltage for TDA9808T (DIP20) only)
·Applicable for IFs (Intermediate Frequencies) of 38.9MHz, 45.75MHz and 58.75 MHz
·Gain controlled wide band Video IF (VIF)-amplifier (AC-coupled)
·True synchronous demodulation with active carrier regeneration (very linear demodulation, good intermodulation figures, reduced harmonics, excellent pulse response)
·Robustness for over-modulation better than 105% due to Phase Locked Loop (PLL)-bandwidth control at negative modulated standards
·VIF Automatic Gain Control (AGC) detector for gain control, operating as peak sync detector
·Tuner AGC with adjustable TakeOver Point (TOP)
·Automatic Frequency Control (AFC) detector without extra reference circuit
·AC-coupled limiter amplifier for sound intercarrier signal
·Alignment-free FM-PLL demodulator with high linearity
·Sound IF (SIF) input for single reference Quasi Split
Sound (QSS) mode (PLL controlled); SIF AGC detector for gain controlled SIF amplifier, single reference QSS mixer for high performance
·Electrostatic Discharge (ESD) protection for all pins.

2. General Description

The TDA9808T is an integrated circuit for single standard (negative modulated) vision IF signal processing and FM demodulation, with single reference QSS-IF in TV and VTR sets.

3. Block Diagram

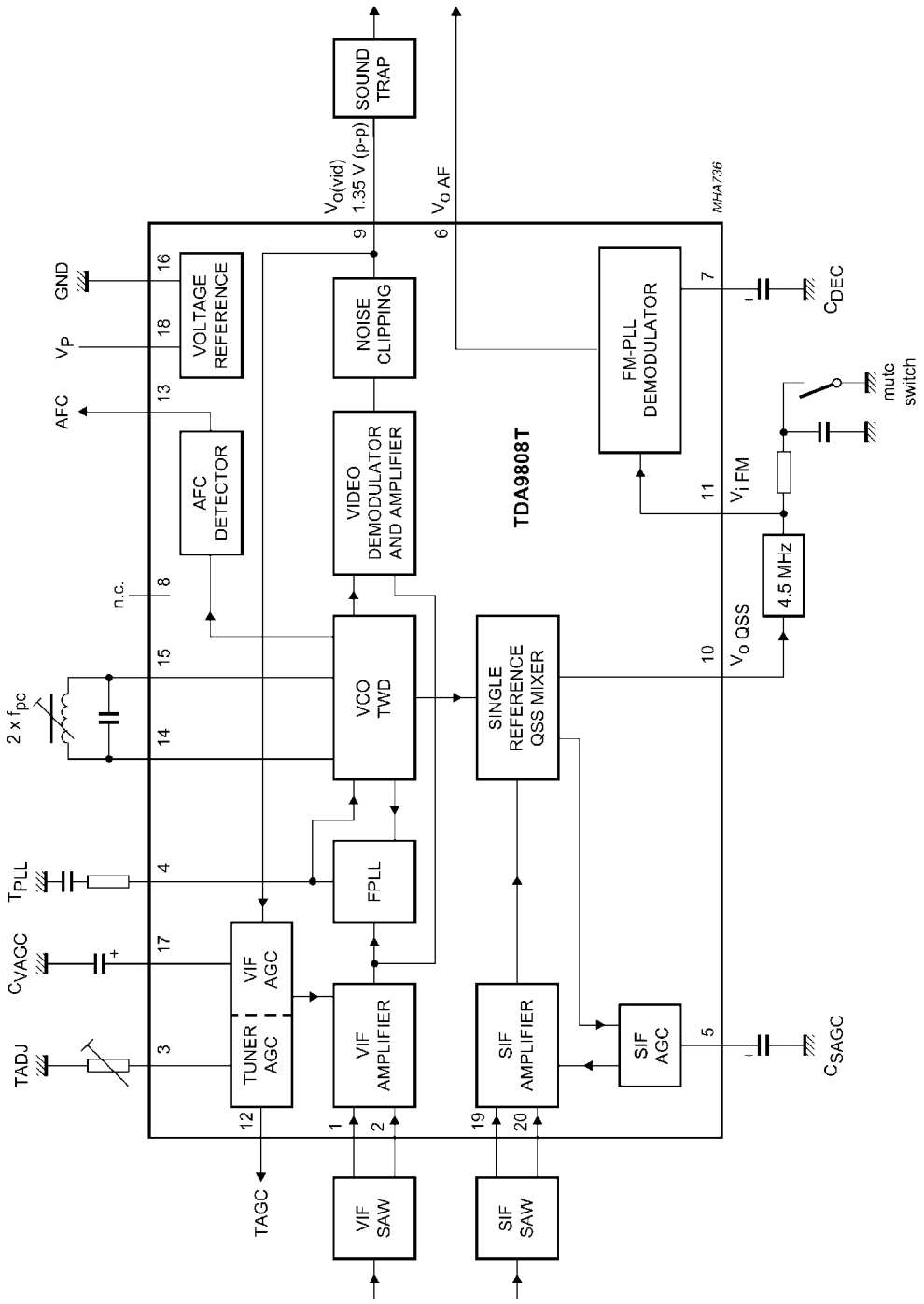


Fig. 15 Block Diagram

4. Refer to Table 20 about Functions and Data of the IC's Pins.

MSP34X0G

MULTISTANDARD SOUND PROCESSOR FAMILY

Release Note: Revision bars indicate significant changes to the previous edition. The hardware and software description in this document is valid for the MSP34X0G version B5 and following versions.

1. Introduction

The MSP34X0G family of single-chip Multistandard Sound Processors covers the sound processing of all analog TV-Standards worldwide, as well as the NICAM digital sound standards. The full TV sound processing, starting with analog sound IF signal-in, down to processed analog AF-out, is performed on a single chip. Figure 10 shows a simplified functional block diagram of the MSP34X0G.

This new generation of TV sound processing ICs now includes versions for processing the multichannel television sound (MTS) signal conforming to the standard recommended by the Broadcast Television Systems Committee (BTSC). The DBX noise reduction, or alternatively MICRONAS Noise Reduction (MNR) is performed alignment free.

Other processed standards are the Japanese FM-FM multiplex standard (EIA-J) and the FM Stereo Radio standard.

Current ICs have to perform adjustment procedures in order to achieve good stereo separation for BTSC and EIA-J.
The MSP34X0G has optimum stereo performance without any adjustments.

All MSP34X0G versions are pin and software downward-compatible to the MSP34X0G. The MSP34X0G further simplifies controlling software. Standard selection requires a single I^2C transmission only.
The MSP34X0G has built-in automatic Functions: The IC is able to detect the actual sound standard automatically (Automatic Standard Detection). Furthermore, pilot levels and identification signals can be evaluated internally with subsequent switching between mono/stereo/bilingual, no I^2C interaction is necessary (Automatic Sound Selection).

The ICs are produced in submicron CMOS technology.
The MSP34X0G is available in the following packages, PLCC68, PSDIP64, PSDIP52, PQFP80 and PLQFP64.

2. Block Diagram

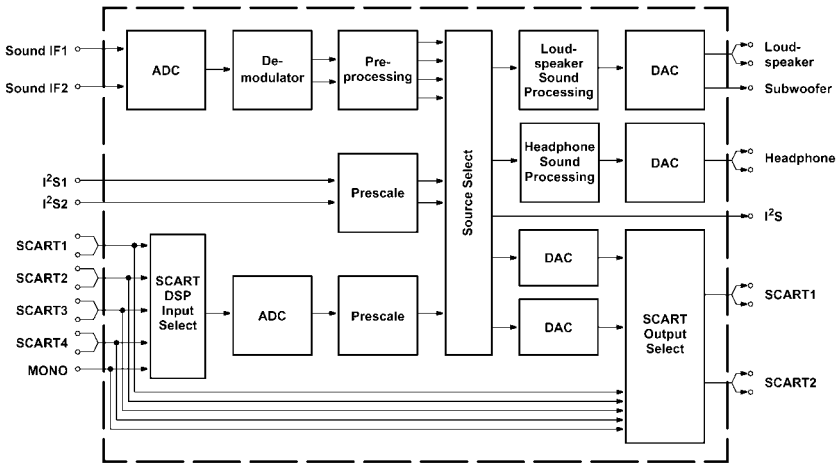


Fig. 16 Simplified Functional Block Diagram of the MSP34X0G

3. Refer to Table 21 about Functions and Data of the IC's Pins.

SERVICE DATA OF KEY ICS

Table 4 Functions and Service Data of LA76835 (N101)'s Pins

Pin No.	Function Description	GDM8145 Multimeter		
		Voltage of Pin (V)	Ground Resistance (Ω)	
			Measure with red probe while grounding black probe.	Measure with black probe while grounding red probe.
1	Audio signal output (NC)	2.33	810	712
2	Audio demodulation output	2.36	975	675
3	IF AGC filter	2.6	860	718
4	RFAGC voltage output	1.95	∞	680
5	IF signal input	2.89	780	693
6	IF signal input	2.89	778	712
7	IF circuit ground	0	0	0
8	Supply voltage for IF circuit	5.04	500	280
9	Filter for discriminator	1.98	910	713
10	AFT voltage output	3.65	910	617
11	I^2C bus data line	4.71	1560	640
12	I^2C bus clock line	4.41	1542	667
13	Auto brightness control input	3.68	945	577
14	R character signal input	1.43/0	920	700
15	G character signal input	1.46/0	913	701
16	B character signal input	1.44/0	906	700
17	Supply voltage for decoder	0.02/0	780	683
18	Red (R) signal output	8.28	525	500
19	Green (G) signal output	2.81	780	671
20	Blue (B) signal output	2.79	780	670
21	Character blanking signal input	2.7	780	670
22	White balance adjusting signal input (NC)	1.85	830	696
23	Vertical sawtooth output	2.45	710	672
24	Vertical sawtooth generation	2.64	782	702
25	Horizontal start supply voltage	5.27	350	350
26	Low pass filter for horizontal AFC	2.72	815	708
27	Line drive pulse output	0.72	700	653
28	Line flyback pulse input	0.91	785	707
29	Reference voltage generation terminal	1.74	746	700
30	B-Y color difference signal input (SECOM)	0.93	825	608
31	C-Y color difference signal input (SECOM)	0.94	330	330
32	External video/chroma signals inputs	4.17	∞	567
33	1H baseband delay circuit ground	0	0	0

(continued)

34	X-RAY detection input	0	775	712
35	4.43MHz CW signal output or SECAM killer signal input	2.05	776	712
36	AFC filter for color sub-carrier	3.41	810	724
37	Clamp filter	0	800	706
38	4.43 MHz crystal oscillator connection	2.83	790	716
39	APC filter	1.89	760	697
40	Video signal output (NC)	2.76	730	662
41	Video/chroma/scan part ground	0	0	0
42	Video signals input from AV terminals or Y signal input from S-VIDEO terminal	2.93	800	711
43	Supply voltage for video/chroma/scan part	4.99	285	280
44	C signal input from AV terminals or S-VIDEO terminal (NC)	2.76	805	707
45	Filter for black level stretch	3.16	762	700
46	Video detection output	2.9	397	397
47	IF lock detection filter	3.58	840	712
48	External VCO harmonic oscillating coil	4.29	526	526
49	External VCO harmonic oscillating coil	4.29	530	530
50	IF PLL APC filter	2.47	820	698
51	Audio signal input (NC)	2.23	800	701
52	Sound IF output	1.94	809	697
53	APC filter for audio discrimination	2.41	808	691
54	Sound IF input	3.17	824	712

Table 5 Functions and Service Data of CH04T1227 (D701)'s Pins

Pin No.	Function Description	GDM8145 Multimeter		
		Voltage of Pin (V)	Ground Resistance (KΩ)	
			Measure with red probe while grounding black probe.	Measure with black probe while grounding red probe.
1	Not connected	1.50	11.8	4.40
2	Not connected	1.43	12.1	5.20

(continued)

3	Bus data line	4.70	11.6	6.20
4	Bus clock line	4.47	12.1	6.00
5	Ground	0.00	0.00	0.00
6	Input terminal for clock oscillating signal	1.78	12.6	5.1
7	Output terminal for clock oscillating signal	2.88	12.0	4.91
8	Supply voltage	5.31	7.90	3.72
9	Button-control voltage input terminal 1	0.02	9.70	5.34
10	AFT voltage input terminal	2.47	4.90	5.08
11	X-RAY detection input	2325	6.70	4.59
12	Button-control voltage input terminal 2	0.015	8.86	3.81
13	Reset	5.27	4.67	1.88
14	Character oscillating filter	3.87	1.11	4.98
15	Video signal input terminal	3.53	12.3	4.50
16	Three bits input/output terminals	0.01	9.76	15.0
17	Input terminal for vertical flyback pulse	5.07	15.4	18.1
18	Input terminal for horizontal flyback pulse	4.62	17.4	18.4
19	R character output terminal	0.015	3.92	3.29
20	G character output terminal	0.014	3.95	3.71
21	B character output terminal	0.015	3.19	3.66
22	Output terminal for fast blanking signal	0.015	6.50	3.67
23	Mute	0.015	18.7	17.62
24	Standby control	0.015	1.43	7.30
25	Not connected	1.23	9.50	6.65
26	Control terminal for production modes	4.61	13.0	6.95
27	Degaussing circuit control	0.014	3.713	3.42
28	Remote control signal input	5.19	12.2	5.32
29	Not connected	5.30	12.4	5.49
30	Not connected	5.30	12.6	5.42
31	Not connected	0.01	12.7	5.35
32	Not connected	0.01	12.7	5.30
33	Output terminal for on/off control signals	5.30	12.7	6.59
34	Output terminal for AV2 on/off control	5.30	11.8	6.36
35	Output terminal for AV1 on/off control	5.30	11.4	6.33
36	Output terminal for AV0 on/off control	5.29	11.2	6.33

Table 6 Functions and Service Data of AT24C08 (D702)'s Pins

Pin No.	Function Description	GDM8145 Multimeter		
		Voltage of Pin (V)	Ground Resistance (KΩ)	
			Measure with red probe while grounding black probe.	Measure with black probe while grounding red probe.
1	Address terminal 0	0	0	0
2	Address terminal 1	0	0	0
3	Address terminal 2	0	0	0
4	Ground	0	0	0
5	Data line	4.8	11.7	5.25
6	Clock line	4.8	11.72	5.5
7	Write-in/read-out control terminal	0	0	0
8	Supply voltage	5	6.7	4

Table 7 Functions and Service Data of KA2192B (NV01)'s Pins

Pin No.	Function Description	DT890D Digital Multimeter		
		Voltage of Pin (V)	Ground Resistance (KΩ)	
			Measure with red probe while grounding black probe.	Measure with black probe while grounding red probe.
1	L TV IN	5.67	6.45	3.53
2	R TV IN	5.67	6.45	3.74
3	TV IN	5.67	6.57	4.02
4	LS IN	5.69	6.45	3.66
5	RS IN	5.69	6.47	3.72
6	SY IN	5.54	6.85	3.96
7	TV SW	0.00	0.00	0.00
8	SC IN	5.54	6.75	3.85
9	L1 IN	5.69	6.43	3.36
10	R1 IN	5.70	6.37	3.72
11	E1 IN	5.56	6.85	3.96
12	L2 IN	5.70	6.43	3.87

(continued)

13	R2 IN	5.70	6.33	3.67
14	E2 IN	5.56	6.83	4.01
15	SW1	5.25	6.84	5.59
16	SW2	5.25	6.85	5.59
17	MUTE	0.00	0.00	0.00
18	Y OUT	3.89	1.418	1.51
19	GND	0.00	0.00	0.00
20	C OUT	3.84	0.96	1.15
21	R OUT	4.37	0.63	3.35
22	L OUT	4.37	6.61	3.31
23	NC	0.06	6.71	3.97
24	Y IN	5.55	6.70	4.18
25	SYNC CLAMP	3.47	6.80	5.75
26	C IN	5.57	6.67	4.07
27	NC	0.25	6.69	4.13
28	VCC	9.38	0.34	0.33
29	VCC	9.38	0.31	0.30
30	VOUT	3.17	6.47	0.48

Table 8 Functions and Service Data of LA7840 (N301)'s Pins

Pin No.	Function Description	DT890D Digital Multimeter		
		Voltage of Pin (V)	Ground Resistance (Ω)	
			Measure with red probe while grounding black probe.	Measure with black probe while grounding red probe.
1	Ground	0	0	0
2	Vertical output terminal	14.8	365	360
3	Pump supply voltage input	24.5	∞	584
4	Reference voltage	2.24	660	600
5	Inverting input terminal	2.23	800	672
6	Supply voltage	24	770	465
7	Vertical flyback pulse output terminal	2.25	1167	638

Table 9 Functions and Service Data of TDA7057AQ (N191)'s Pins

Pin No.	Function Description	GDM8145 Multimeter		
		Voltage (V)	Positive Resistance (KΩ)	Negative Resistance (KΩ)
1	Volume control input	0.95	6.85	6.15
2	Not connected	0.00	∞	∞
3	Audio R signal input	2.38	12.59	6.51
4	Supply voltage	17.48	0.47	0.47
5	Audio L signal input	2.37	12.5	6.51
6	Ground	0.00	0.00	0.00
7	Volume control input	0.95	6.85	0.15
8	Left channel in-phase signal output	8016	6.46	5.59
9	Ground	0.00	0.00	0.00
10	Left channel inverting signal output	8.25	6.46	5.59
11	Right channel inverting signal output	8.24	6.46	5.59
12	Ground	0.00	0.00	0.00
13	Right channel in-phase signal output	8.13	6.46	5.59

Table 10 Functions and Service Data of HEF4053 (NK01)'s Pins

Pin No.	Function Description	GDM8145 Multimeter		
		Voltage (V)	Positive Resistance (KΩ)	Negative Resistance (KΩ)
1	Signal input terminal	3.91	6.31	0.12
2	Signal input terminal	5.01	6.31	0.11
3	Signal input terminal	0.00	0.00	3.41
4	Signal output terminal	0.02	6.07	0.05
5	Signal input terminal	0.22	6.17	3.72
6	Ground	0.00	0.00	0.00
7	Ground	0.00	0.017	0.00
8	Ground	0.00	0.017	0.00
9	Control signal input terminal	4.42	6.27	6.08
10	Control signal input terminal	4.42	6.24	6.07
11	Control signal input terminal	4.42	6.24	6.08
12	Signal input terminal	3.30	6.08	3.66
13	Signal output terminal	1.31	5.96	4.72
14	Signal input terminal	1.44	5.95	3.69
15	Signal output terminal	1.43	6.017	4.01
16	Supply voltage	5.04	0.352	0.33

Table 11 Functions and Service Data of LM7805 (N503)'s Pins

Pin No.	Function Description	DT890D Digital Multimeter		
		Voltage of Pin (V)	Ground Resistance (Ω)	
			Measure with red probe while grounding black probe.	Measure with black probe while grounding red probe.
1	Input terminal	15	865	477
2	Regulation output	5	1015	477
3	Ground	0	0	477

Table 12 Functions and Service Data of TDA9808T Pins

Pin No.	Function Description	Digital Multimeter		
		Reference Voltage (V)	Positive Resistance (20KΩ)	Negative Resistance(20KΩ)
1	PIF signal input 1	3.23	7.2	6.03
2	PIF signal input 2	3.23	7.2	5.99
3	RFAGC start-control level adjust	0.99	6.7	5.85
4	PLL APC filter	2.53	7.9	6.3
5	Audio AGC filter	3.29	7.8	6.17
6	Audio output (NTSC 4.5MHz)	2.34	7.2	5.86
7	Filter	1.79	7.9	6.29
8	1/2VCC comparison voltage bias	0	∞	∞
9	Video output	2.18	7.6	6.09
10	Second SIF signal output	2.03	7.7	6.17
11	Second SIF signal input	2.81	5.2	4.99
12	RFAGC output	0.04		6.1
13	AGC signal output	3.05	7.9	6.2
14	External connection for VCO oscillating LC network	2.76	7	6
15	External connection for VCO oscillating LC network	2.76	7	6
16	Ground	0	0.001	0.00
17	AGC filter	3.13	7.9	6.11
18	Supply voltage input terminal	8	2.1	2.7
19	SIF signal input	3.2	2.1	6.27
20	SIF signal input?	3.2	7	6.27

Table 13 Functions and Service Data of MSP3410G Pins

Pin No.	Function Description	Digital Multimeter		
		Reference Voltage (V)	Positive Resistance (20KΩ)	Negative Resistance (20KΩ)
1	TP NC	0.16	7.3	5.3
2	AVD-GL-OUT NC	2.52	6.8	5.51
3	D-CTR-I/O-1 NC	0.01	7.3	5.57
4	D-CTR-I/O-0 NC	0.01	7.2	5.58
5	ADR-SEL	4.79	0.7	4.54

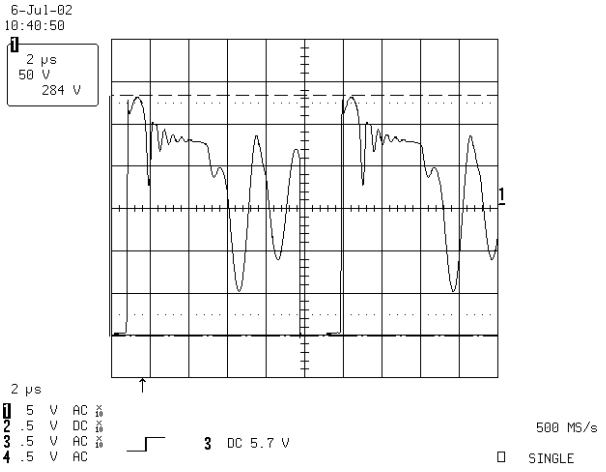
(Continued)

6	STANDBYQ	4.79	0.7	4.54
7	I2C-CL	3.56	7	4.44
8	I2C-DA	3.9	7	4.44
9	I2S-CL NC	2.36	7.2	6.24
10	I2S-WS NC	2.4	7.2	6.24
11	I2C-DA-WT NC	2.36	7.2	6.24
12	I2S-DA-IN1 NC	0.07	7.2	5.29
13	ADR-DA NC	0.07	7.2	5.59
14	ADR-WS	0.07	7.2	5.59
15	ADR-CL	0.07	7.2	5.59
16	DVSVP	4.79	0.7	4.54
17	DVSS	0.01	0.001	0.00
18	I2S-DA-IN2 NC	0.07	7.3	5.31
19	NC	0	∞	∞
20	RESETQ	4.76	7	5.24
21	DACA-R NC	0.8	3.5	3.54
22	DACA-L NC	0.08	3.5	3.52
23	VREF-I	0.01	0.001	0.00
24	DACM-R	0.17	3.5	3.52
25	DACM-L	0.08	3.5	3.54
26	DACM-SVB NC	0.18	3.6	3.6
27	SC2-OUT-R NC	3.82	7.1	5.92
28	SC2-OUT-L NC	3.82	7.1	5.91
29	CREF 1	0.01	0.001	0.00
30	SC1-OVT-R	3.82	7.1	5.91
31	SC1-OUT-L	3.82	7.1	5.92
32	SAPL-A	7.19	7.1	6.04
33	AHVSUP	8	1.3	4.59
34	CAPL-M	7.2	7.1	6.04
35	AHVSS	7.2	7.1	0.00
36	ABNDC	0.01	0.001	6.02
37	SC3-ZN-L NC	3.74	7.1	6.1
38	SC3-IN-R NC	3.77	7.1	6.1
39	SC2-IN-L NC	3.77	7.1	6.1
40	SC2-IN-R NC	3.77	7.1	6.1
41	SC1-IN-L	3.77	7.1	6.1
42	SC1-IN-R	3.77	7.1	6.1
43	VREFTOP	2.6	1.6	1.63
44	WONO-IN NC	3.78	7	6.1
45	AVSS	0.01	0.001	0.00
46	AVSVP	4.9	0.7	4.53
47	ANA-IN1+	1.53	7.3	5.27
48	ANA-IN1-	1.53	7.3	5.26
49	ANA-IN2+	0.09	7.3	5.27

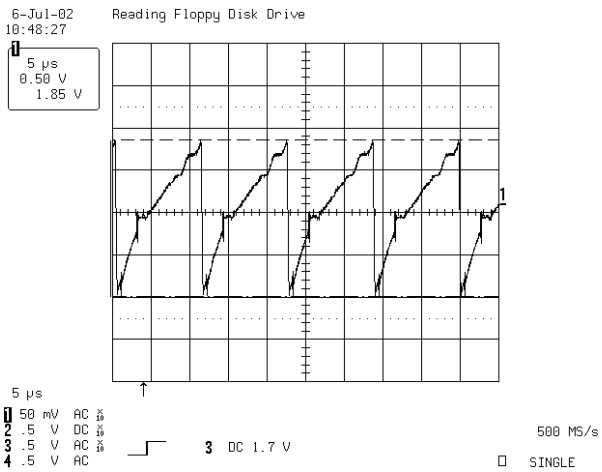
(Continued)

50	TESTEN	0.01	0.001	0.00
51	XTAL-2N	2.35	6.8	5.27
52	XTAL-OUT	2.36Hs	6.8	5.3

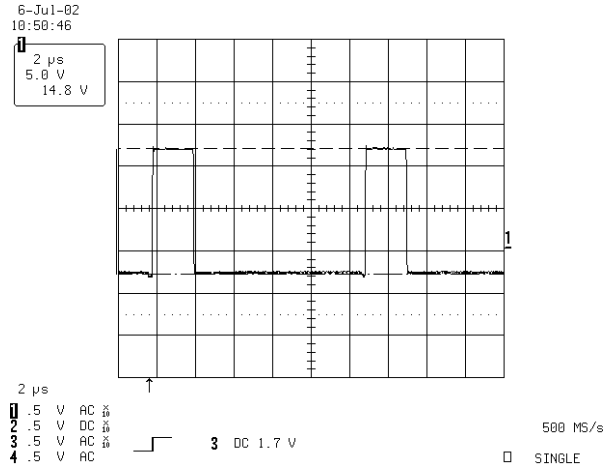
WAVEFORMS OF KEY POINTS



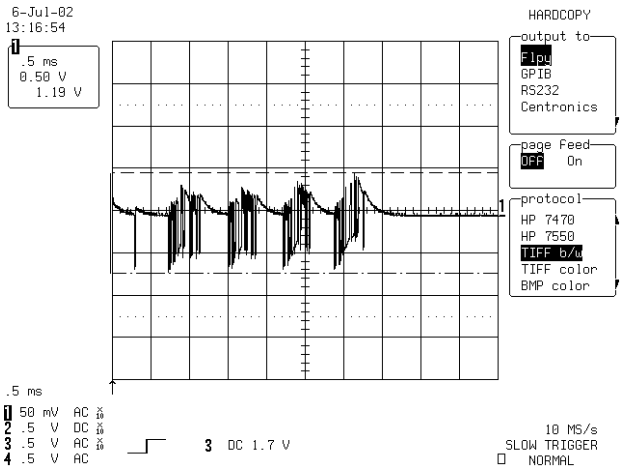
Switch Transistor QI'S Ⓓ on DVD Power PCB



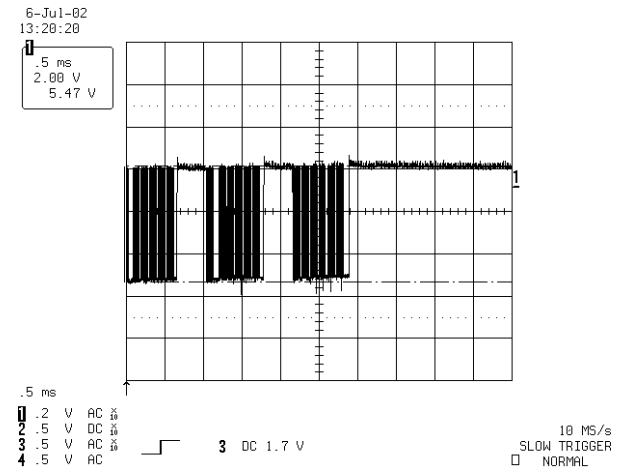
DVD Power PCB N01's Pin 4



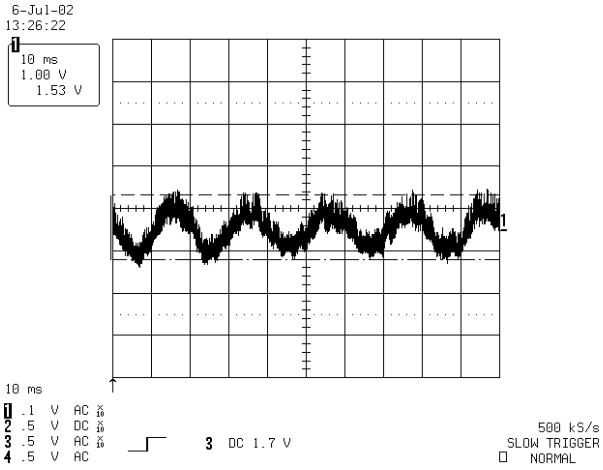
DVD Power PCB N01's Pin 6



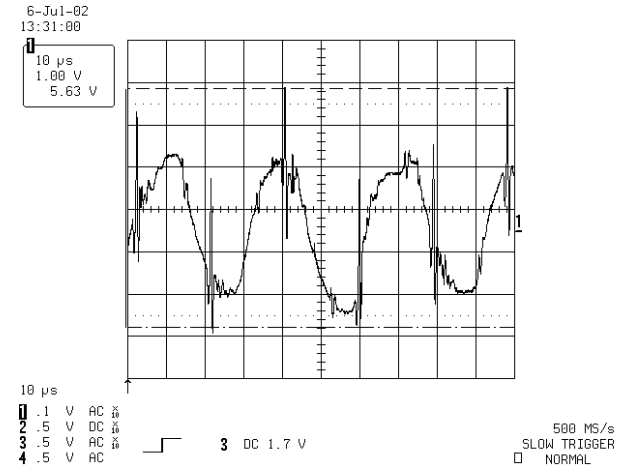
D701's Pin 3 SCL



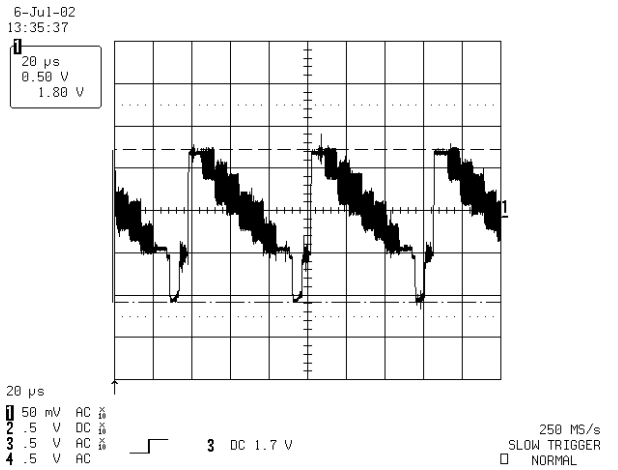
D701's Pin 4 SDA



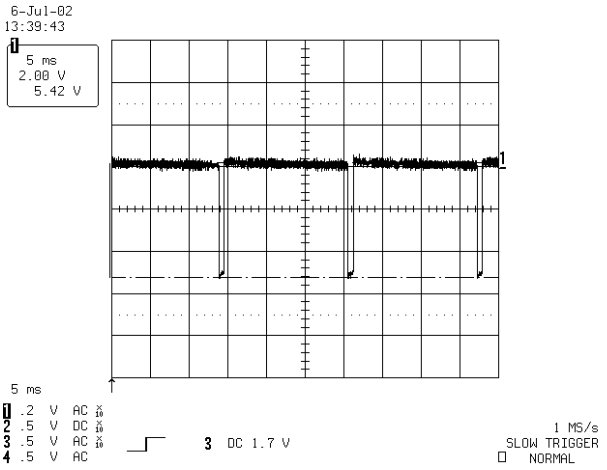
D701's Pin 6 XT1



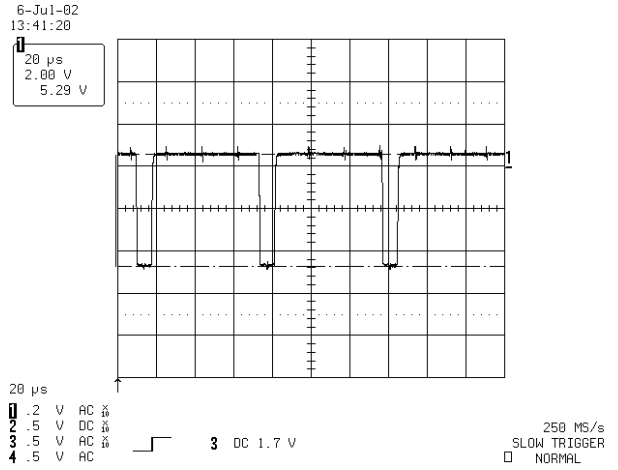
D701's Pin 7 XT2



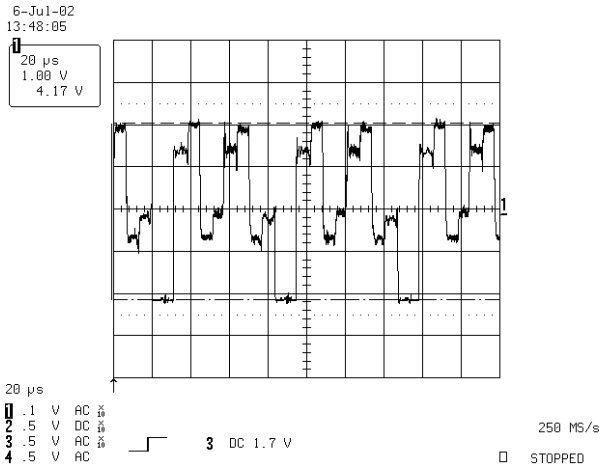
D701's Pin 15 C-VIN



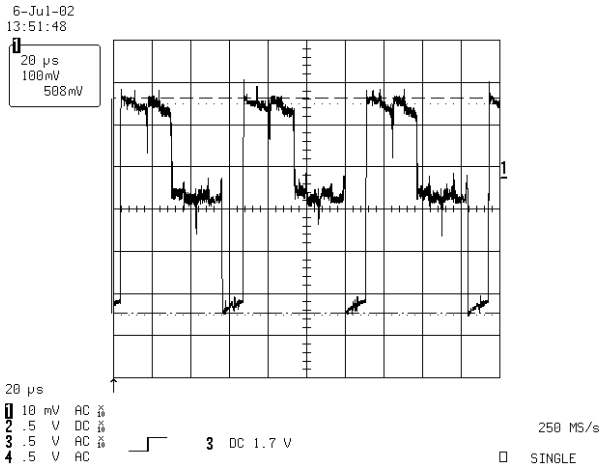
D701's Pin 17 V-SYNC



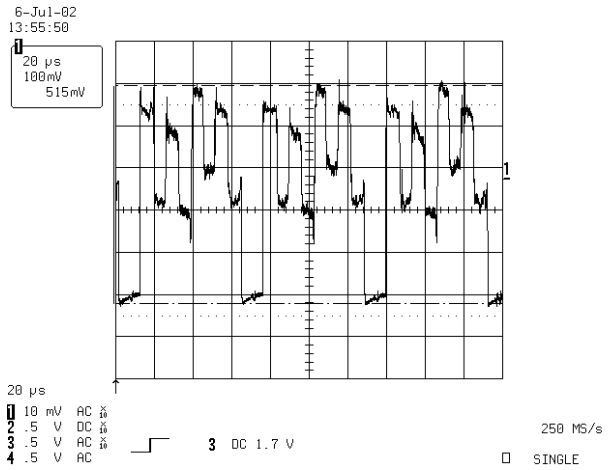
D701's Pin 18 H-SYNC



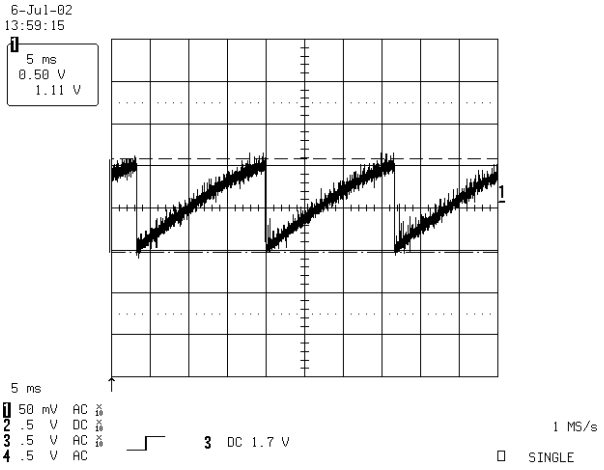
N101's Pin 19 R-OUT



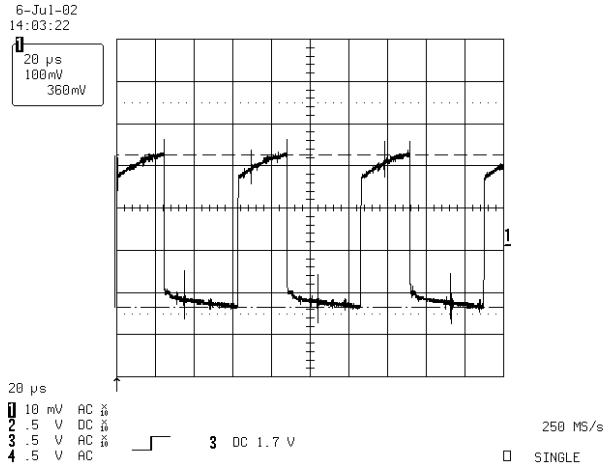
N101's Pin 20 G-OUT



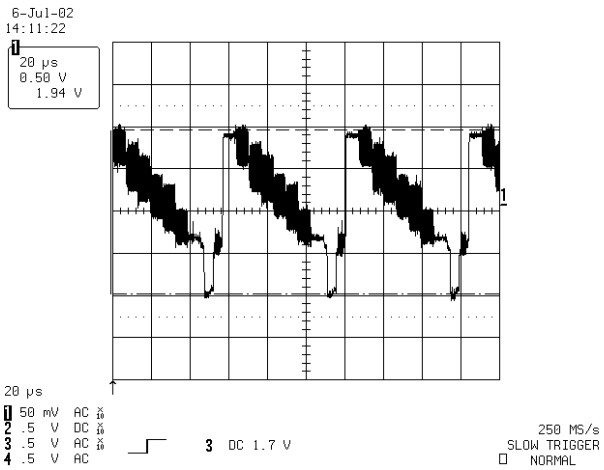
N101's Pin 21 B-OUT



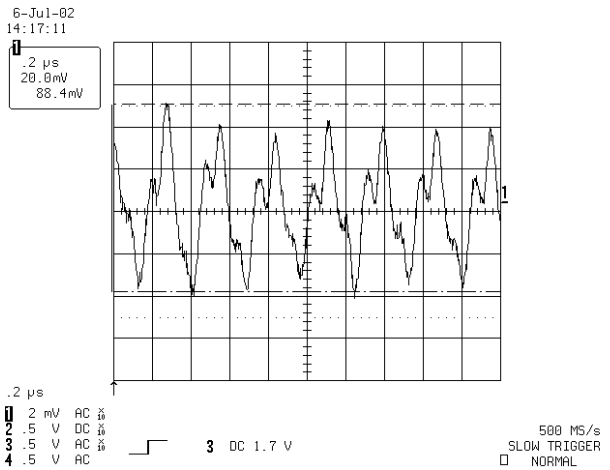
N101's Pin 23 VER-OUT



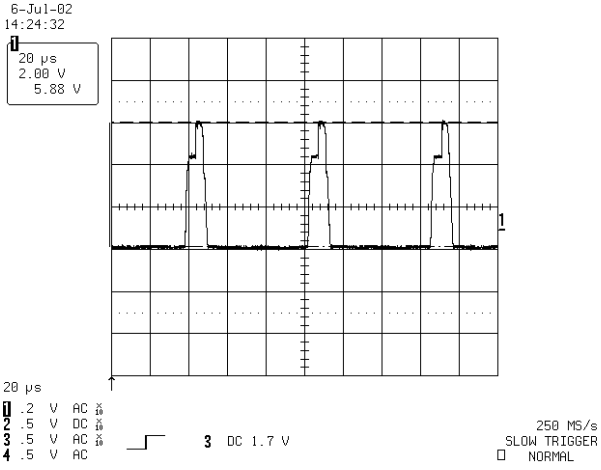
N101's Pin 27 HOR-OUT



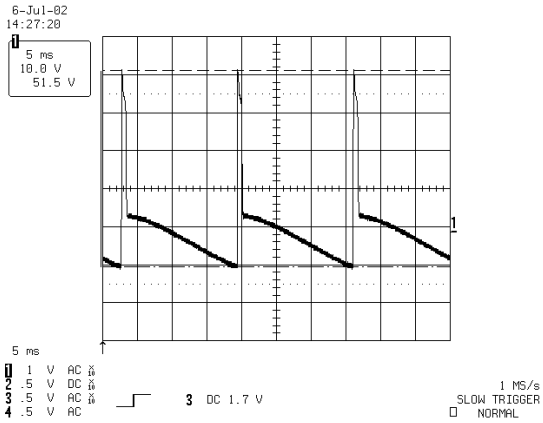
N101's Pin 46 VIDEO-OUT

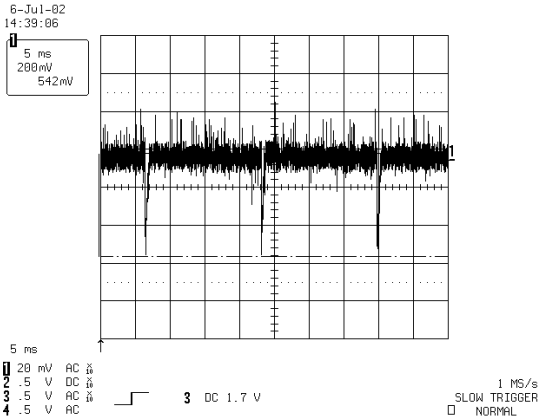


N101's Pin 38 X TAL

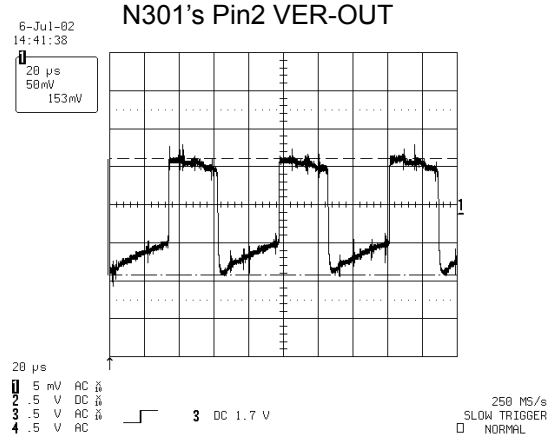


N101's Pin 28 FBP-IN



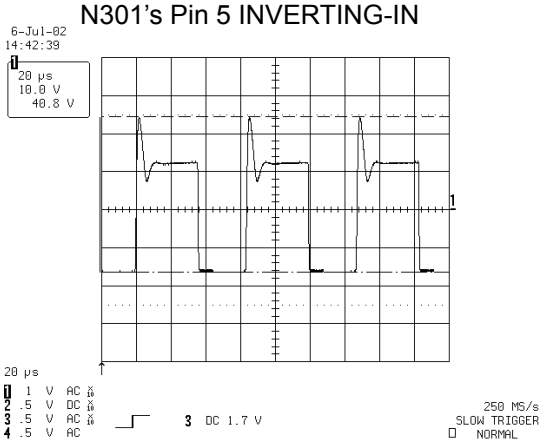


N301's Pin2 VER-OUT

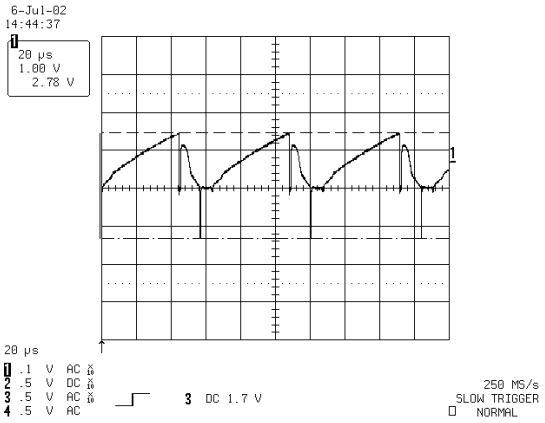


V431 (B)

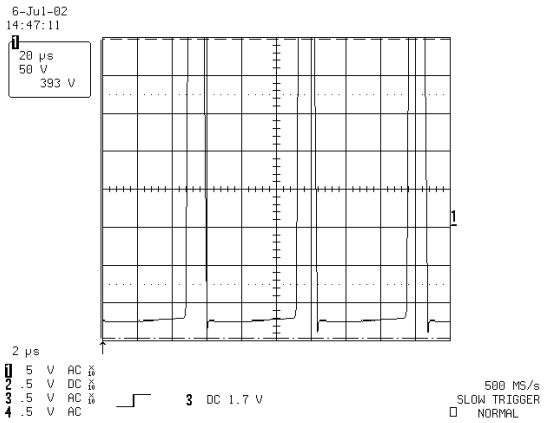
N301's Pin 5 INVERTING-IN



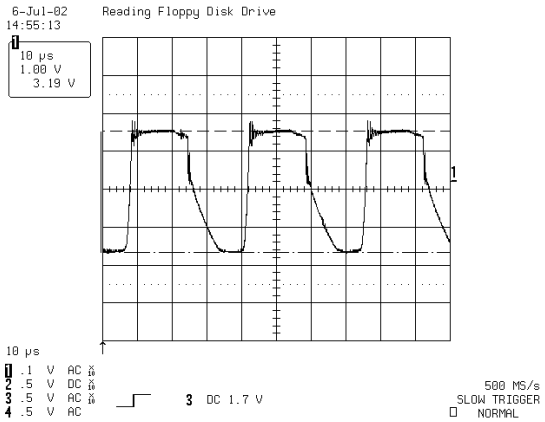
V431 (C)



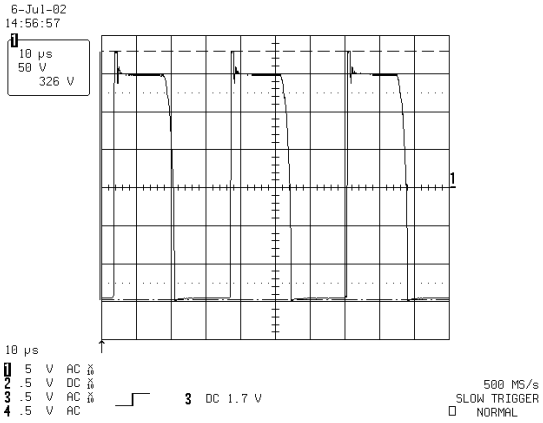
V432 (B)



V432 (C)



V513 (B)



V513 (C)

SERVICE DATA FOR DVD UNIT

TECHNICAL DATA OF KEY ICS

MT1369AE

MPEG decoder/DVD servo processor

1. Features

■ Super Integration DVD player single chip

· Servo controller and data channel processing
· MPEG-1/MPEG-2/JPEG video decoding
· AC-3/DTS/DVD-Audio/MP3 audio decoding
· Unified track buffer and A/V decoding buffer
· Video processing for scaling and video quality enhancement
· OSD & Sub-picture decoding
· Built-in clock generator

■ Speed Performance on Servo and Decoding

· DVD-ROM up to 8XS
· CD-ROM up to 24XS
· Built-in a frequency programmable clock to μp and RSPO decoder to optimize the performance over power

■ Channel Data Processor

· Provides interface with analog front-end processor
· Analog data slicer for small jitter capability
· Built-in high performance data PLL for channel data demodulation
· EFM/EFM+ data demodulation
· Enhanced channel data frame sync protection & DVD-ROM sector sync protection

■ Servo Control and Spindle Motor Control

· Programmable frequency error gain and phase error gain of spindle PLL to control spindle motor on CLV and CAV mode
· Provide a varipitch speed control for CLV and CAV mode
· Built-in ADCs and DACs for digital servo control
· Provide 2 general PWM
· Tray control can be PWM output or digital output
· Built-in DSP for digital servo control

■ Host Micro controller

· Built-in 8032 micro controller
· Built-in internal 373 and 8-bit programmable lower address port
· 256-bytes on-chip RAM
· Up to 1M bytes FLASH-programming interface
· Supports 5/3.3-Volt. FLASH interface
· Supports power-down mode
· Supports additional serial port

■ DVD-ROM/CD-ROM Decoding Logic

· Supports CD-ROM Mode 1， CD-ROM XA Mode 2 Form 1， CD-ROM XA Mode 2 Form 2， and CD-DA formats

· High-speed ECC logic capable of correcting one error per each P-codeword or Q-codeword

· Automatic sector mode and form detection
· Automatic sector header verification
· 8-bit counter for decode completion on ck
· Automatically repeated error corrections
· 8-bit C2 Pointer counter
· Decoder Error Notification Interrupt that signals various decoder errors
· Provide error correction acceleration

■ Buffer Memory Controller
· Supports 16Mb/32Mb/64Mb SDRAM
· Supports 16-bit/32-bit SDRAM data bus interface
· Build in a DRAM interface programmable clock to optimize the DRAM performance
· Provide the self-refresh mode SDRAM
· Programmable DRAM access cycle and refresh cycle timings
· Block-based sector addressing
· Programmable buffering counter for buffer status tracking
· Maximum DRAM speed is 133MHz
· Support 5/3.3-Volt. DRAM Interface

■ Video Decode
· Decodes MPEG1 video and MPEG2 main level，main profile video（720/480 and 720×576）
· Maximum input bit-rate of 15Mbits/sec
· Smooth digest view function with 1, P and B picture decoding
· Baseline, extended-sequential and progressive JPEG image decoding
· Support CD-G titles

■ Video/SPU/HLI Processor
· Arbitrary ratio vertical/horizontal scaling of video, from 0.25X to 256X
· 256/16/4/2-color bitmap format OSD
· 256/16 color RLC format OSD
· Automactic scrolling of OSD image
· Warp mode of OSD can reduce memory required
· Dual Sub-picture decoder
· Provides 4-color/32×32-pixel hardware cursor
· Fade-in，Fade out，and Wipe functions as specified in the DVD Audio Specification and other slide show transition effects

■ Audio Processing
- Decoder format supports.
- Dolby Digital (AC-3) decoding
- DTS decoding
- MLP decoding for DVD-Audio
- MPEG-1 layer 1/layer 2 audio decoding

- MPEG-2 layer1/layer2 2-channel audio decoding
- Dolby Pro Logic decoding
  - Up to 6 channel linear PCM output for DVD Audio/DVD Video
  - Downmix function
  - Support IEC 60958/61937 output
- PCM/bit stream/mute mode
- Custom IEC latency up to 2 frames

  a)
  - Pink noise and white noise generator
  - Karaoke functions
- Microphone echo with adjustable echo level, echo-depth and delay length
- Microphone tone control with three custom second-order IIR filter
- Vocal mute/vocal assistant
- Key shift up to +/-8 keys controlled by 1/2 key
  - Channel equalizer
  - 3D surround processing include virtual surround and speaker separation
  - Power-down control
  - Outline
  - 208-pin LQFP package
  - 313/216-Volt Dual perating votages

2. Pin Definitions

Pin	Symbol	Type	Description
1	IREF	Analog Input	Current reference input. It generate reference current for data PLL. Connect an external 100K resistor to this pin and PLLVSS.
2	PLLVSS	Ground	Ground for data PLL and related analog circuitry
3	LPIOP	Analog Output	Positive output of the low pass filter
4	LPION	Analog Output	Negative output of the low pass filter
5	LPFON	Analog Output	Negative output of loop filter amplifier
6	LPFIP	Analog Input	Positive input of loop filter amplifier
7	LPFIN	Analog Input	Negative input of loop filter amplifier
8	LPFOP	Analog Output	Positive output of loop filter amplifier
9	JITFO	Analog Output	RF jitter meter output
10	JITFN	Analog Input	Negative input of the operation amplifier for RF jigger meter
11	PLLVDD3	Power	Power for data PLL and related analog circuitry
12	FOO	Analog Output	Focus servo output. PDM output of focus servo compensator
13	TRO	Analog Output	Tracking servo output PDM output of focus servo compensator
14	TROPENPWM	Analog Output	Tray open output, controlled by microcontroller. This is PWM output for $TRWMEN_{27hRW2}$=1 or is digital output for $TRWMEN_{27hRW2}$=0
15	PWMOUT 2	Analog Output	The general PWM output
16	DVD2	Power	2.5V power
17	DMO	Analog Output	Disk motor control output PWM output

(Continued)

18	FMO	Analog Output	Feed motor control. PWM output
19	FG	Inout, Pull Up	Motor Hall sensor input
20	DVSS	Ground	Ground
21	HIGHA0	Inout, Pull Up	Microcontroller address 8
22	HIGHA1	Inout, Pull Up	Microcontroller address 9
23	HIGHA2	Inout, Pull Up	Microcontroller address 10
24	HIGHA3	Inout, Pull Up	Microcontroller address 11
25	HIGHA4	Inout, Pull Up	Microcontroller address 12
26	HIGHA5	Inout, Pull Up	Microcontroller address 13
27	DVSS	Ground	Ground
28	HIGHA6	Inout, Pull Up	Microcontroller address 14
29	HIGHA7	Inout, Pull Up	Microcontroller address 15
30	AD7	Inout	Microcontroller address/data 7
31	AD6	Inout	Microcontroller address/data 6
32	AD5	Inout	Microcontroller address/data 5
33	AD4	Inout	Microcontroller address/data 4
34	DVDD3	Power	3.3V power
35	AD3	Inout	Microcontroller address/data 3
36	AD2	Inout	Microcontroller address/data 2
37	AD1	Inout	Microcontroller address/data 1
38	AD0	Inout	Microcontroller address/data 0
39	IOA0	Inout, Pull Up	Microcontroller address 0/GPIO0
40	IOA1	Inout, Pull Up	Microcontroller address 1/GPIO1
41	DVDD2	Power	2.5V power
42	IOA2	Inout, Pull Up	Microcontroller address 2/GPIO2
43	IOA3	Inout, Pull Up	Microcontroller address 3/GPIO3
44	IOA4	Inout, Pull Up	Microcontroller address 4/GPIO4
45	IOA5	Inout, Pull Up	Microcontroller address 5/GPIO5
46	IOA6	Inout, Pull Up	Microcontroller address 6/GPIO6
47	IOA7	Inout, Pull Up	Micro controller address 7/GPIO7
48	A16	Output	Flash address 16
49	A17	Output	Flash address 17
50	IOA18	Inout	Flash address 18/GPIO10
51	KOA19	Inout	Flash address 19/GPIO11
52	DMVSS	Ground	Ground for DRAM clock circuitry
53	DMVDD3	Power	Power for DRAM clock circuitry
54	ALE	Inout, Pull Up	Microcontroller address latch enable
55	LOOE#	Inout	Flash output enable, active low/GPIO13
56	LOWR#	Inout	Flash write enable, active low/GPIO17
57	LOCS#	Inout, Pull Up	Flash chip select, active low/GPIO18
58	DVSS	Ground	Ground
59	UP1-2	Inout, Pull Up	Microcontroller port 1-2
60	UP1-3	Inout, Pull Up	Microcontroller port 1-3
61	UP1-4	Inout, Pull Up	Microcontroller port 1-4

(Continued)

62	UP1-5	Inout, Pull Up	Microcontroller port 1-5
63	UP1-6	Inout, Pull Up	Microcontroller port 1-6
64	DVDD3	Power	3.3V power
65	UP1-7	Inout, Pull Up	Microcontroller port 1-7
66	UP3-0	Inout, Pull Up	Microcontroller port 3-0
67	UP3-1	Inout, Pull Up	Microcontroller port 3-1
68	INT0#	Inout, Pull Up	Microcontroller interrupt 0, active low
69	IR	Input	IR control signal input
70	DVDD2	Power	2.5V power
71	UP3-4	Inout	Microcontroller port 3-4
72	UP3-5	Inout	Microcontroller port 3-5
73	UWR#	Inout, Pull Up	Microcontroller write strobe, active low
74	URD#	Inout, Pull Up	Microcontroller read strobe, active low
75	XTALI	Input	Crystal input, 27MHz
76	XTALO	Output	Crystal output
77	DVSS	Ground	Ground
78	RD7	Inout	DRAM data 7
79	RD6	Inout	DRAM data 6
80	RD5	Inout	DRAM data 5
81	RD4	Inout	DRAM data 4
82	DVDD2	Power	2.5V power
83	RD3	Inout	DRAM data 3
84	RD2	Inout	DRAM data 2
85	RD1	Inout	DRAM data 1
86	RD0	Inout	DRAM data 0
87	RWE#	Output	DRAM write enable, active low
88	CAS#	Output	DRAM column address strobe, active low
89	RAS#	Output	DRAM row address strobe, active low
90	RCS#	Output	DRAM chip select, active low
91	BA0	Output	DRAM bank address 0
92	DVDD3	Power	3.3V power
93	RD15	Inout, Pull Up/Down	DRAM data 15
94	RD14	Inout, Pull Up/Down	DRAM data 14
95	RD13	Inout, Pull Up/Down	DRAM data 13
96	RD12	Inout, Pull Up/Down	DRAM data 12
97	DVSS	Ground	Ground
98	RD11	Inout, Pull Up/Down	DRAM data 11
99	RD10	Inout, Pull Up/Down	DRAM data 10
100	RD9	Inout, Pull Up/Down	DRAM data 9
101	RD8	Inout, Pull Up/Down	DRAM data 8
102	VPVDD3	Power	Power for varipitch VCO circuitry
103	VCOCIN	Analog Input	Connect capacitor for compensator loop filter
104	VPVSS	Ground	Ground for varipitch VCO circuitry
105	DVSS	Ground	Ground

(Continued)

106	CLK	Output	DRAM clock
107	CLE	Output	DRAM clock enable
108	RA11	Output	DRAM address bit 11 or audio serial data 3 (channel 3/8)
109	RA9	Output	DRAM address 9
110	RA8	Output	DRAM address 8
111	DVDD2	Power	2.5V power
112	RA7	Output	DRAM address 7
113	RA6	Output	DRAM address 6
114	RA5	Output	DRAM address 5
115	RA4	Output	DRAM address 4
116	DVSS	Ground	Ground
117	DQM1	Output	Mask for DRAM input/output byte 1
118	DQM0	Output	Mask for DRAM input/output byte 0
119	BA1	Output	DRAM bank address 0
120	RA10	Output	DRAM address 10
121	DVDD2	Power	2.5V power
122	RA0	Output	DRAM address 0
123	RA1	Output	DRAM address 1
124	RA2	Output	DRAM address 2
125	RA3	Output	DRAM address 3
126	DVSS	Ground	Ground
127	RD31	Inout, Pull Up/Down	DRAM data 31
128	RD30	Inout, Pull Up/Down	DRAM data 30
129	RD29	Inout, Pull Up/Down	DRAM data 29
130	RD28	Inout, Pull Up/Down	DRAM data 28
131	DVDD3	Power	3.3V power
132	RD27	Inout, Pull Up/Down	DRAM data 27
133	RD26	Inout, Pull Up/Down	DRAM data 26
134	RD25	Inout, Pull Up/Down	DRAM data 25
135	RD24	Inout, Pull Up/Down	DRAM data 24
136	DVSS	Ground	Ground
137	DQM3	Output	Mask for DRAM input/output byte 3
138	DQM2	Output	Mask for DRAM input/output byte 2
139	RD23	Inout, Pull Up/Down	DRAM data 23
140	RD22	Inout, Pull Up/Down	DRAM data 22
141	DVDD2	Power	2.5V power
142	RD21	Inout, Pull Up/Down	DRAM data 21
143	RD20	Inout, Pull Up/Down	DRAM data 20
144	RD19	Inout, Pull Up/Down	DRAM data 19
145	RD18	Inout, Pull Up/Down	DRAM data 18
146	DVSS	Guound	Ground
147	RD17	Inout, Pull Up/Down	DRAM data 17
148	RD16	Inout, Pull Up/Down	DRAM data 16
149	ABCK	Output	Audio bit clock

(Continued)

150	ALRCK	Inout, Pull Down	(1) Audio left/right channel clock (2) Trap value in power-on reset. 1:use external 373, 0:use internal 373
151	DVDD3	Power	3.3V power
152	ASDATA0	Inout, Pull Down	Audio serial data 0 (left/right channel)
153	ASDATA1	Inout, Pull Down	Audio serial data 1 (surround left/surround right channel)
154	ASDATA2	Inout, Pull Down	Audio serial data 2 (center/LFE channel)
155	ACLK	Inout	Audio DAC master clock (384/256 audio sample frequency)
156	APVDD8	Power	Power for audio clock circuitry
157	APVSS	Ground	Ground for audio clock circuitry
158	SPDIE	Output	SPDIF output
159	MC-DAT	Input	Miorophone serial input
160	BLANK#	Inout	Video blank area, active low/GPIO14
161	VSYN	Inout	Vertical sync/GPIO16
162	HSYN	Inout	Horizontal sync/GPIO15
163	DVSS	Ground	Ground
164	YUV0	Output	Video data output bit 0
165	YUV1	Output	Video data output bit 1
166	YUV2	Output	Video data output bit 2
167	YUV3	Output	Video data output bit 3
168	YUV4	Output	Video data output bit 4
169	DVDD2	Power	2.5V power
170	YUV5	Output	Video data output bit 5
171	YUV6	Output	Video data output bit 6
172	YUV7	Output	Video data output bit 7
173	ICE	Input, Pull Down	Microcontroller ICE mode enable
174	PRST	Input, Pull Down	Power on reset input, active high
175	DVSS	Ground	Ground
176	VFO13	Output	The 1st, 3rd VFO pulse output of DVD-RAM ID header
177	IDGATE	Output	DVD-RAM ID header detect signal output
178	DVDD3	Power	3.3V power
179	UDGATE	Output	DVD-RAM recording data gate singal output
180	WOBSI	Input	Wobble signal output
181	SDATA	Output	RF serial data output
182	SDEN	Output	RF serial data latch enable
183	SLCK	Output	RF serial clock output
184	BDO	Input, Pull Down	Flag of defect data status input
185	DVDD3	Power	3.3V power
186	PDMVDD3	Power	Power for PDM circuitry
187	PWMVREF	Analog Input	A reference voltage input for PWM circuitry. A typical value of 2.8v
188	PWM2VREF	Analog Input	A reference voltage input for PWM circuitry. A typical value of 1.4v
189	PDMVSS	Ground	Ground for PDM circuitry
190	ADCVSS	Ground	Ground for ADC circuitry
191	ADIN	Analog Input	General AVD input

(Continued)

192	RFSUBI	Analog Input	RF subtraction signal input terminal
193	TEZISLV	Analog Input	Tracking error zero crossing low pass input
194	TEI	Analog Input	Tracking error input
195	CSO	Analog Input	Central servo input
196	FEI	Analog Input	Focus error input
197	RFLEVEL	Analog Input	Sub beam add input or RFRP low pass input
198	RFRP-DC	Analog Input	RF ripple detect input
199	RFRP-AC	Analog Input	RF ripple detect input (through AC coupling)
200	RFRPSLV	Analog Input	RFRP slice level input
201	HRFZC	Analog Input	High frequency RF ripple zero crossing
202	ADCVDD8	Power	Power for ADC circuitry
203	RADTSI VP	Analog Output	Positive RF data slicer level output
204	SCON	Analog Output	Negative analog slicer current output
205	SCOP	Analog Output	Positive analog slicer current output
206	RFDTSLVN	Analog Output	Negative RF data slicer level output
207	RFIN	Analog Input	Negative input of RF differential signal
208	RFP	Analog Input	Positive input of RF differential signal

MT1336E

RF amplifier

1.General Description

MT1336 is a high performance CMOS analog front-end IC for both CD_ROM driver up to 48XS and DVD_ROM driver up to 16XS. It also supports DVD_RAM lead up to 4XS Version 2. It contains servo amplifiers to generate focusing error, 3-beam tracking error, 1 beam radial push-pull signal, RF level and SBAD for servo functions. It also includes DPD tracking error signal for DVD_ROM application. For DVD_RAM disks, there are also Differential Push-Pull (DPP) method for generating tracking signal and Differential Astigmatic Detection (DAD) for processing focusing signal. Programmable equalizer and AGC circuits are also incorporated in this chip to optimize read channel performance. In addition, this chip has dual automatic laser power control circuits for DVD-ROM (DVD-RAM) and CD-ROM separately and reference voltage generators to reduce external components. Programmable functions are implemented by the access of internal register through bi-directional serial port to configure modes selection.

2. Features

- RF equalizer with programmable fc from 3MHz to 70MHz and programmable boost from 3dB to 13dB.
- MT1336 supports at least eight different kinds of pick-up heads with versatile input configuration for both RF input stages and servo signal blocks.
- 3 beams tracking error signal generator for CD_ROM application.
- One beam differential phase tracking error (DPD) generator for DVD_ROM application.
- Differential push pull tracking error (DPP) generator for DVD_RAM application.
- Focusing error signal generator for CD-ROM, DVD-ROM and DVD-RAM (DAD method).
- RF level signal generator.
- Sub-beam added signal for 3 beams CD-ROM.
- One beam push-pull signal generator for central servo application.
- High speed RF envelop detection circuit with bandwidth up to 400KHz for CD-ROM.
- Defect and Blank detection circuits.
- Dual automatic laser power control circuits with programmable level of LD monitor voltage.
- Vref=1.4V voltage and V2ref=2.8V voltage generators.
- V20=2.0V voltage for pick-up head reference.
- Bi-directional serial port to access internal registers.
- 128-pin LQFP.

3. block Diagram

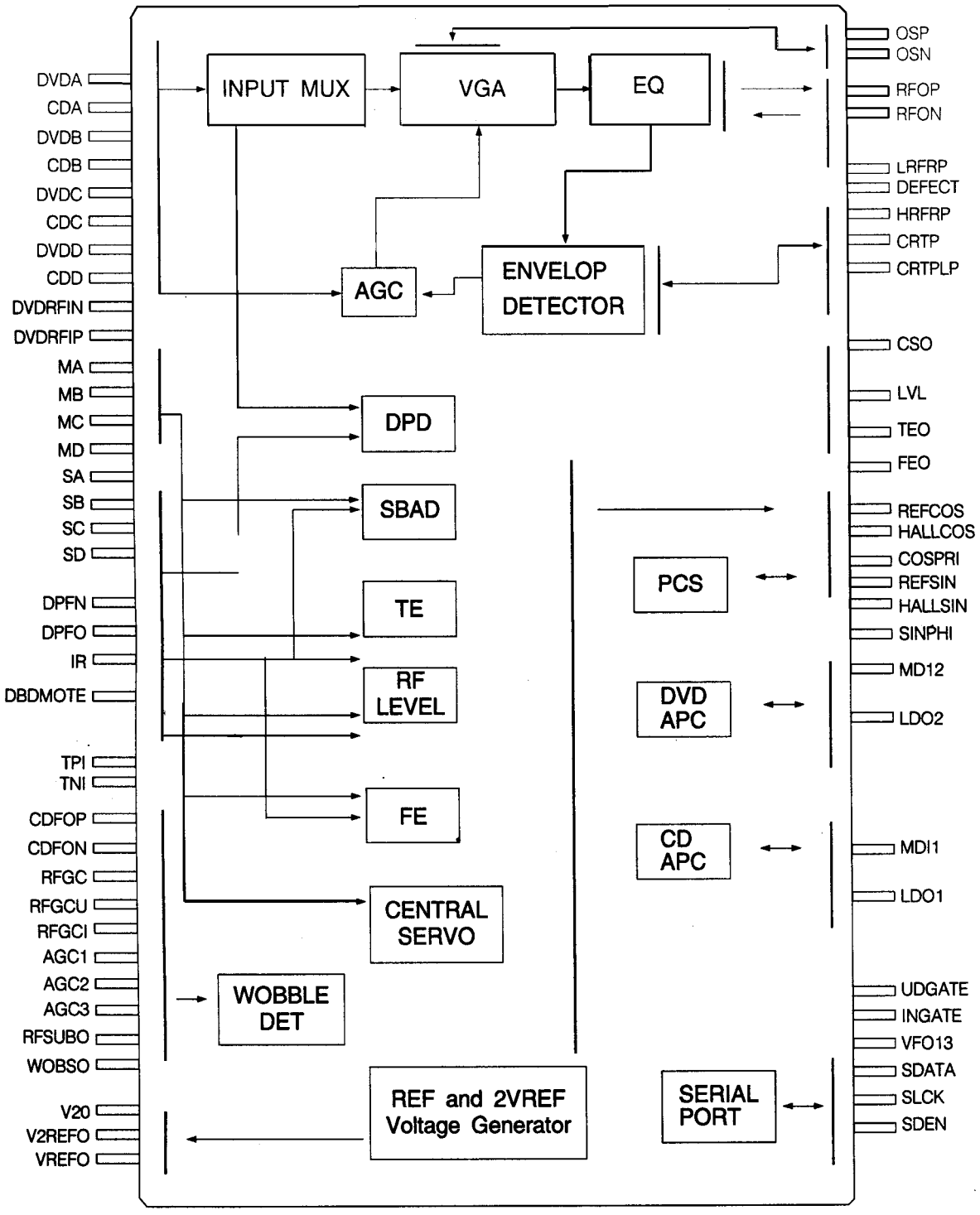


Fig17. MT1336 Function Block Diagram

4.MT1336 Pin Descriptions

Pin Numbers	Symbol	Type	Description
LQFP128			
RF Flag Interface			
23	DEFECT	Digital Output	Flag of bad data output status
RF SIO interface			
56	SCLK	Digital Input	RF serial clock input
58	SDEN	Digital Input	RF serial data input
59	SDATA	Digital IO	RF serial data IO
60	RST	Digital Input	Reset(active high)
55	XCK16M	Digital Input	16.9MHz for verification
RF SERVO interface			
40	UOG ATE	Digital Input	Control signal for DVD-RAM
41	GGATE	Digital Input	Control signal for DVD RAM
38	VFO13	Digital Input	DVD-RAM Header signal
RF			
100	DVDA	Analog Input	AC coupled DVD RF signal input A
99	DVDB	Analog Input	AC coupled DVD RF signal input B
98	DVDC	Analog Input	AC coupled DVD RF signal input C
97	DVDD	Analog Input	AC coupled DVD RF signal input D
95	DVDRFIN	Analog Input	AC coupled DVD RF signal input RFIN
96	DVDRFIP	Analog Input	AC coupled DVD RF signal input RFIP
94	CDA	Analog Input	AC coupled CD RF signal input A
93	CDB	Analog Input	AC coupled CD RF signal input B
92	CDC	Analog Input	AC coupled CD RF signal input C
91	CDD	Analog Input	AC coupled CD RF signal input D
90	OSN	Analog	RF offset cancellation capacitor connecting
89	OSP	Analog	RF offset cancellation capacitor connecting
85	CEQP	Analog	RF offset cancellation capacitor connecting
84	CEQN	Analog	RF offset cancellation capacitor connecting
88	RFGC	Analog	RF AGC loop capacitor connecting for DVD-ROM
87	RFGCU	Analog	RF AGC loop capacitor connecting for DVD-RAM
86	RFGCU	Analog	RF AGC loop capacitor connecting for DVD-RAM
101	MA	Analog Input	DC coupled DVD-RAM main-beam RF signal input A

(Continued)

102	MB	Analog Input	DC coupled DVD-RAM main-beam RF signal input B
103	MC	Analog Input	DC coupled DVD-RAM main-beam RF signal input C
104	MD	Analog Input	DC coupled DVD-RAM main-beam RF signal input D
105	SA	Analog Input	DC coupled DVD-RAM sub-beam RF signal input A
106	SB	Analog Input	DC coupled DVD-RAM sub-beam RF signal input B
110	SC	Analog Input	DC coupled DVD-RAM sub-beam RF signal input C
111	SD	Analog Input	DC coupled DVD-RAM sub-beam RF signal input D
108	IR	Analog	External current bias resistor (R=20K)
119	AGC1	Analog	Wobble AGC loop1 capacitor
121	AGC2	Analog	Wobble AGC loop2 capacitor
122	AGC3	Analog	Wobble AGC loop3 capacitor
127	RFSUBO	Analog Output	Header push-pull RF output signal
	V OBSO	Digital Output	Wobble signal output
5	RFOP	Analog Output	RF positive output
7	PFON	Analog Output	RF negative output
TRACKING ERROR			
32	DPFN	Analog	DPD amplifier negative input
33	DPFO	Analog	DPD amplifier output
61	DPDMUTE	Digital Input	DPD mute control input
116	TNI	Analog Input	3 beam satellite PD signal negative input E
115	TPI	Analog Input	3 beam satellite PD signal negative input F
21	TEO	Analog Output	Tracking error output
FOCUSING ERROR & RF LEVEL & CENTRAL SERVO SIGNAL			
112	CDFOP	Analog Input	CD focusing error positive input
113	CDFON	Analog Input	CD focusing error negative input
18	FEO	Analog Output	Focusing error output
19	LVL	Analog Output	RF level output
20	CSO	Analog Output	Central servo signal output
ALPC			
124	MDI1	Analog Input	Laser power monitor input
125	LDO1	Analog Output	Laser driver output
123	MDI2	Analog Input	Laser power monitor input

126	LDO2	Analog Output	Laser driver output
RF RIPPLE			
26	CRTP	Analog	RF top envelop filter capacitor connecting
27	CRTPLP	Analog	Defect level filter capacitor connecting
25	HRFRP	Analog output	High frequency RF ripple output or Blank detector's output
24	LRFRP	Analog output	Low frequency RF ripple output
POWER			
67, 69	AVDD	Power	Master PLL filter power
65, 73	AGND	GND	GND for Master PLL filter
64	AVDD	Power	DPD Power
62	AGND	GND	DPD GND
109	AVDD	Power	RF path Power
107	AGND	GND	RF path GND
114	SVDD	Power	Servo Power
117	SGND	GND	Servo GND
2,120	WAVDD	Power	Wobble Power
128, 118	WAGND	GND	Wobble GND
5	AVDDO	Power	Power for RF output
8	AGNDO	GND	GND for RF output
14	AVDDT	Power	Power for trimming PAD
12	AGNDT	GND	GND for trimming PAD
22	VDDP	Power	Peak Detection Power
31	GNDP	GND	Peak Detection GND
37, 54	VDD	Power	Serial I/O Power
39, 57	GND	GND	Serial I/O GND
REFERENCE VOLTAGE			
16	VREFO	Analog output	Reference voltage 1.4V
15	V2REFO	Analog output	Reference voltage 2.8V
17	V20	Analog output	Reference voltage 2.0V
ALPC TRIMMING			
9	TM1	Analog input	Trimming pin for ALPC1
10	TM2	Analog input	Trimming pin for ALPC1
11	TM3	Analog input	Trimming pin for ALPC2
13	TM4	Analog input	Trimming pin for ALPC2
HIGH SPEED TRACK COUNTING			
29	TRLP	Analog	Low-pass filter capacitor connecting

(Continued)

28	TRLPA	Analog	Low-pass filter capacitor connecting
30	HTRC	Digital output	High speed track counting digital output
PCS			
74	HALLSIN	Analog input	Negative input of amplifier for hall sensor signal
75	REFSIN	Analog input	Positive input of amplifier for hall sensor signal
76	SINPHI	Analog output	Amplifier output for hall sensor signal
71	HALLCOS	Analog input	Negative input of amplifier for hall sensor signal
72	REFCOS	Analog input	Positive input of amplifier for hall sensor signal
70	COSPHI	Analog output	Amplifier output for hall sensor signal
FOR MONITOR ONLY			
81	MON	Analog output	
80	MOP	Analog output	
66	VCON	Analog output	
77	SWO	Analog output	Output from mux of SW1 & SW2
78	SW2	Analog input	External input for servo input select
79	SW1	Analog input	External input for servo input select
FOR SERIAL I/O			
42	IO0		
43	IO1		
44	IO2		
45	IO3		
46	IO4		
47	IO5		

CS4334

Audio D/A Controller

1. Features

- Complete Stereo DAC System: Interpolation, D/A, Output Analog Filtering
- 24-Bit Conversion
- 96 dB Dynamic Range
- –88 dB THD+N
- Low Clock jitter Sensitivity
- Single +5V Power Supply
- Filtered Line Level Outputs
- On-Chip Digital De-emphasis
- Popguard™ Technology
- Functionally Compatible with CS4330/31/33

2. Description

The CS4334 family members are complete, stereo digital-to-analog output systems including interpolation, 1-bit D/A conversion and output analog filtering in an 8-pin package. The CS4334/5/6/7/8/9 support all major audio data interface formats, and the individual devices differ only in the supported interface format.

The CS4334 family is based on delta-sigma modulation, where the modulator output controls the reference voltage input to an ultra-linear analog low-pass filter. This architecture allows for infinite adjustment of sample rate between 2 kHz and 100 kHz simply by changing the master clock frequency.

The CS4334 family contains on-chip digital de-emphasis, operates from a single +5V power supply, and requires minimal support dircuitry. These features are ideal for set-top boxes, DVD players, SVCD players, and A/V receivers.

3. Block Diagram

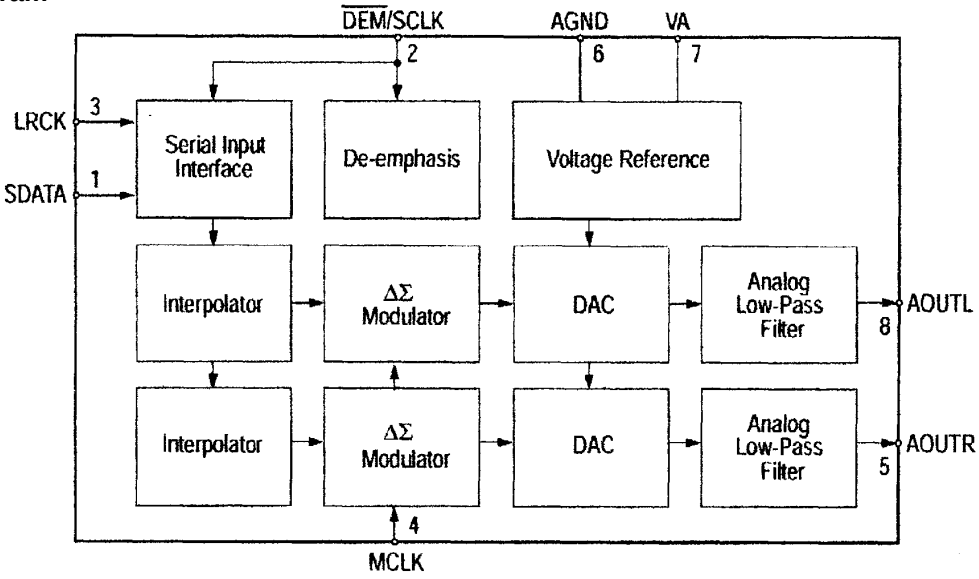


Fig.18

CS4955

Video Encoder

1. Features

- Six DACs providing simultaneous composite, S-Video, and RGB or Component YUV outputs
- Programmable DAC output currents for low impedance (37.5 Ω) and high impedance (150 Ω) loads.
- Multi-standard support for NTSC-M, NTSC-JAPAN, PAL (B, D, G, H, I, M, N, Combination N)
- ITU R.BT656 input mode supporting EAV/SAV codes and CCIR601 Master/Slave input modes
- Programmable HSYNC and VSYNC timing Multistandard Teletext (Europe, NABTS, WST) support
- VBI encoding support
- Wide-Screen Signaling (WSS) support, EIA-J CPX1204
- NTSC closed caption encoder with interrupt
- CS4955 supports Macrovision copy protection Version 7
- Host interface configurable for parallel or I^2C compatible operation
- On-chip voltage reference generator
- +3.3 V or +5V operation CMOS. low-power modes, tri-state DACs

2. Description

The CS4954/5 provides full conversion from digital video formats YCbCr or YUV into NTSC and PAL Composite, Y/C (S-Video) and RGB, or YUV analog video. Input formats can be 27 MHz 8-bit YUV, 8-bit YCbCr, or ITU R.BT656 with support for EAV/SAV codes. Video output can be formatted to be compatible with NTSC-M, NTSC-J, PAL-B, D, G, H, I, M, N, and combination N systems. Closed Caption is supported in NTSC. Teletext is supported for NTSC and PAL.

Six 10-bit DACs provide two channels for an S-Video output port, one or two composite video outputs, and three RGB or YUV outputs. Two-times oversampling reduces the output filter requirements and guarantees no DAC-related modulation components within the specified bandwidth of any of the supported video standards.

Parallel or high-speed I^2C compatible control interfaces are provided for flexibility in system design. The parallel interface doubles as a general purpose I/O port when the CS4954/5 is in I^2C mode to help conserve valuable board area.

Package:

CS4954CQ/CS4955CQ 48-Pin TQFP

3. Block Diagram

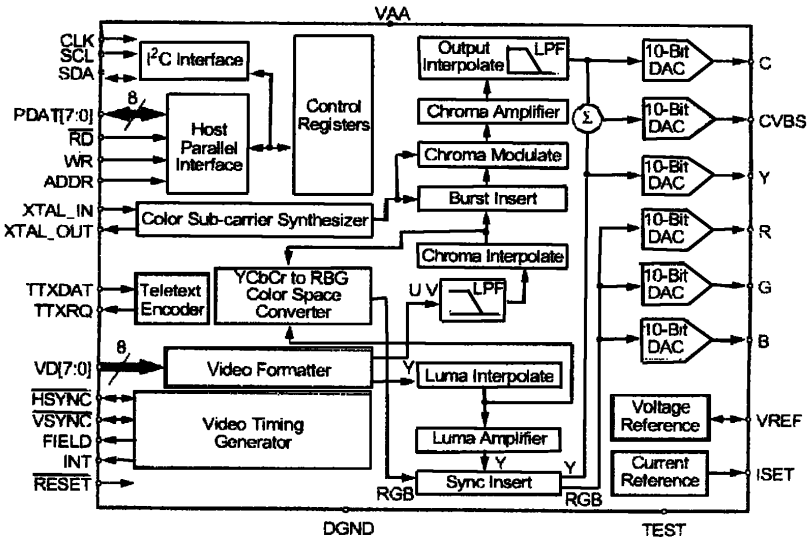


Fig. 19

BA5954

Focus/tracking Coil and Feed Motor Drive

1. Functions

- BA5954FM is a 4 channel driver for optical disc motor driver. Dual channel current feedback type drivers are built in, in addition to dual channel motor drivers.
- Wide dynamic range (4.0V (typ.) at PreVcc=12V, PVcc=5V, RL=8Ω)
- Separating Vcc into Pre+Power of sled motor, Power of loading motor and Power of actuator, can make better power efficiency, by low supply voltage drive.
- Level shift circuit built in.
- Thermal-shut-down circuit built in.
- Stand-by mode built in.

<Actuator driver>

Current phase lag influenced load inductance is little, because this type is current feedback.

< Sled motor driver >

Input pins consist of (+) and (-), therefore various input types are available such as differential input.

<Loading driver >

This is a single input linear BTL driver.

2. Pin Description

No.	Symbol	Function	No.	Symbol	Function
1	VINFC	Input for focus driver	15	VOTK+	Non inverted output of tracking
2	CFCerr1	Connection with capacitor for error amplifier	16	VOTK-	Inverted output of tracking
3	CFCerr2		17	VOLD+	Non inverted output of loading
4	VINSL+	Non inverting input for Op-amp	18	VOLD-	Inverted output of loading
5	VINSL-	Inverting input for OP-amp	19	PGND	GND for power block
6	VOSL	Output of OP-amp	20	VNFTK	Feedback for tracking driver
7	VNFFC	Feedback for focus driver	21	PVcc2	Vcc for power block of actuator
8	Vcc	Vcc for pre-drive block and power block of sled	22	PreGND	GND for pre-drive block
9	PVcc1	Vcc for power block of loading	23	VINLD	Input for loading driver
10	PGND	GND for power block	24	CTKerr2	Connection with capacitor for error amplifier
11	VOSL-	Inverted output of sled	25	CTKerr1	
12	VOSL+	Non inverted output of sled	26	VINTK	Input for tracking driver
13	VOFC-	Inverted output of focus	27	BIAS	Input for reference voltage
14	VOFC+	Non inverted output of focus	28	STBY	Input for stand-by control

Notes: Symbol of + and – (output of drivers) means polarity to input pin.
(For example if voltage of Pin1 is high, Pin14 is high.)

NJM4558M

Sound Amplifier

1. General Description

The NJM4558/4559 integrated circuit are a dual high-gain operational amplifier internally compensated and constructed on a single silicon chip using an advanced epitaxial process. Combining the features of the NJM741 with the close parameter matching and tracking of a dual device on a monolithic chip results in unique performance characteristics. Excellent channel separation allow the use of the dual device in single NJM741 operational amplifier applications providing density. It is especially well suited for applications in differential-in, differential-out as well as in potentiometric amplifiers and where gain and phase matched channels are mandatory.

5. Package Outline

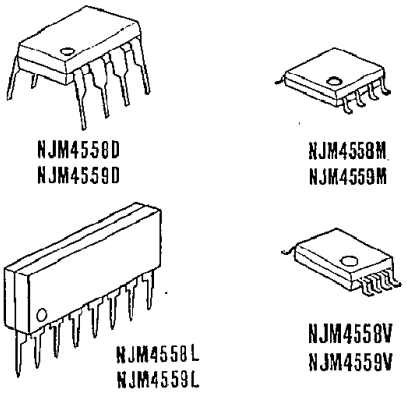


Fig. 20

2. Features

- Operating Voltage (±4V～±18V)
- High Voltage Gain (100dB typ.)
- High Input Resistance (5MΩ typ.)
- Rackage Outline DIP8. DMP8. SIP8. SSOP8
- Bipolar Technology

3. Pin Configuration

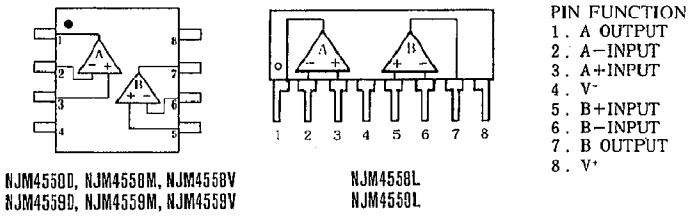


Fig. 21

4. Equivalent Circuit (1/2 Shown)

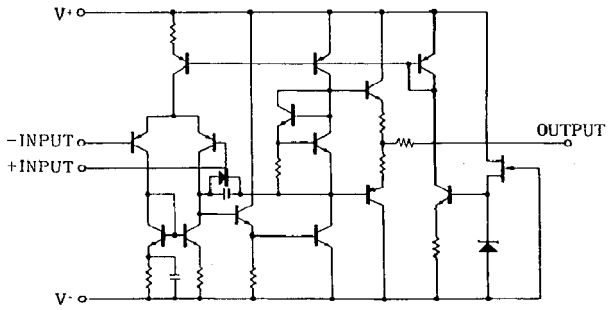


Fig. 22

1K EEPROM

1. Features

- Single supply with 5.0V operation
- Low power CMOS technology
  - 1 mA active current typical
  - 10 μA standby current typical at 5.0V
  - 5 μA standby current typical at 5.0V
- Organized as a single block of 128 bytes (128×8) or 256 bytes (256×8)
- 2-wire serial interface bus, I^2C compatible
- 100KHz compatibility
- Self-timed write cycle(including auto-erase)
- Page-write buffer for up to 8 bytes
- 2 ms typical write cycle time for page-write
- Hardware write protect for entire memory
- Can be operated as a serial ROM
- ESD protection ＞ 3,000V
- 1,000,000 ERASE/WRITE cycles guaranteed
  Data retention ＞ 200 years
- 8 pin DIP or SOIC package
- Available for extended temperature ranges
  - Automotive(E) -40℃ to +125℃

2. Description

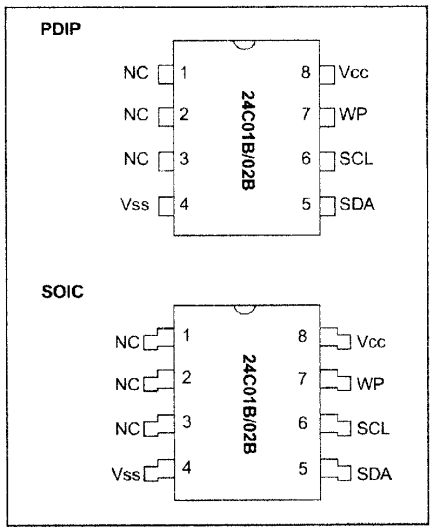
The Microchip Technology Inc. 24C01B and 24C02B are 1K bit and 2K bit Electrically Erasable PROMs The devices are organized as a single block of 128×8 bit or 256×8 bit memory with a 2-wire serial interface. The 24C01B and 24C02B also have page-write capability for up to 8 bytes of data. The 24C01B and 24C02B are available in the standard 8-pin DIP and an 8-pin surface mount SOIC package.

These devices are for extended temperature applications only. It is recommended that all other applications use Microchip's 24LC01B/02B.

Pin Function Table

Name	Function
Vss	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
Vcc	+5.0V Power Supply
NC	No Internal Connection

3. Package Types



4. Block Diagram

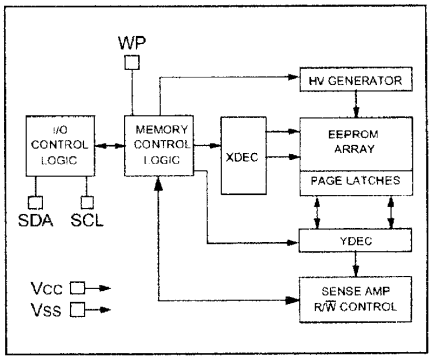


Fig. 23

SERVICE DATA OF KEY ICS

Table 14 Service Data of Key ICs

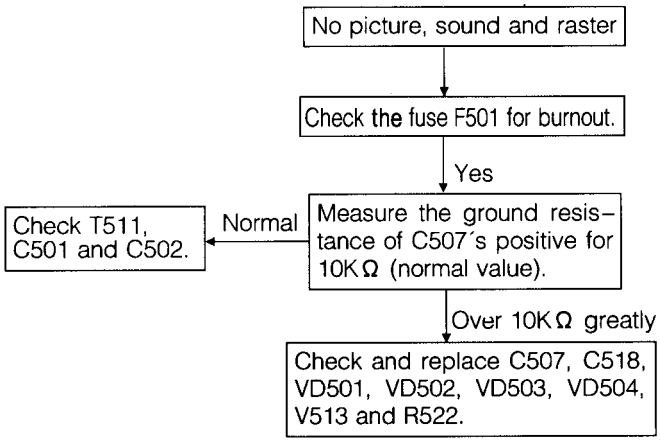
Position	Pin No.	Digital Multimeter
		Operating Voltage (V)
U1 (MT1336E)	7	RF signal 0.9-1.5V_{P-P}
	2,5,14,64,67,69,109,114,120	5
U3 (MT1369AE)	16,41,70,82,111,121,141,169	2．5
	11,34,53,64,92,102,131,151, 156, 178,185,186,202	3．3
U7 (8M FLASH)	12	0
	14	Non-cyclical pulse
U21 (BA5954)	8	10．6
	9,21	5
	11,12,13,14,15,16,17,18	2．5

TROUBLESHOOTING FLOW CHARTS

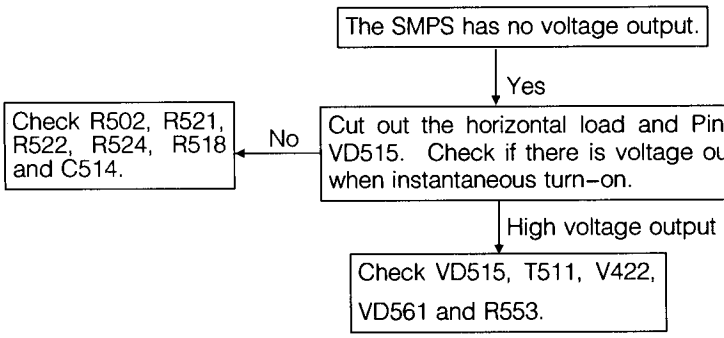
TROUBLESHOOTING FLOW CHARTS FOR TV UNIT

1. Switch Mode Power Supply

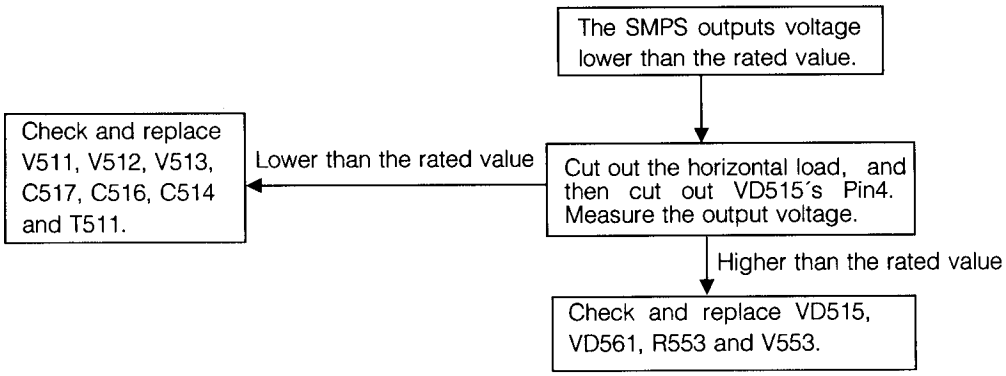
1.1 No picture, sound and raster



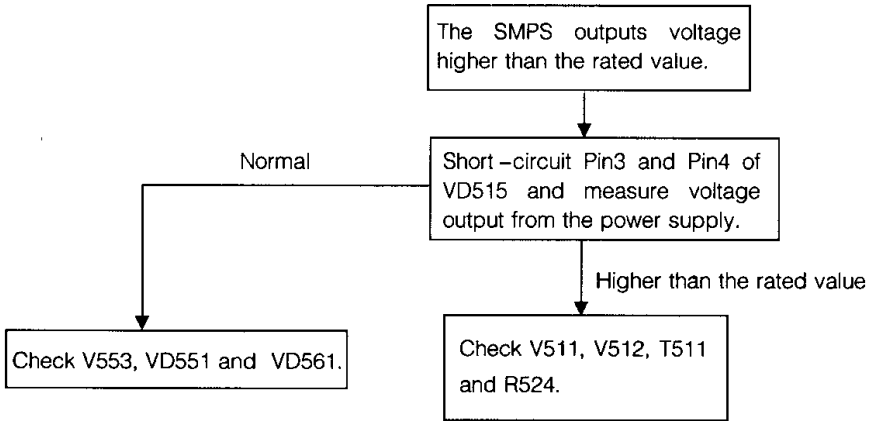
1.2 The SMPS has no voltage output.



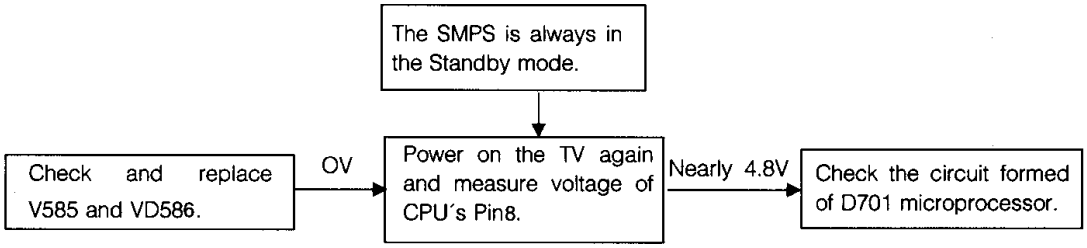
1.3 The SMPS outputs voltage lower than the rated value.



1.4 The SMPS outputs voltage higher than the rated value.

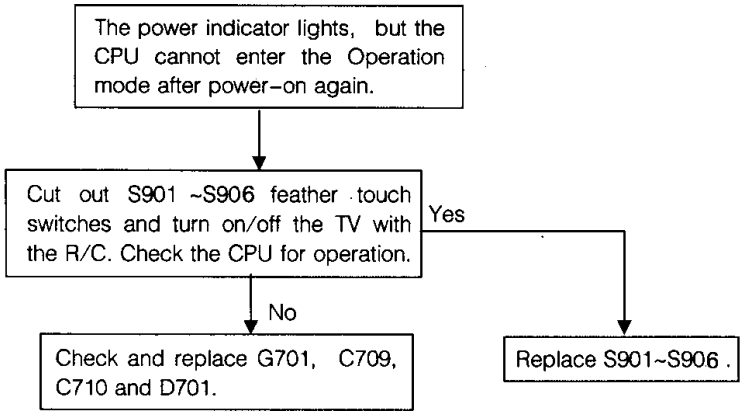


1.5 The power indicator lights, but the SMPS is still in the Standby mode.

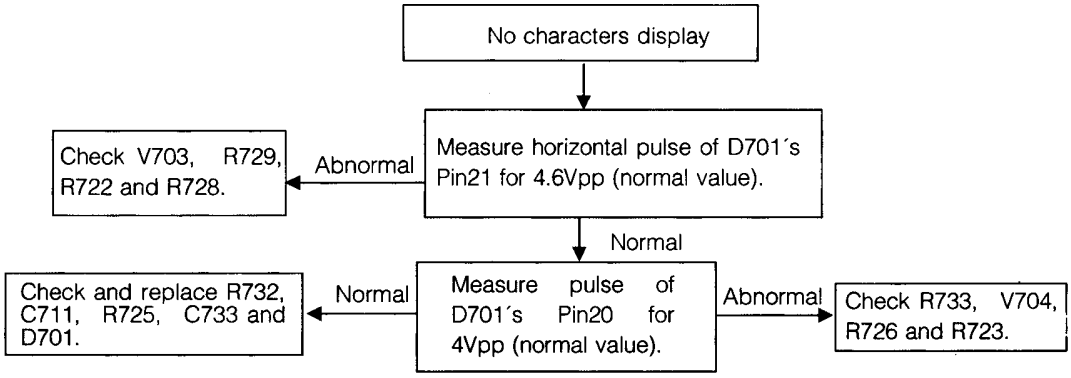


2. Control System

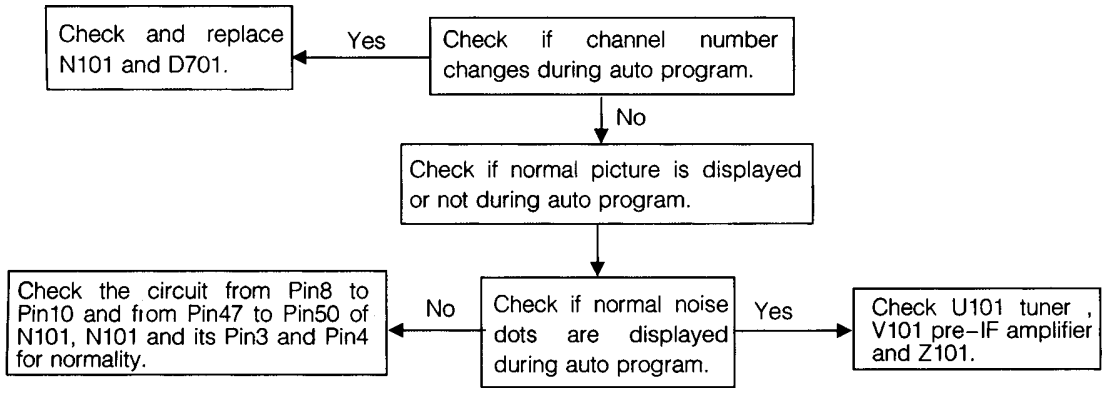
2.1 The power indicator lights, but the CPU cannot enter the Operation mode after power-on again.



2.2 No characters display

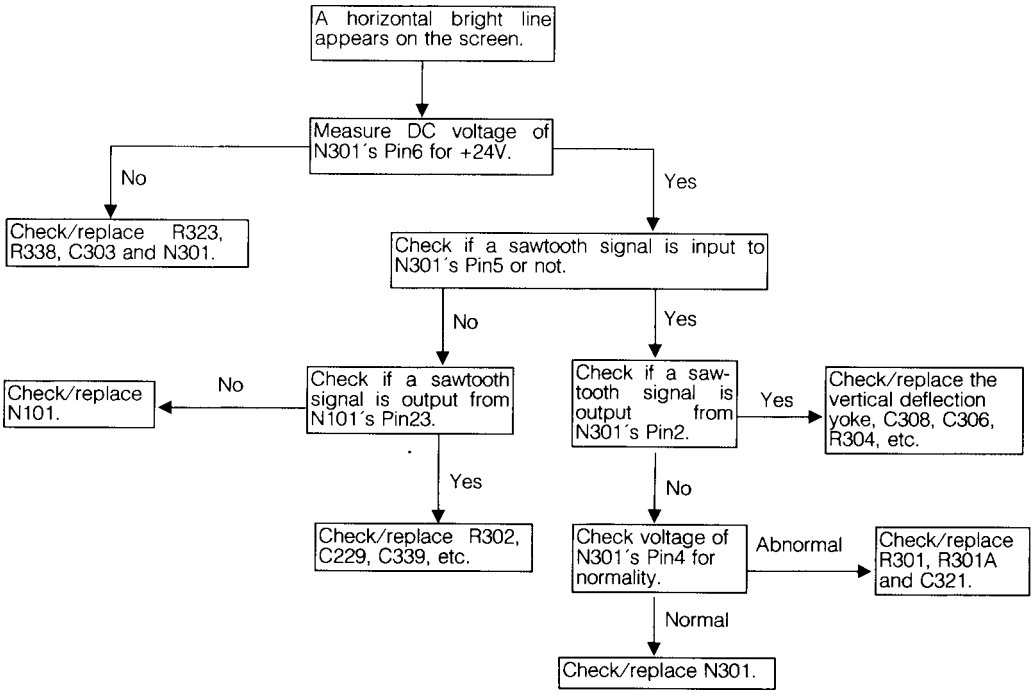


2.3 Channel number remains unchanged during auto program.

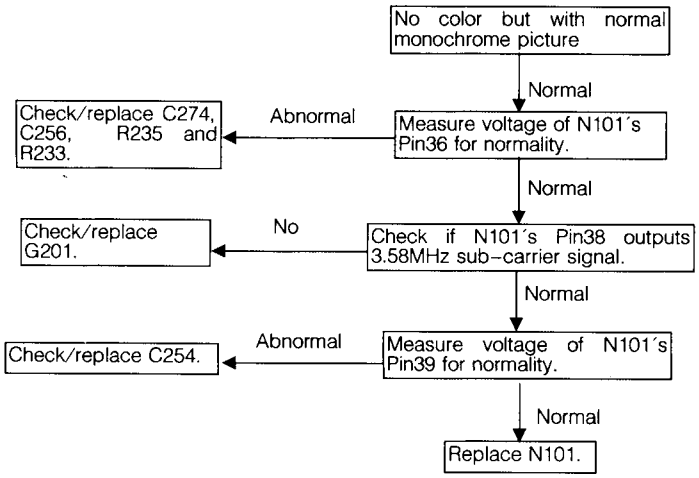


3. Video Signal Processor

3.1 A horizontal bright line appears on the screen.

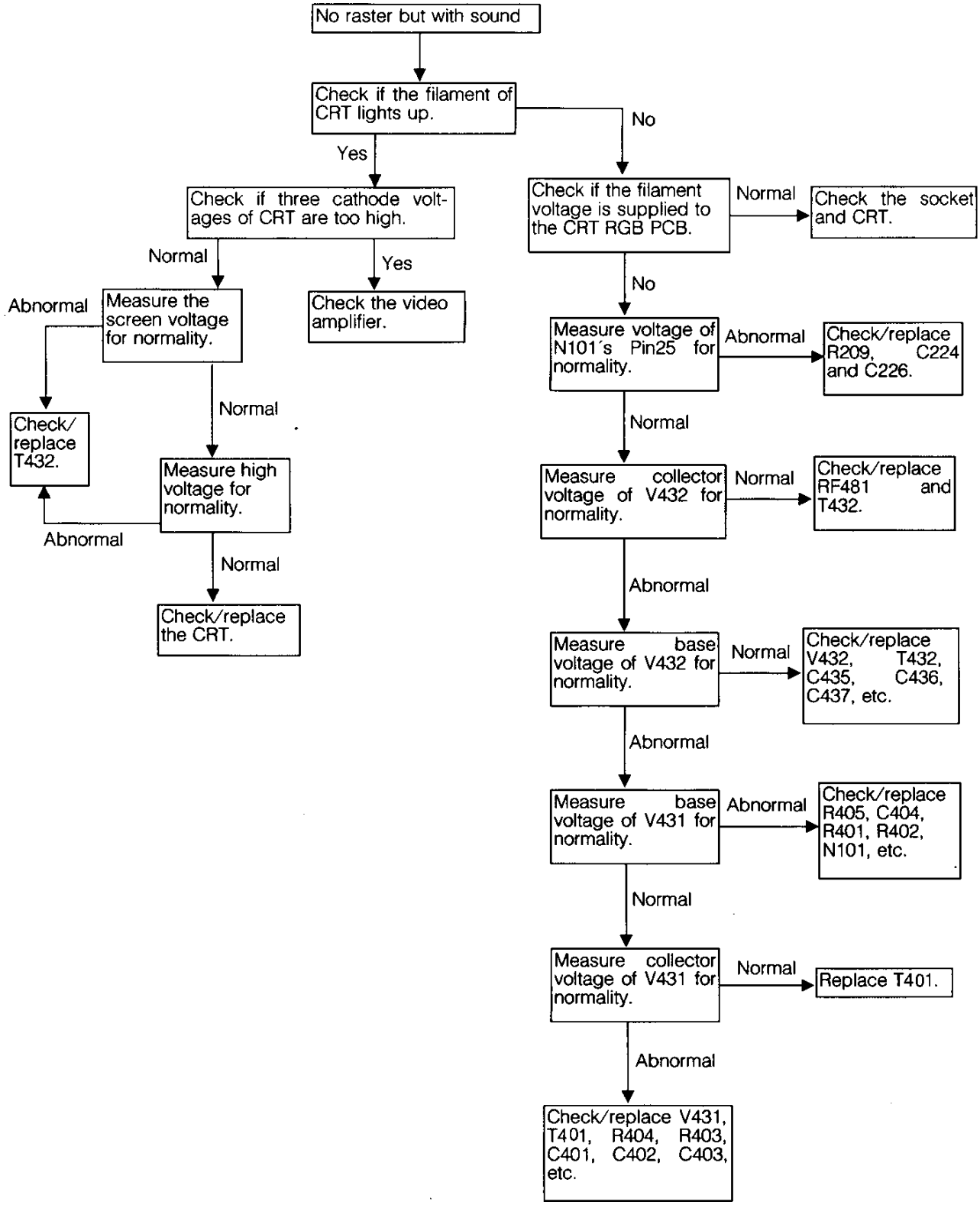


3.2 No color but with normal monochrome picture

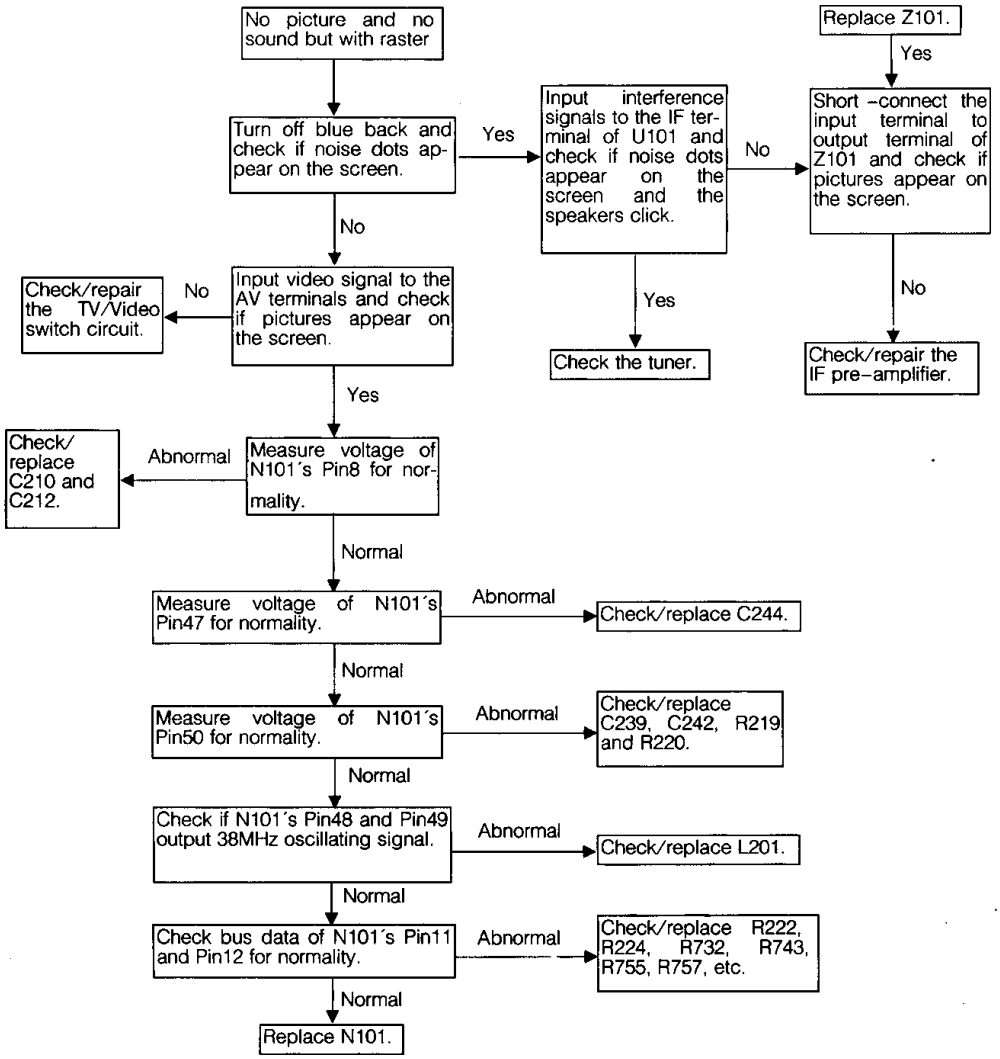


4. Horizontal/Vertical Scan Circuit

4.1 No raster but with sound

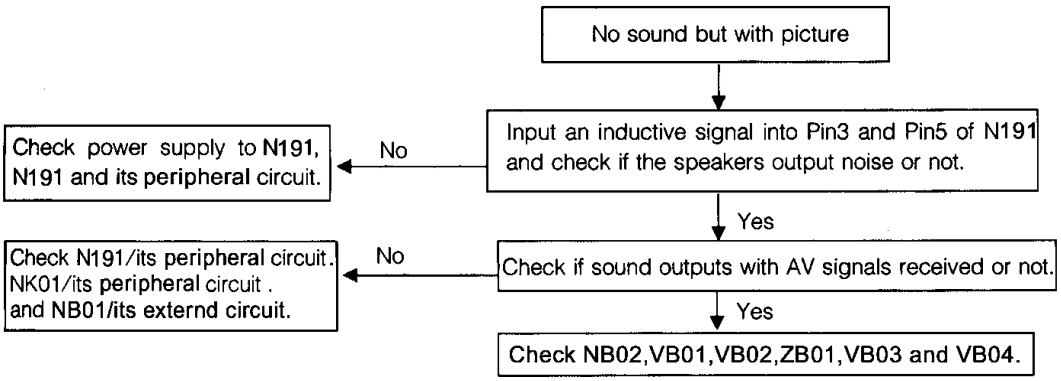


4.2 No picture and no sound but with raster

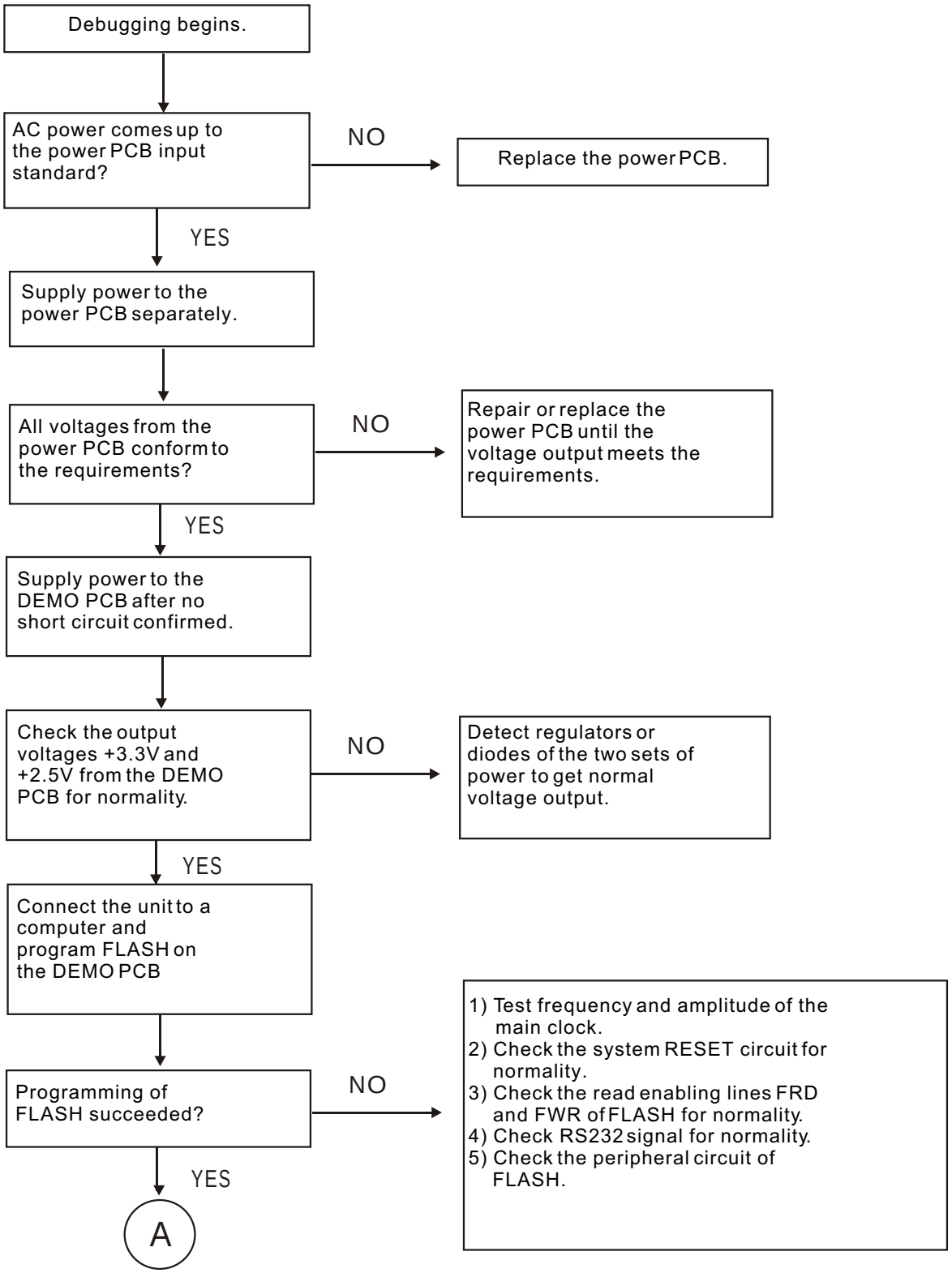


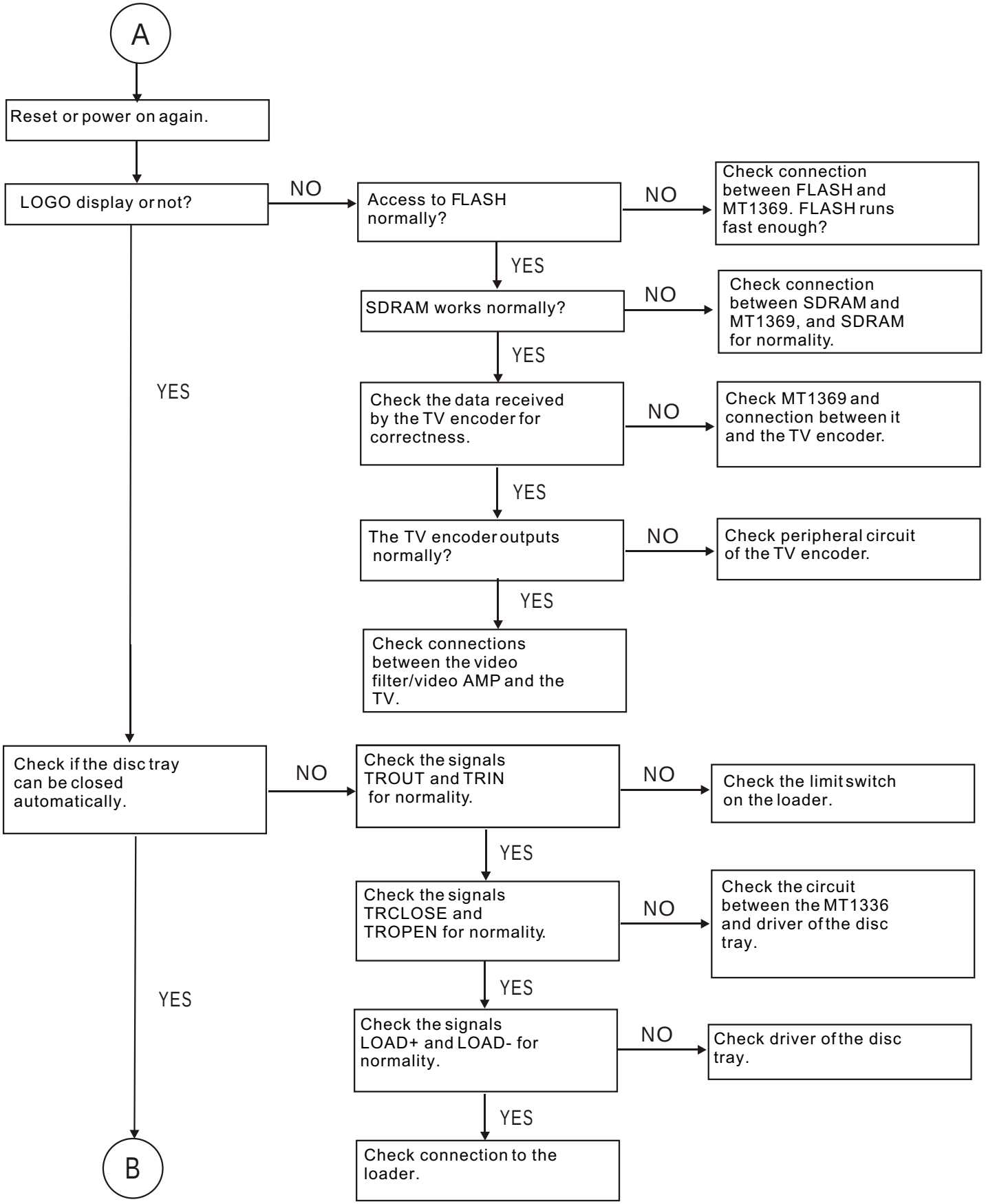
5. Audio System

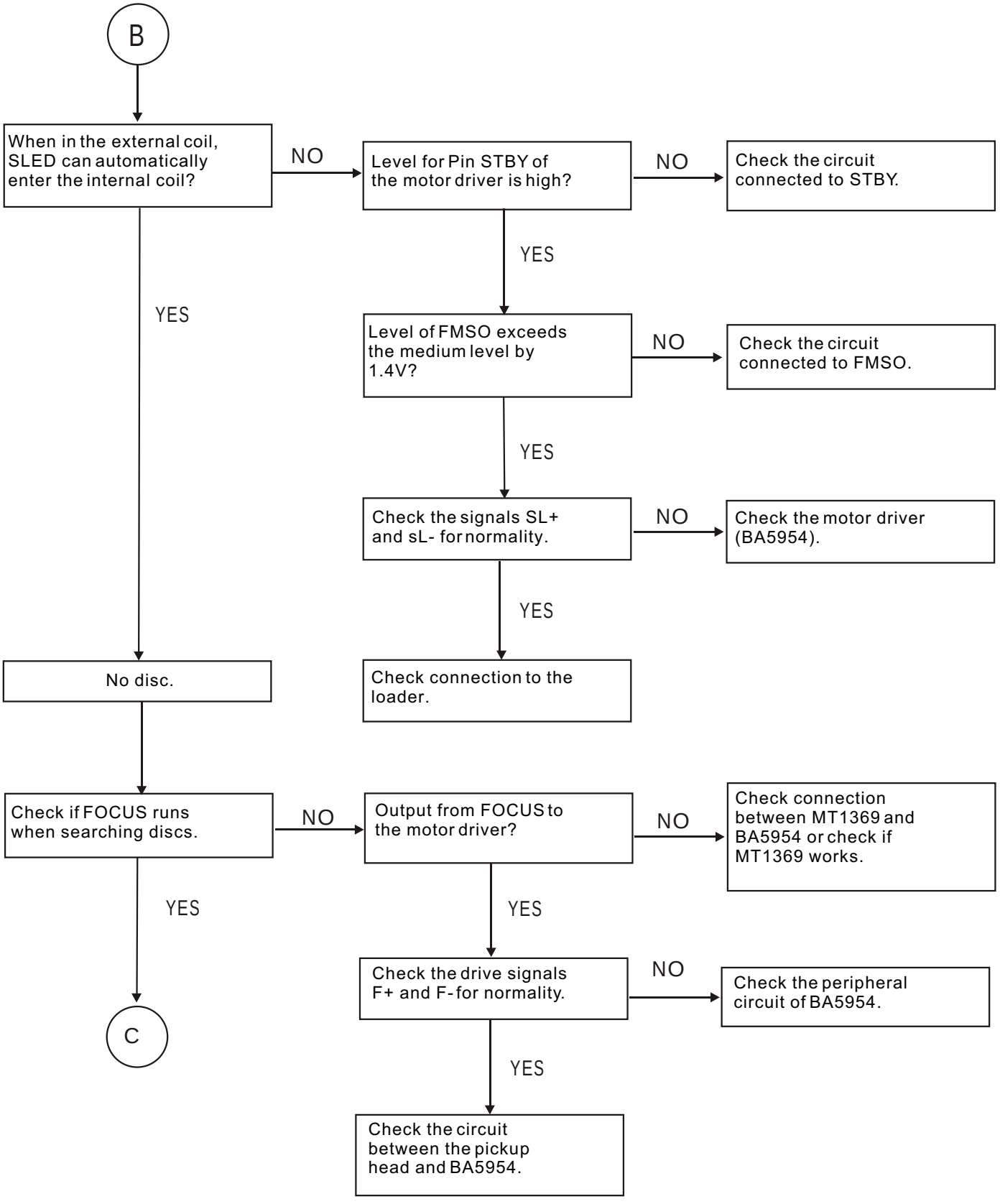
No sound

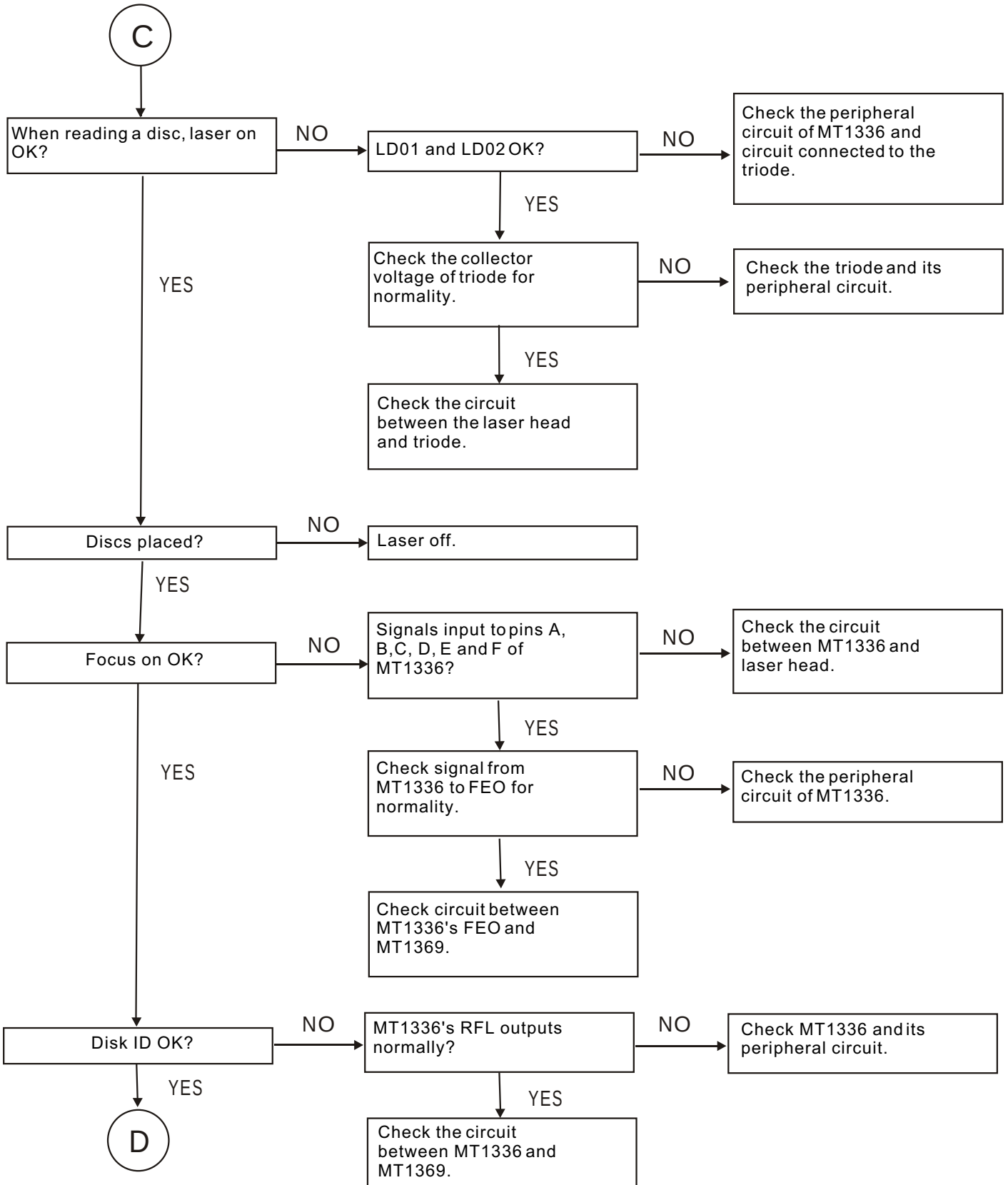


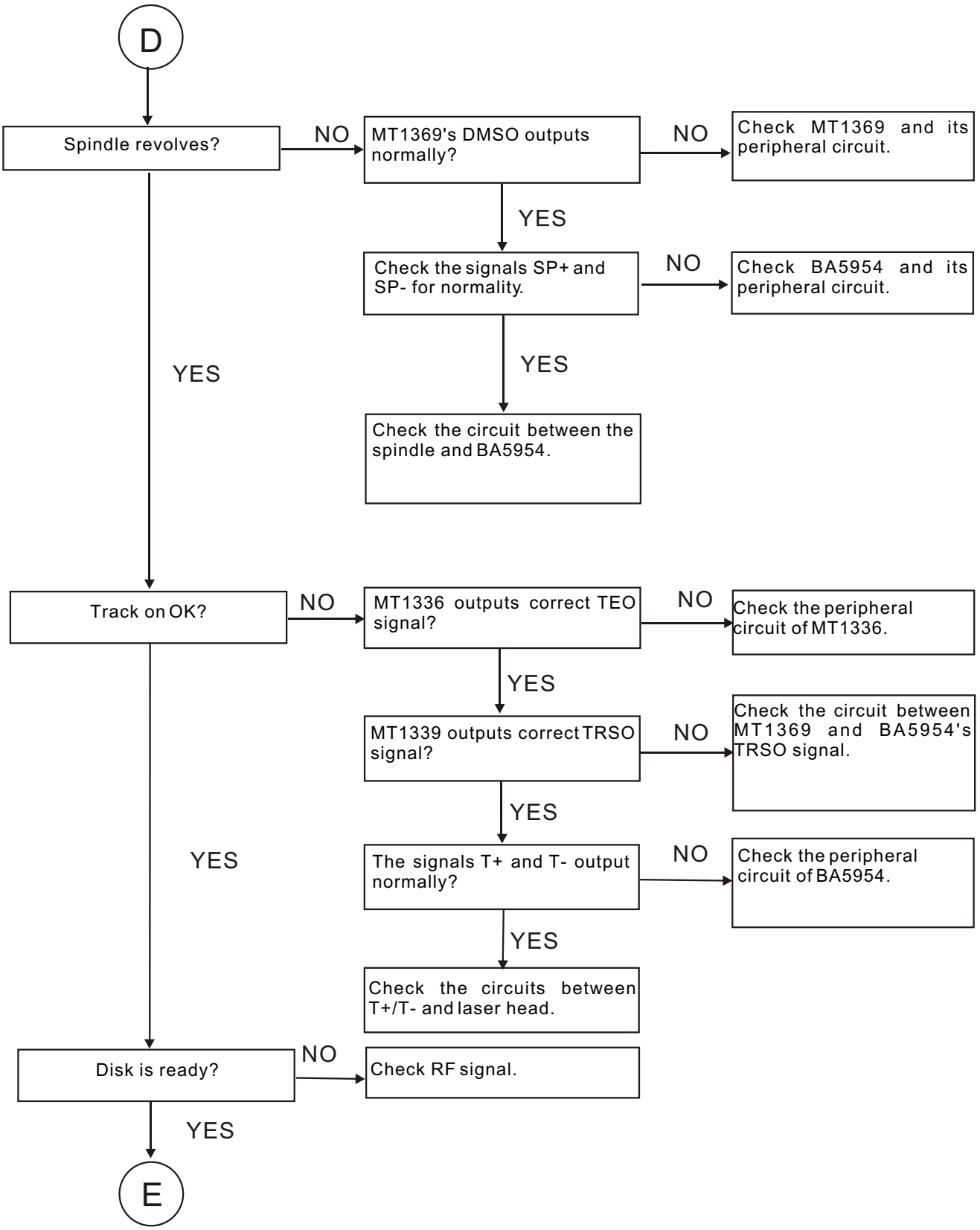
TROUBLESHOOTING FLOW CHARTS FOR DVD UNIT

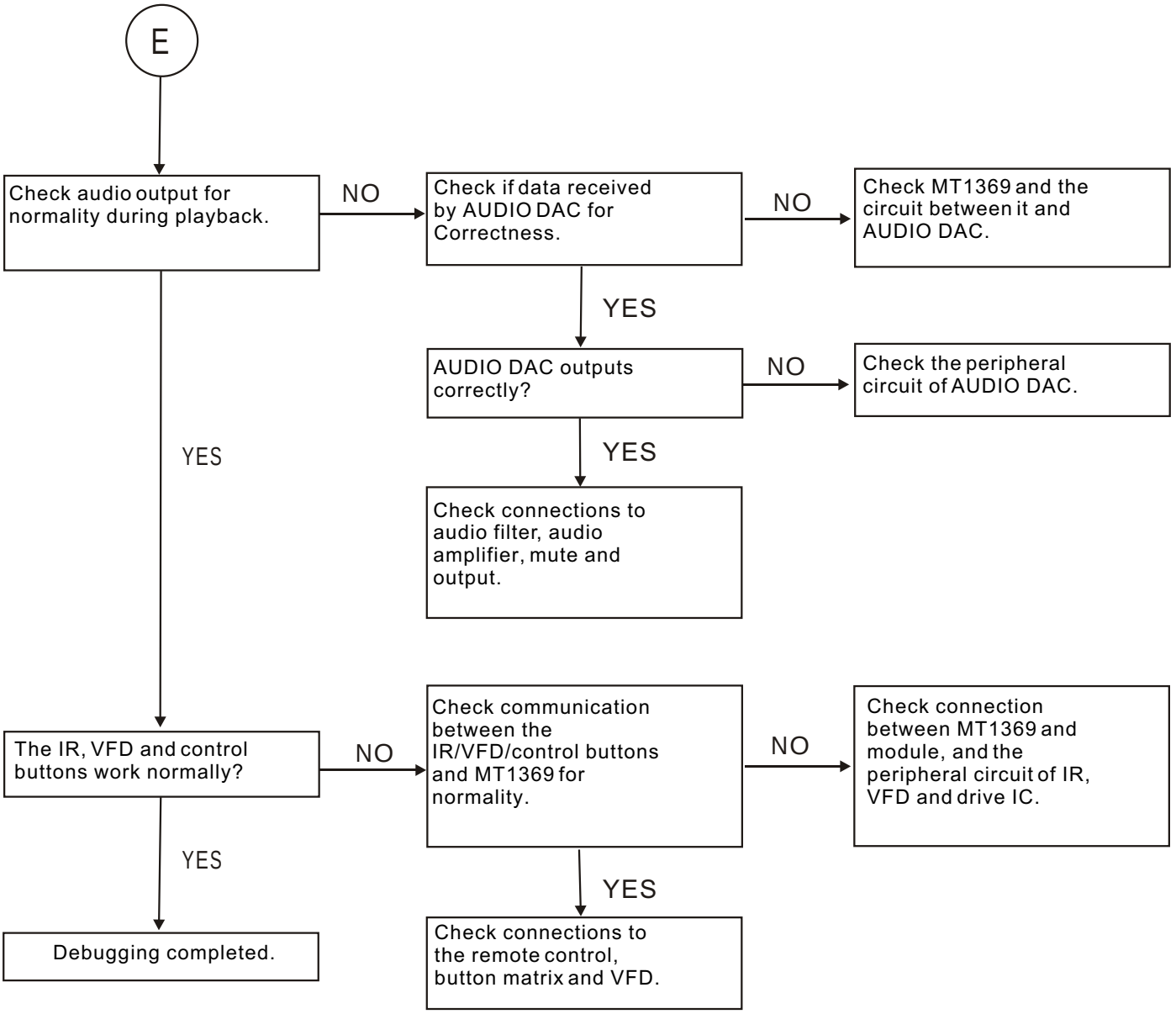



A
Reset or power on again.
LOGO display or not?
NO
Access to FLASH normally?
NO
Check connection between FLASH and MT1369. FLASH runs fast enough?
YES
SDRAM works normally?
NO
Check connection between SDRAM and MT1369, and SDRAM for normality.
YES
YES
Check the data received by the TV encoder for correctness.
NO
Check MT1369 and connection between it and the TV encoder.
YES
The TV encoder outputs normally?
NO
Check peripheral circuit of the TV encoder.
YES
Check connections between the video filter/video AMP and the TV.
Check if the disc tray can be closed automatically.
NO
Check the signals TROUT and TRIN for normality.
NO
Check the limit switch on the loader.
YES
Check the signals TRCLOSE and TROPEN for normality.
NO
Check the circuit between the MT1336 and driver of the disc tray.
YES
YES
Check the signals LOAD+ and LOAD- for normality.
NO
Check driver of the disc tray.
YES
B
Check connection to the loader.

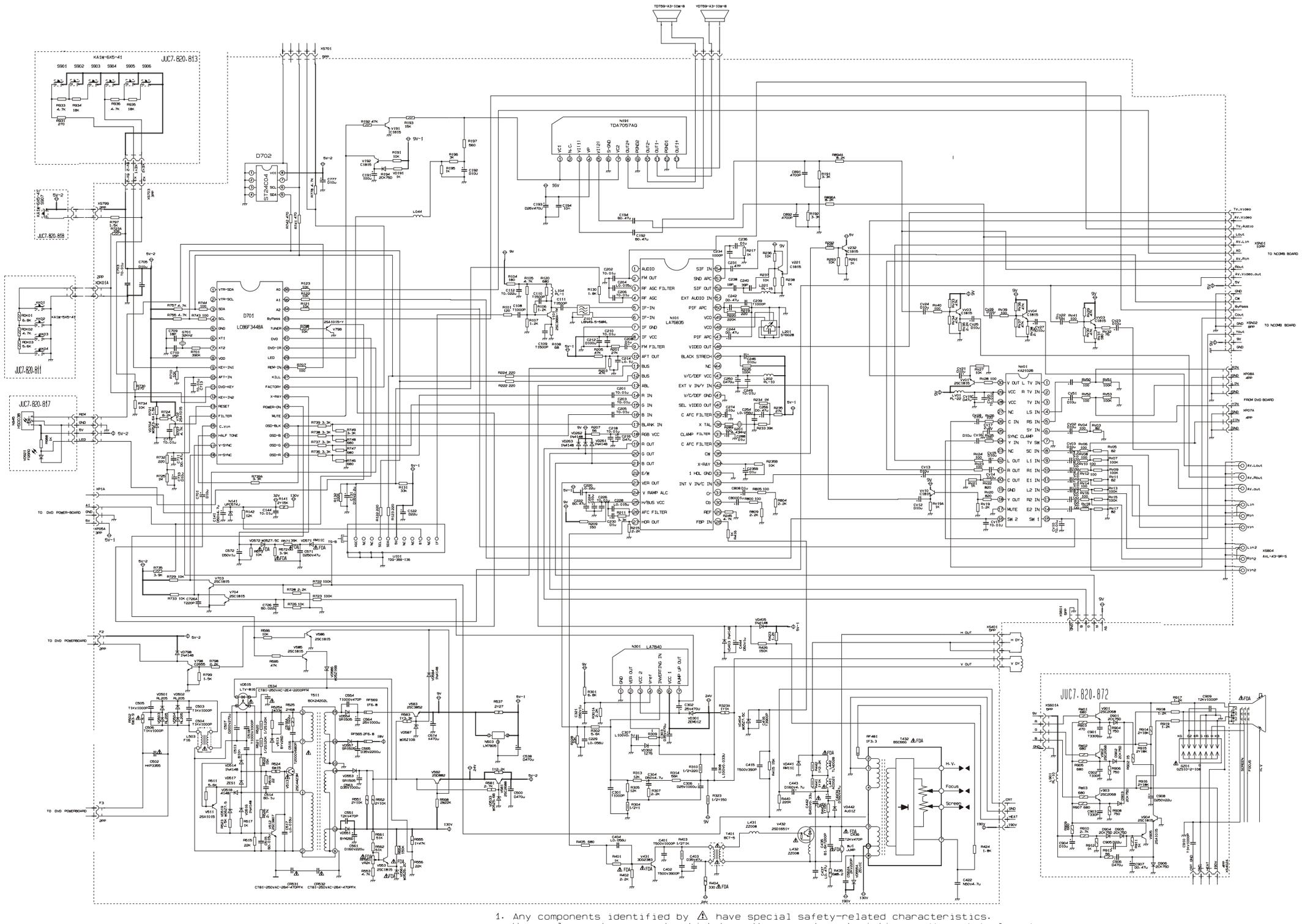

B
When in the external coil, SLED can automatically enter the internal coil?
NO
Level for Pin STBY of the motor driver is high?
NO
Check the circuit connected to STBY.
YES
YES
Level of FMSO exceeds the medium level by 1.4V?
NO
Check the circuit connected to FMSO.
YES
Check the signals SL+ and sL- for normality.
NO
Check the motor driver (BA5954).
YES
No disc.
Check connection to the loader.
Check if FOCUS runs when searching discs.
NO
Output from FOCUS to the motor driver?
NO
Check connection between MT1369 and BA5954 or check if MT1369 works.
YES
YES
Check the drive signals F+ and F- for normality.
NO
Check the peripheral circuit of BA5954.
C
YES
Check the circuit between the pickup head and BA5954.


C
When reading a disc, laser on OK?
NO
LD01 and LD02 OK?
NO
Check the peripheral circuit of MT1336 and circuit connected to the triode.
YES
YES
Check the collector voltage of triode for normality.
NO
Check the triode and its peripheral circuit.
YES
Check the circuit between the laser head and triode.
Discs placed?
NO
Laser off.
YES
Focus on OK?
NO
Signals input to pins A, B,C, D, E and F of MT1336?
NO
Check the circuit between MT1336 and laser head.
YES
YES
Check signal from MT1336 to FEO for normality.
NO
Check the peripheral circuit of MT1336.
YES
Check circuit between MT1336's FEO and MT1369.
Disk ID OK?
NO
MT1336's RFL outputs normally?
NO
Check MT1336 and its peripheral circuit.
YES
YES
D
Check the circuit between MT1336 and MT1369.


D
Spindle revolves?
NO
MT1369's DMSO outputs normally?
NO
Check MT1369 and its peripheral circuit.
YES
Check the signals SP+ and SP- for normality.
NO
Check BA5954 and its peripheral circuit.
YES
YES
Check the circuit between the spindle and BA5954.
Track on OK?
NO
MT1336 outputs correct TEO signal?
NO
Check the peripheral circuit of MT1336.
YES
MT1339 outputs correct TRSO signal?
NO
Check the circuit between MT1369 and BA5954's TRSO signal.
YES
YES
The signals T+ and T- output normally?
NO
Check the peripheral circuit of BA5954.
YES
Check the circuits between T+/T- and laser head.
Disk is ready?
NO
Check RF signal.
YES
E


E
Check audio output for normality during playback.
NO
Check if data received by AUDIO DAC for Correctness.
NO
Check MT1369 and the circuit between it and AUDIO DAC.
YES
AUDIO DAC outputs correctly?
NO
Check the peripheral circuit of AUDIO DAC.
YES
YES
Check connections to audio filter, audio amplifier, mute and output.
The IR, VFD and control buttons work normally?
NO
Check communication between the IR/VFD/control buttons and MT1369 for normality.
NO
Check connection between MT1369 and module, and the peripheral circuit of IR, VFD and drive IC.
YES
YES
Debugging completed.
Check connections to the remote control, button matrix and VFD.

Circuit Diagram

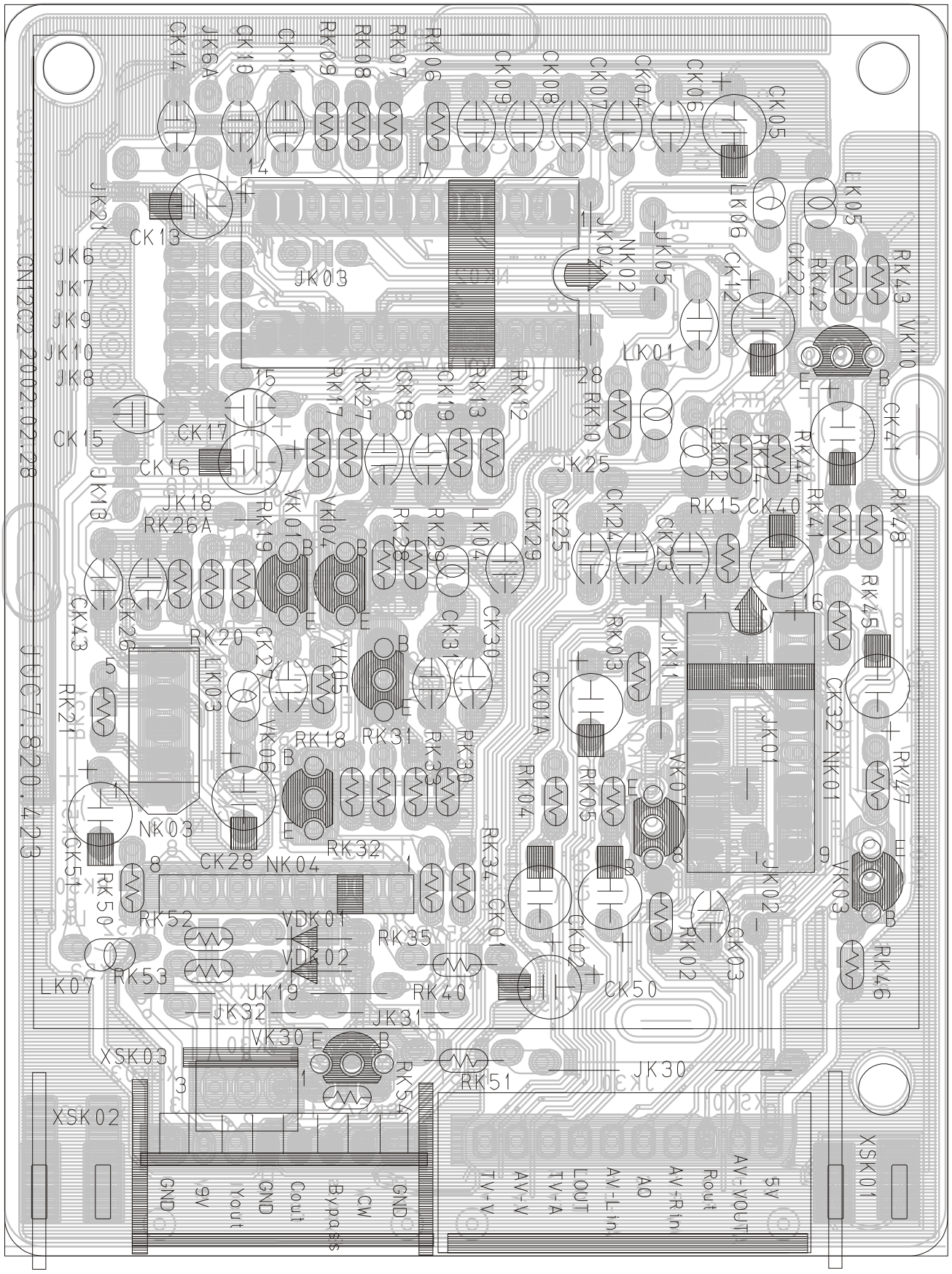


1. Any components identified by ⚠ have special safety-related characteristics.
   Use replacement components which have the same characteristics as the original parts.

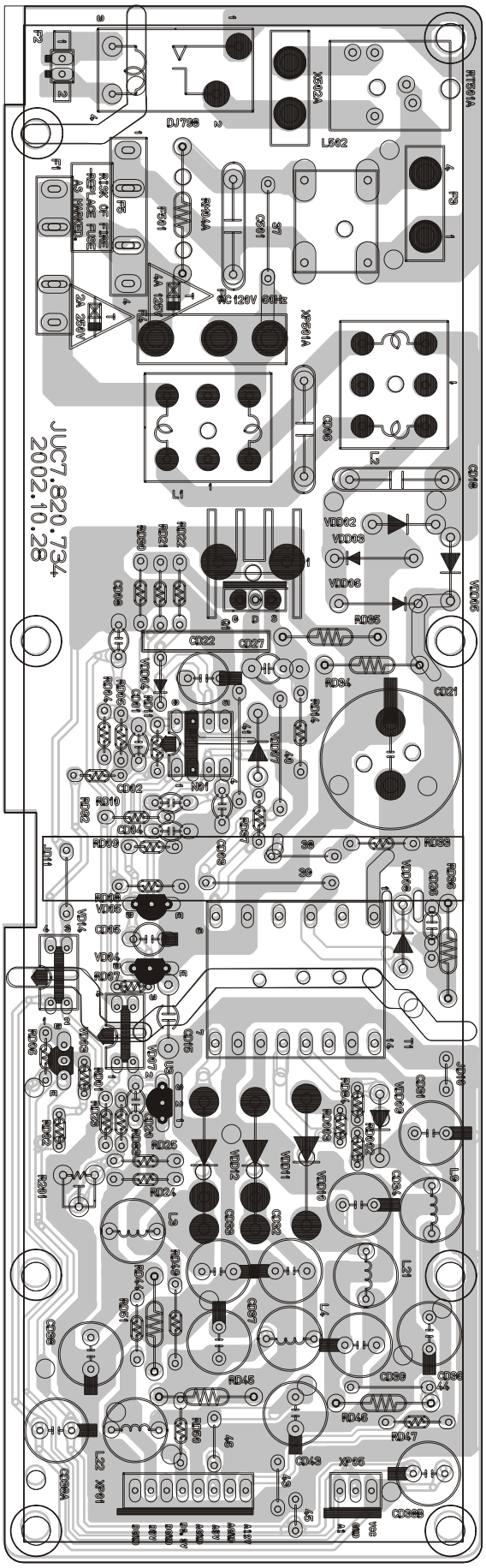
2. ⚠ FDA This symbol tells you that replacement components related to high voltage.
   beam current and X_ray radiation should not be made at will.

This circuit diagram is only for reference.
Specifications are subject to change without notice.

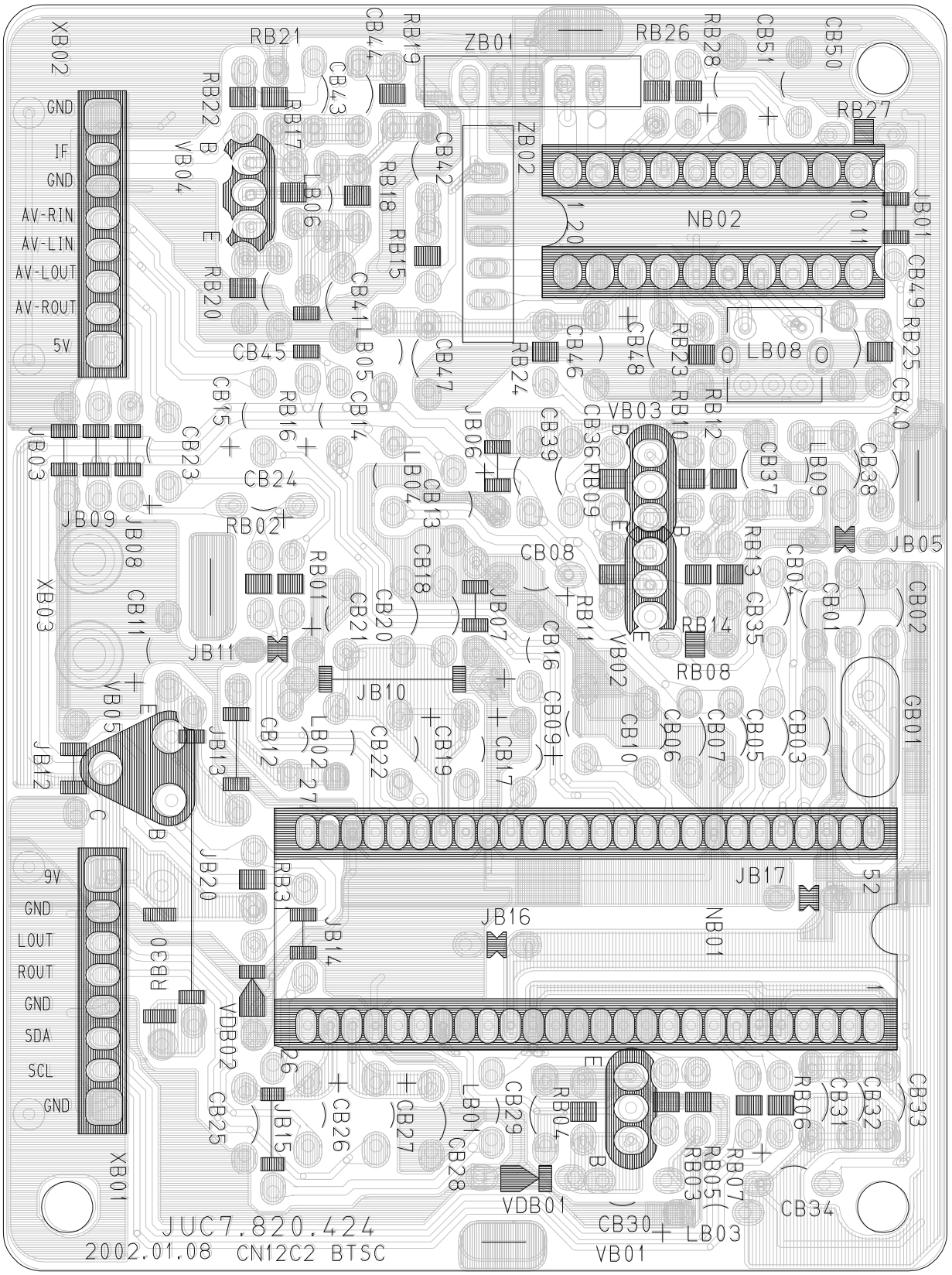
N-COMB PCB ASSEMBLY



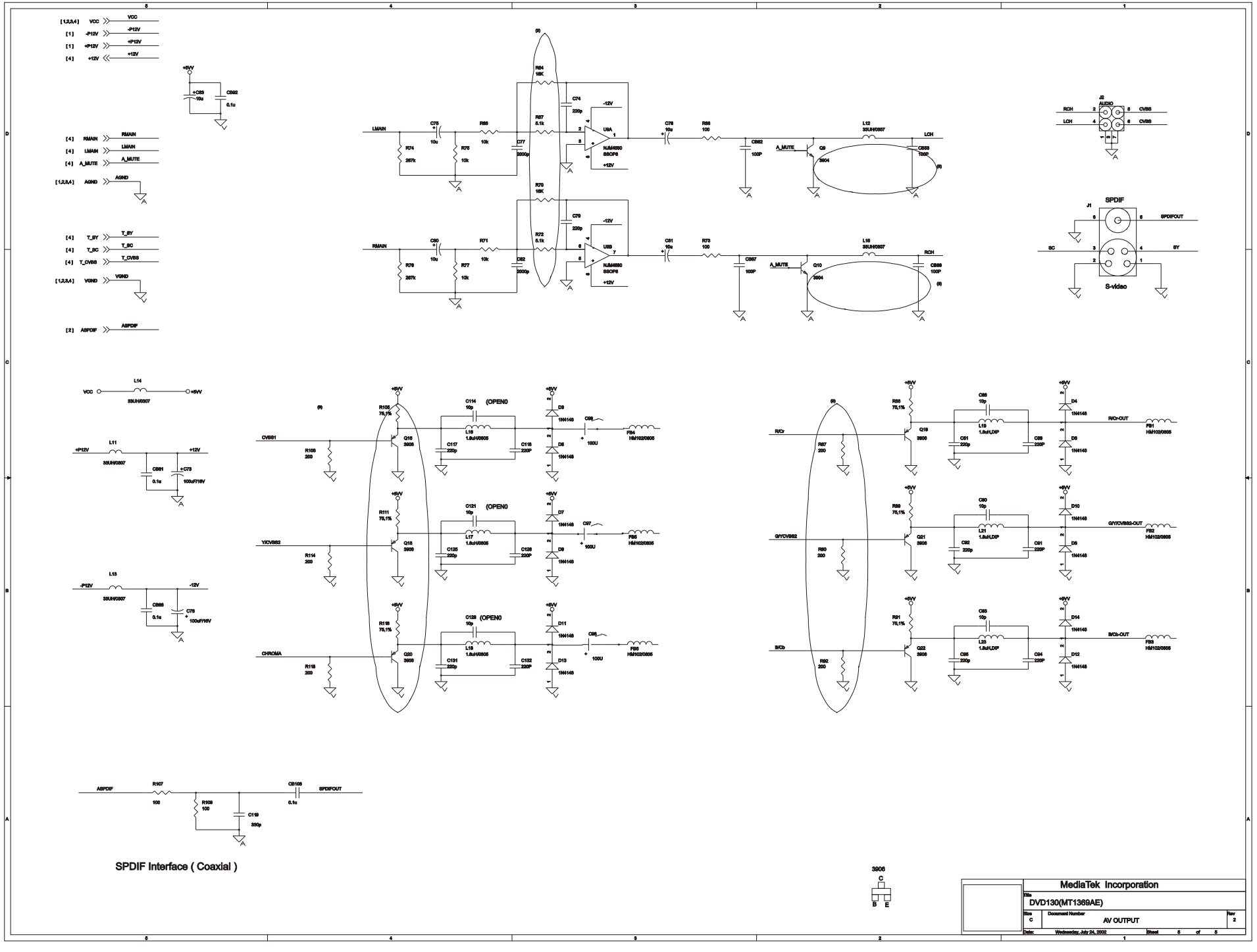
DVD Power PCB



BTSC PCB


XB02
GND
IF
GND
AV-RIN
AV-LIN
AV-LOUT
AV-ROUT
5V
XB03
9V
GND
LOUT
ROUT
GND
SDA
SCL
GND
XB01
ZB01
ZB02
NB02
NB01
JUC7.820.424
2002.01.08 CN12C2 BTSC

Circuit Diagram for DVD130A (1)



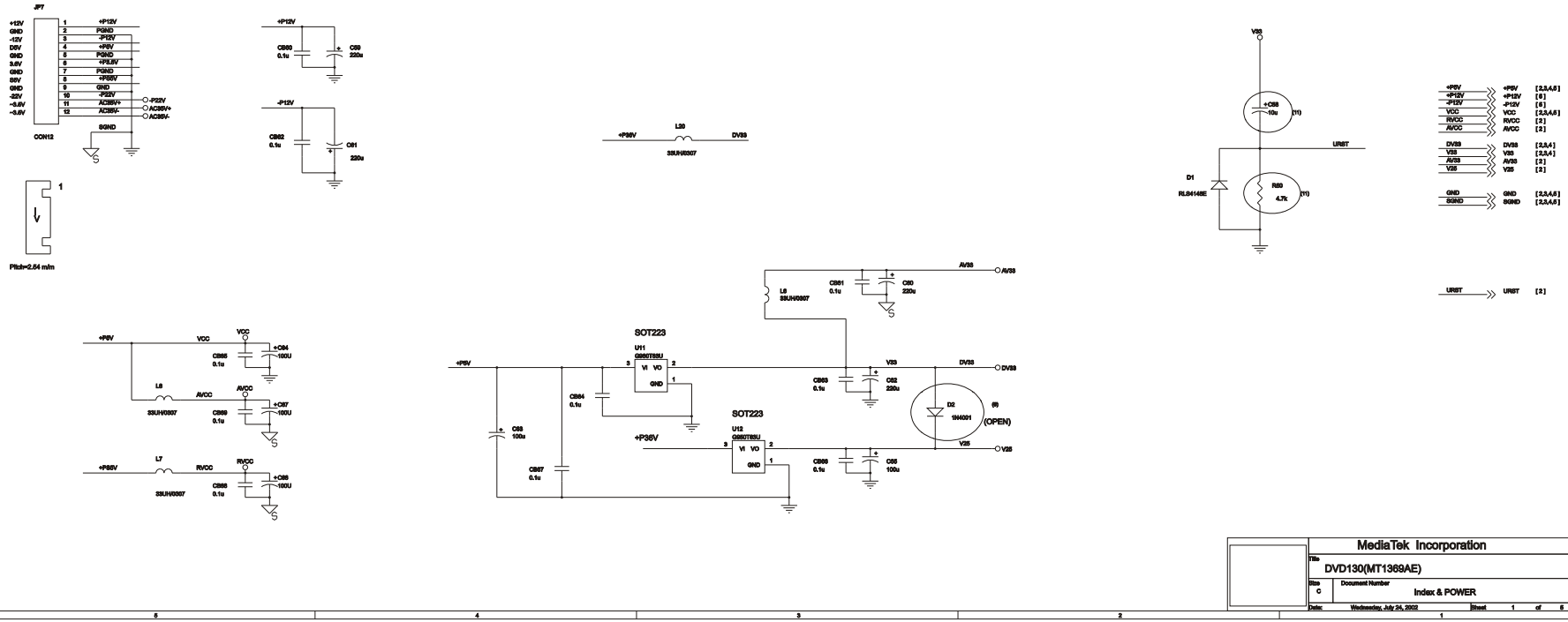
3-SY3689P2-V2

MT1369E (LQFP208) DVD MP Board for Sanyo SF-HD6AV PUH

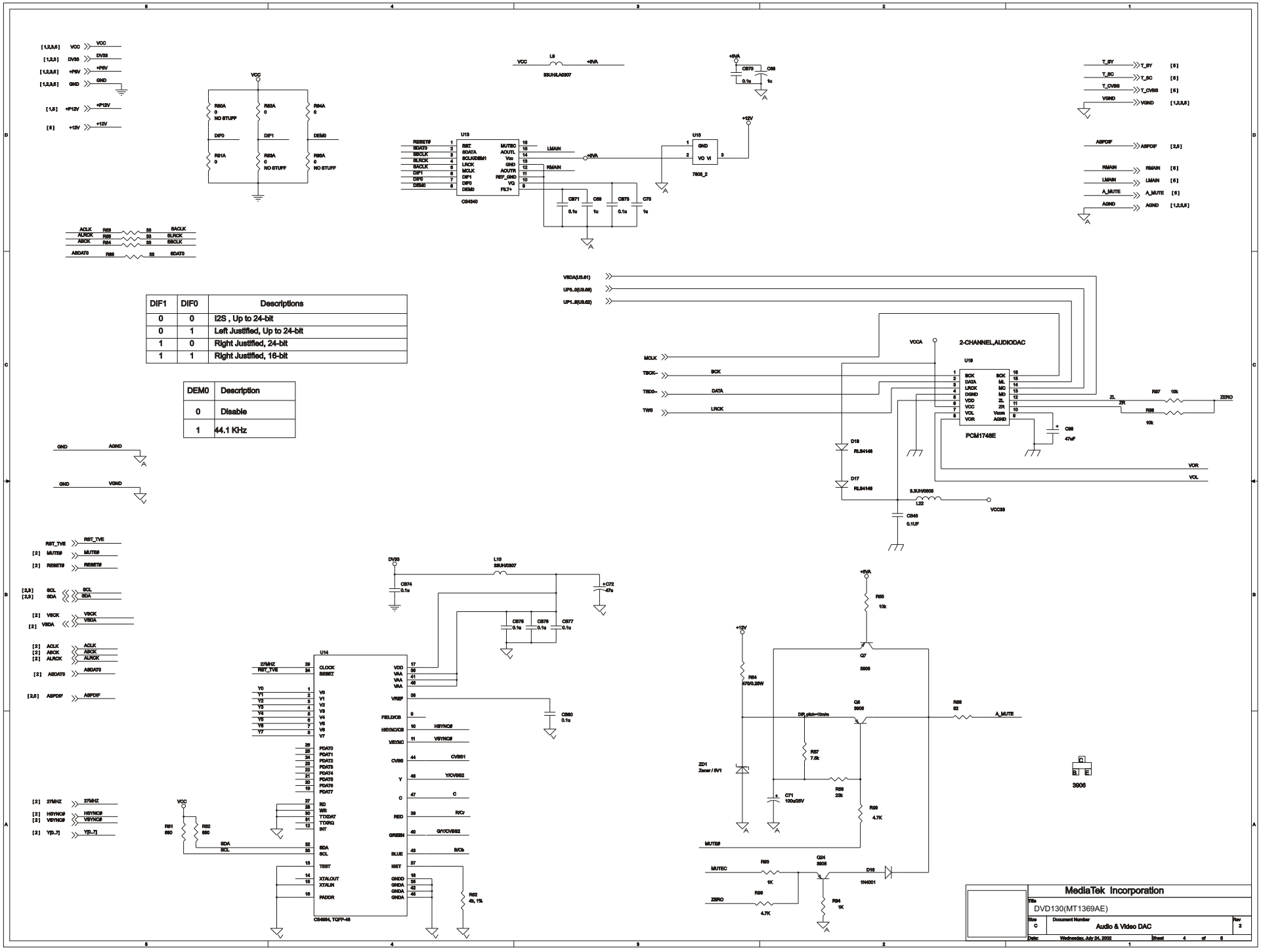
1 INDEX & POWER, RESET
2 RF / SERVO & MPEG - MT1336E / MT1369E
3 MEMORY - SDRAM, FLASH/EEPROM
4 AUDIO - CS4334, VIDEO - CS4954/55
5 AV FILTER.

NAME	TYPE	DEVICE
VCC	Digital 5V	SUPPLY
RVCC	Servo 5V	MT1336E
AVCC	RF 5V	PICKUP HEADER
V33	Digital 3.3V	SDRAM, Flash, VideoDAC
DV33	Digital 3.3V	MT1369E
AV33	Servo 3.3V	MT1369E
V25	Digital 2.5V	MT1369E
+5VA	Audio 5V	Audio DAC
+3VV	Video 3.3V	Video DAC
+5VV	Video 5V	Video DAC
+12V	Audio 12V	Audio filter

NAME	TYPE
GND	Digital Ground
SGND	Servo Analog Ground
AGND	Audio Ground
VGND	Video Ground



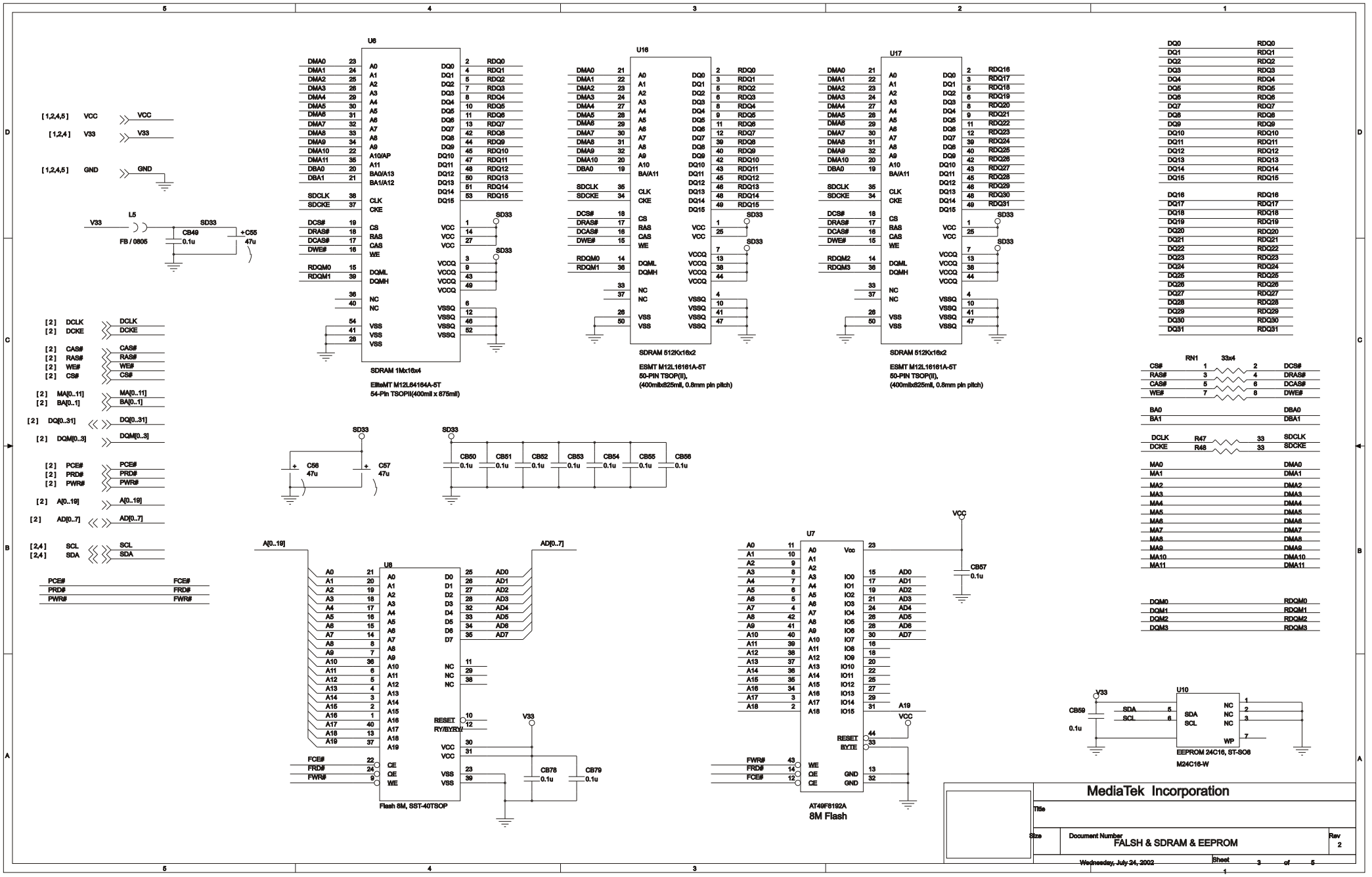
Circuit Diagram for DVD130A (3)



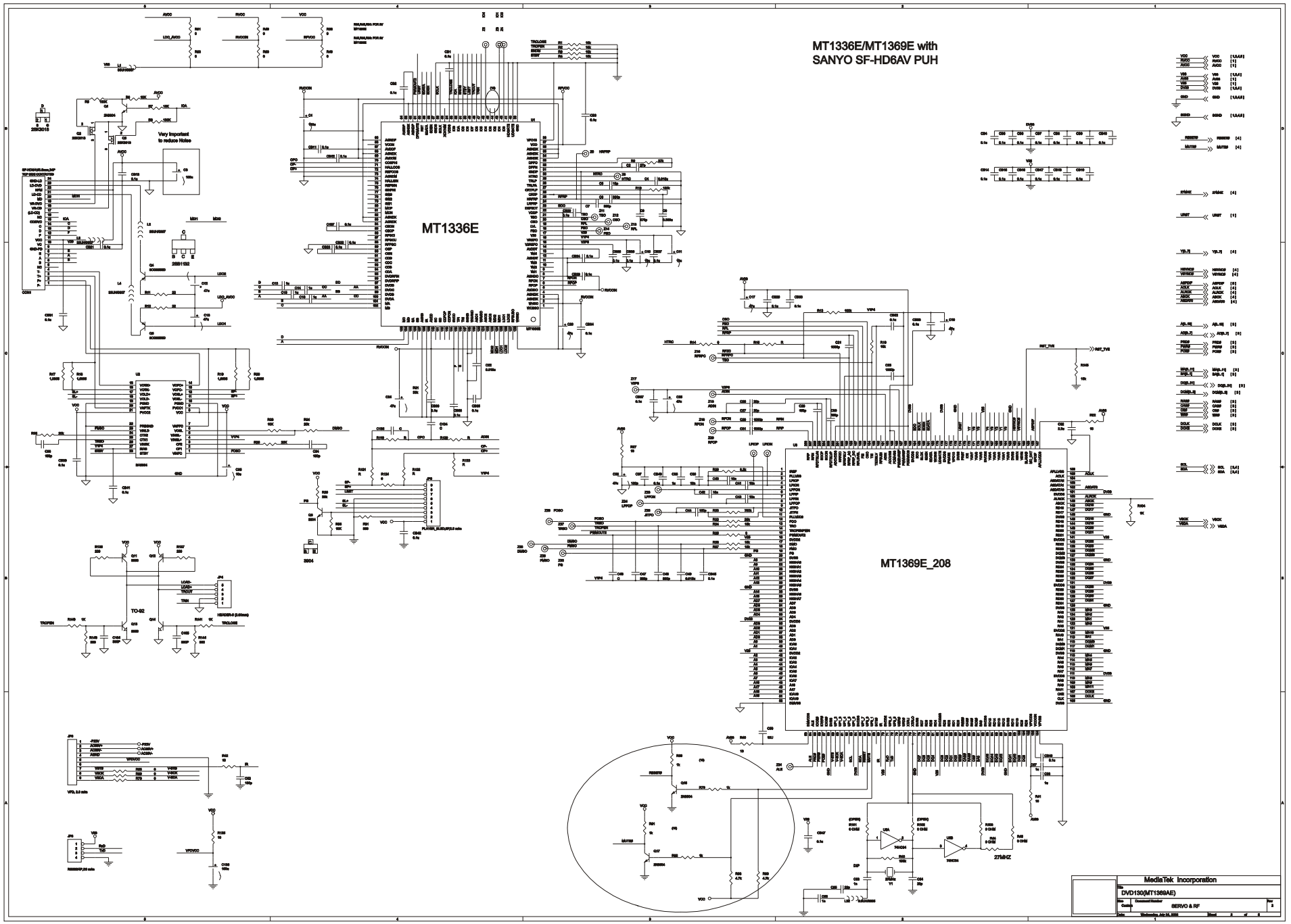
DIF1	DIF0	Descriptions
0	0	I2S , Up to 24-bit
0	1	Left Justified, Up to 24-bit
1	0	Right Justified, 24-bit
1	1	Right Justified, 16-bit

DEM0	Description
0	Disable
1	44.1 KHz

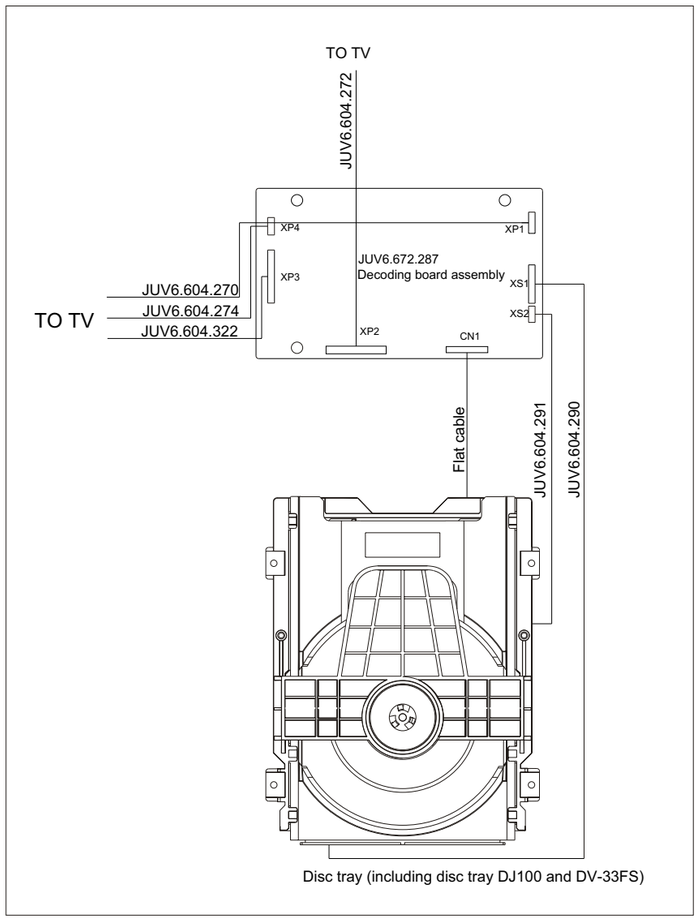
Circuit Diagram for DVD130A (4)



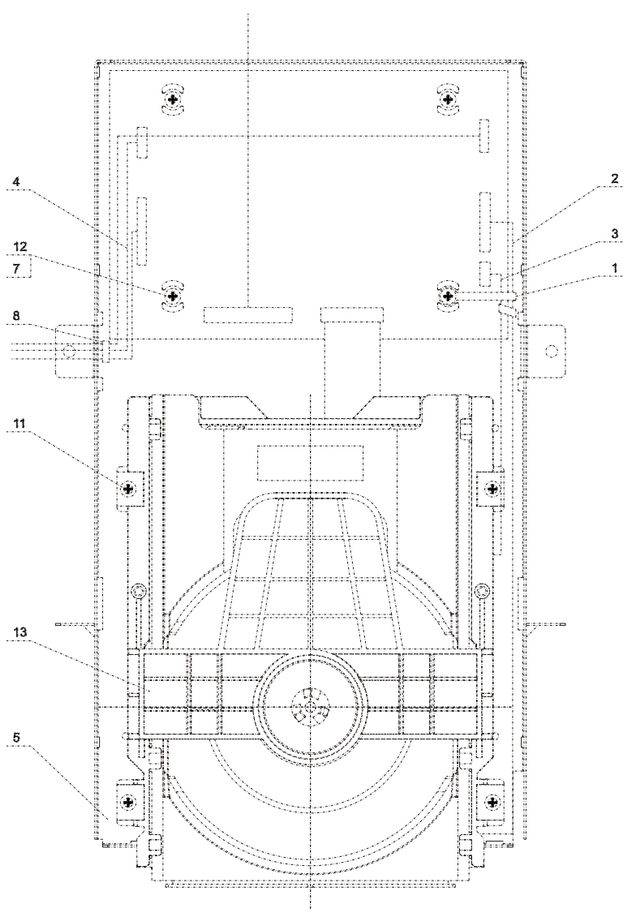
Circuit Diagram for DVD130A (5)

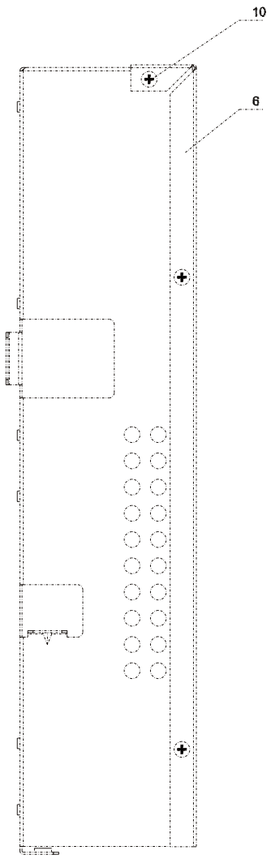


Final Wiring Diagram and Final Assembly Diagram for DVD130A



Final Wiring Diagram for DVD130A





Technical Requirements

1. During mounting, ensure static protection to the disc tray (13).
2. Stick the warning labels (9) conspicuously on the disc tray (13) and shield cover (6) respectively.
3. Fasten the flat cable between the disc tray and decoding board with the tape (14).
4. Bind wire with the wire clip (8).
5. Ensure that four fins of the shield case are not deformed during mounting.

Serial No.	Code No.	Parts	Qty	Remarks
18				
17				
16				
15				
14				
13		Disc tray (DJ100+DV-33FS)		
12		Screw 6560 M3X16	4	
11		Screw 6560 M3X8	4	
10		Tapping screw 3X8VTHO	6	
9	JUV6.817.041	Warning label	2	
8	JU8.667.310	Wire clip	1	
7	JUV8.072.015	Supporting column	4	
6	JUV7.312.004	Shield cover	1	
5	JUV7.312.003	Shield case	1	
4	JUV6.672.287	Decoding board assembly	1	
3	JUV6.604.291	Wired connector	1	
2	JUV6.604.290	Wired connector	1	
1	JUV6.463.001	Fastening clip assembly	1	

Final Assembly Diagram of DVD Unit