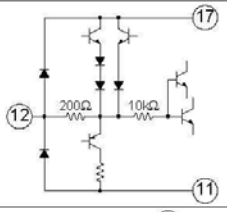
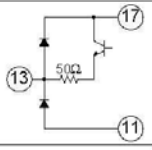
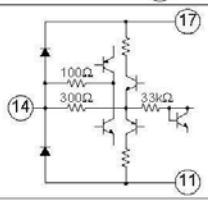
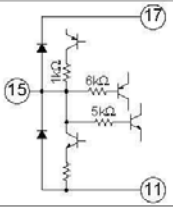
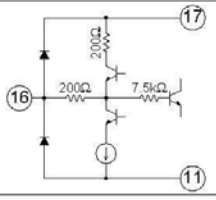
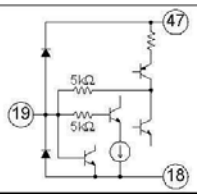
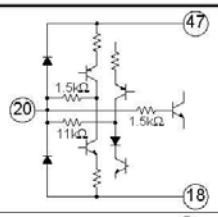
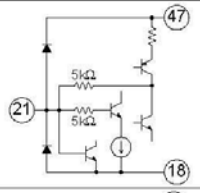
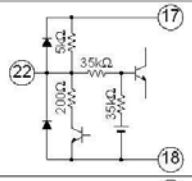
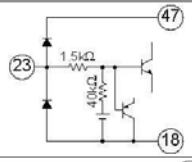
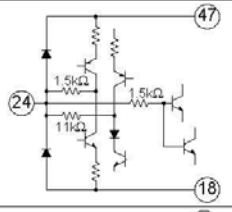
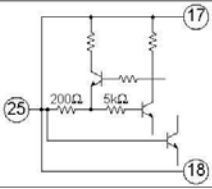
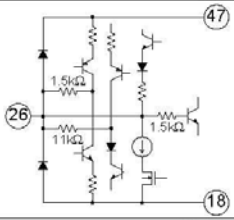
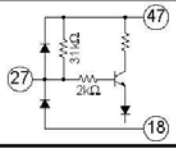
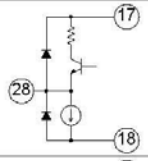
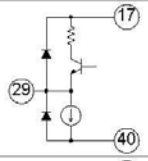
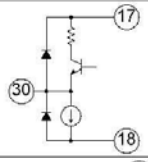
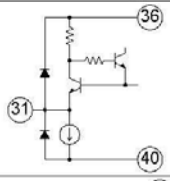
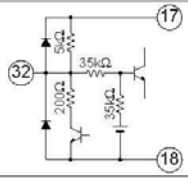
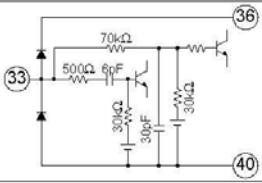
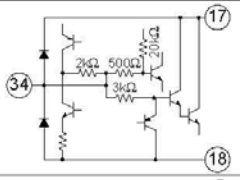
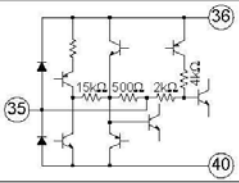
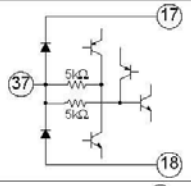
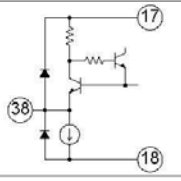
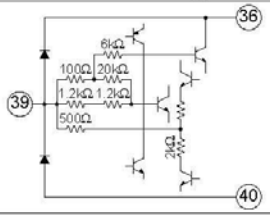
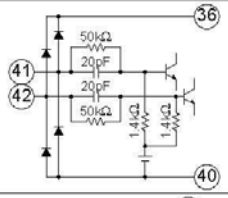
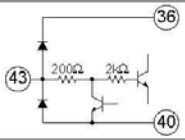
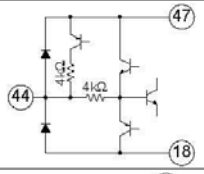
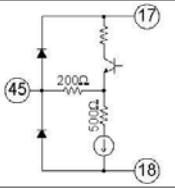
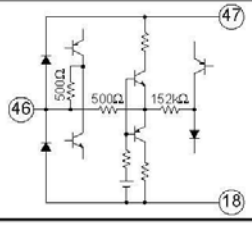
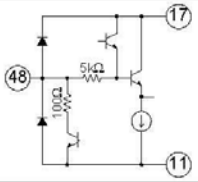
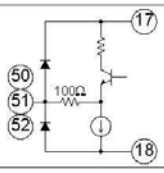
SIGNAL PROCESSOR BLOCK

Pin No.	Pin Name	Function	Interface Circuit	I/O Signal
11	TV DEF AGND	GND terminal for TV DEF block.	—	—
12	FBP in	Input terminal for FBP.		
13	H out	Output terminal for Horizontal driving pulse.		
14	HAFC 1	Terminal to be connected capacitor for H AFC filter. This terminal voltage controls H VCO frequency.		
15	V saw	Terminal to be connected capacitor to generate V saw signal. V saw amplitude is kept constant by V AGC function.		
16	V out	Output terminal for Vertical driving pulse.		
17	AVcc 8V	Vcc terminal for DEF, RGB, Audio out and PIF out circuit. Supply 8V.	—	—
18	TV A GND	GND terminal for TV block.	—	—
19	Cb in	Input terminal for Cb signal.		

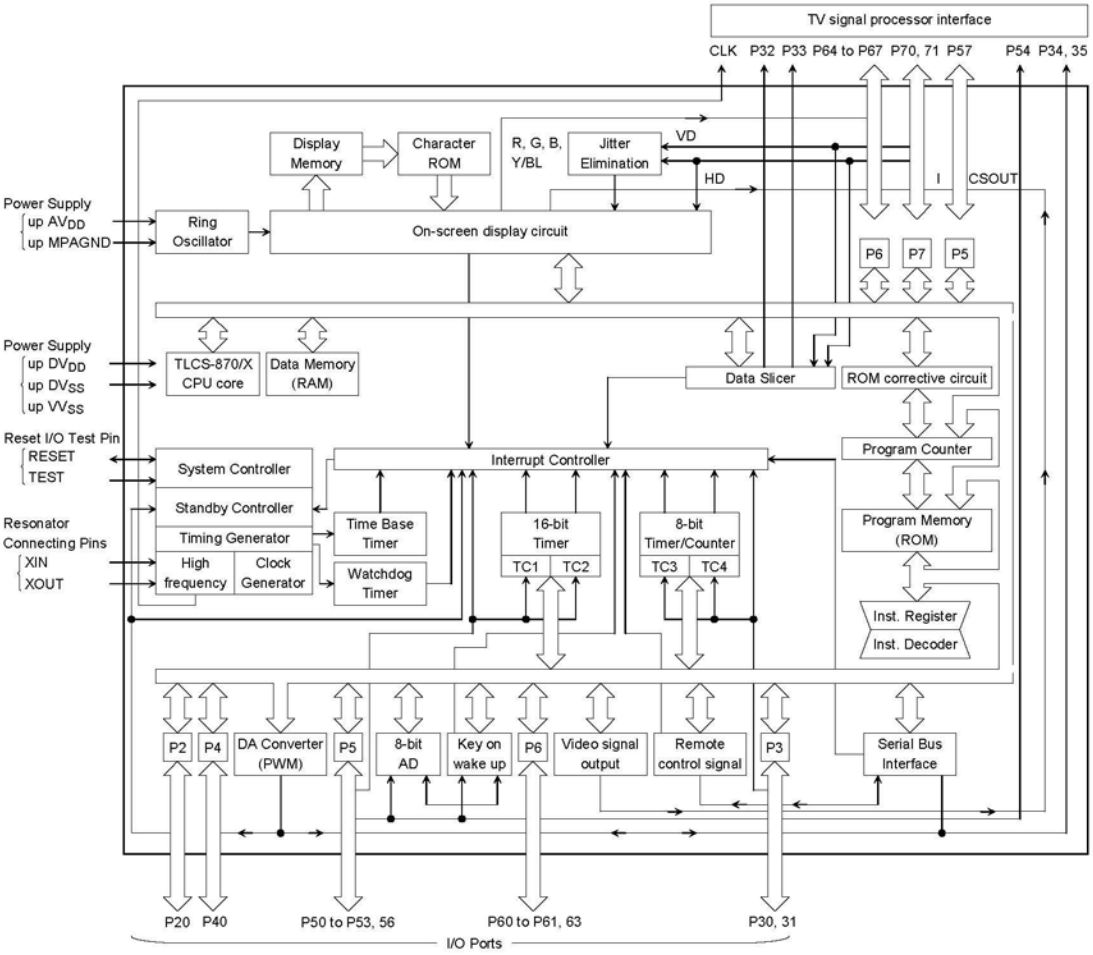
Pin No.	Pin Name	Function	Interface Circuit	I/O Signal
20	Y in	Input terminal for Y signal.		
21	Cr in	Input terminal for Cr signal.		
22	Ext Au1	Input terminal for Audio signal 1.		
23	C in	Input terminal for Chroma signal.		
24	V2 in	Input terminal for Video signal.		
25	ALC filter	Terminal to be connected capacitor for ALC (Audio Level Control).		
26	V1 in	Input terminal for Video signal. (Input level = 1 Vp-p)		
27	ABCL	Input terminal for ABL/ACL control.		

Pin No.	Pin Name	Function	Interface Circuit	I/O Signal
28	Au out 1	Output terminal 1 for Audio signal.		
29	Au out 2	Output terminal 2 for Audio signal.		
30	TV out	Output terminal for detected PIF signal.		
31	1bit DAC /SIF out	Output terminal for 1bit DAC or detected SIF signal.		
32	Ext Au2 in	Input terminal for Audio signal 1.		
33	H correc / SIF in	Input terminal for H correction and 2nd SIF.		
34	DC NF	Terminal to be connected capacitor for DC Negative Feedback from SIF Det output.		
35	PIF PLL	Terminal to be connected with loop filter for PIF PLL. This terminal voltage is controlled PIF VCO frequency.		
36	IF Vcc 5V	Vcc terminal for IF circuit. Supply 5V.		—

Pin No.	Pin Name	Function	Interface Circuit	I/O Signal
37	Reg Fil	Terminal to be connected capacitor for stabilizing internal bias.		
38	AUDIO Monitor out	Output terminal for External audio signal or TV audio signal selected by BUS (Audio SW).		
39	IF AGC	Terminal to be connected with IF AGC filter.		
40	IF GND	GND terminal for IF circuit.		—
41 42	IF in	Input terminals for IF signals. Pin41 and Pin42 are both input poles of differential amplifier.		
43	RF AGC	Output terminal for RF AGC control level.		
44	Black Det	Terminal to be connected with Black Det filter for black stretch.		
45	SVM / Monitor	Output terminal for monitor function. Also output terminal for SVM signal. Selectable through IIC bus		
46	APC filter	Terminal to be connected with APC filter for Chroma demodulation. This terminal voltage controls frequency of VCXO.		

Pin No.	Pin Name	Function	Interface Circuit	I/O Signal
47	YC Vcc 5V	Vcc terminal for Y/C circuit. Supply 5V.	—	—
48	Sync out	Output terminal for Sync pulse. A pull up resister is required because of its open collector output. (Pull up resister: minimum 4.7kohm)		
49	DVCC	Vcc terminal for Digital block. This terminal voltage is clipped about 3.3V by regulator circuit. Supply DVCC voltage from A VCC 8V(#17) voltage via 270Ω.	—	—
50	R out	Output terminal for R signal.		
51	G out	Output terminal for G signal.		
52	B out	Output terminal for B signal.		
53	TV DGND	GND terminal for digital block.	—	—

Microcontrollers Descriptions (MROM version: TMPA8873CMANG /CPANG /CRANG /CSANG)



2. TFA9842AJ

2-channel audio amplifier with volume control (SE: 1 W to 7.5 W)

1. General description

The TFA9842AJ contains two identical audio power amplifiers. The TFA9842AJ can be used as two Single-Ended (SE) channels with a volume control. The maximum gain is 26 dB.
The TFA9842AJ comes in a 9-pin DIL-bent-SIL (DBS9P) power package. The TFA9842AJ is pin compatible with the TFA9843AJ, TFA9843(B)J, TFA9842(B)J and TFA9841J. The difference between the TFA9843AJ and the TFA9843(B)J,TFA9842(B)J, TFA9841J is the functionality of pin 7. The TFA9843AJ has a Volume Control (VC) on pin 7. The TFA9843(B)J, TFA9842(B)J and TFA9841J have a mode select (Mode) on pin 7.
The TFA9842AJ contains a unique protection circuit that is solely based on multiple temperature measurements inside the chip. This gives maximum output power for all supply voltages and load conditions with no unnecessary audio holes. Almost any supply voltage and load impedance combination can be made as long as thermal boundary conditions (number of channels used, external heatsink and ambient temperature) allow it.

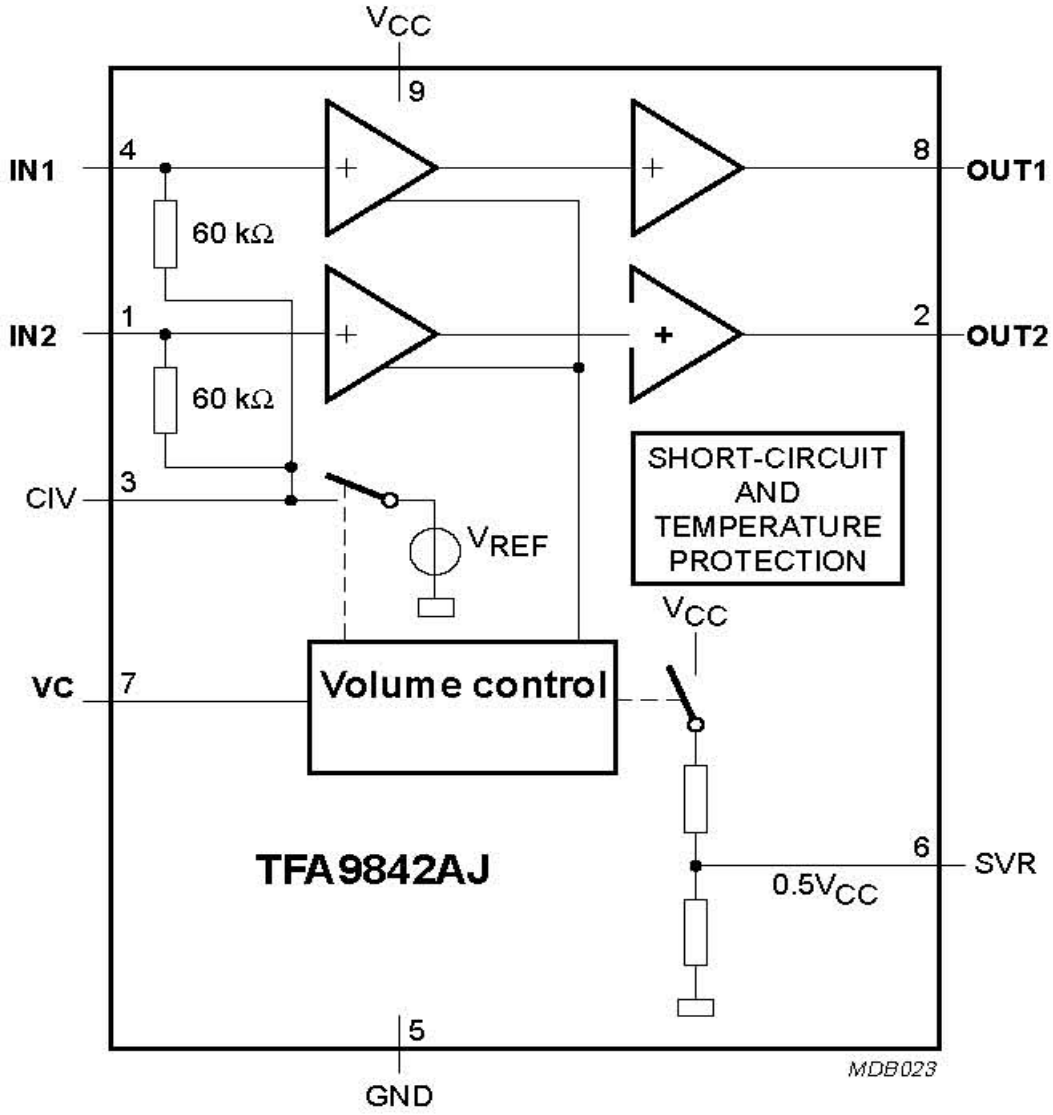
2. Features

- 2 Channel SE: 1 W to 7.5 W operation possibility
- Soft clipping
- Input clamps
- Volume control
- Standby and mute mode
- No on/off switching plops
- Low standby current
- High supply voltage ripple rejection
- Outputs short-circuit protected to ground, supply and across the load
- Thermally protected
- Pin compatible with the TFA9843AJ, TFA9843(B)J, TFA9842(B)J, TFA9841J.

3. Applications

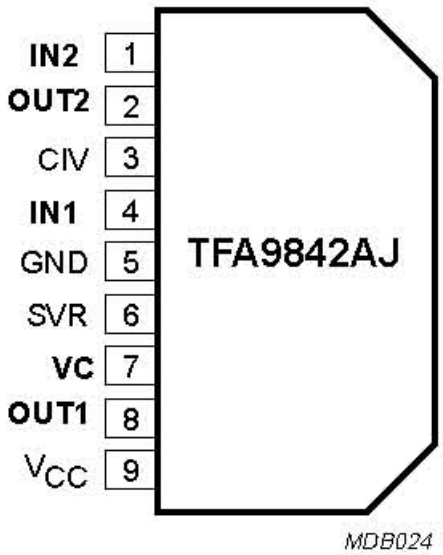
- CRT TV, LCD TV
- Monitors
- PC speakers
- Boom box
- Mini and micro audio receivers.

3. Block diagram



4. Pinning information

4.1 Pinning



4.2 Pin description

Symbol	Pin	Description
IN2	1	input 2
OUT2	2	loudspeaker terminal 2
CIV	3	common input voltage decoupling
IN1	4	input 1
GND	5	ground
SVR	6	half supply voltage decoupling (ripple rejection)
VC	7	volume control input (standby, mute and volume control)
OUT1	8	loudspeaker terminal 1
V_{CC}	9	supply voltage

4. VERTICAL SCAN OUTPUT STAGE CIRCUIT LA78040/LA78041

Both LA78040/LA78041 are vertical scan output stage power amplifiers. But there is a little bit difference between the two amplifiers, that is, LA78040 has supply voltage of 24V and output current of 1.8AP-P while LA78041 has supply voltage of 30V and output current of 2.2AP-P.

LA78040/LA78041 (N602)

Vertical Deflection Output Circuit

1) Features

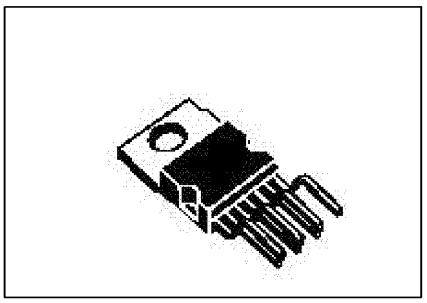
Low power dissipation due to built-in pump-up circuit

Vertical output circuit

Thermal protection circuit built in

Excellent crossover characteristics

DC coupling possible



Package Type:TO-220-7H

Fig.12

2) Block Diagram

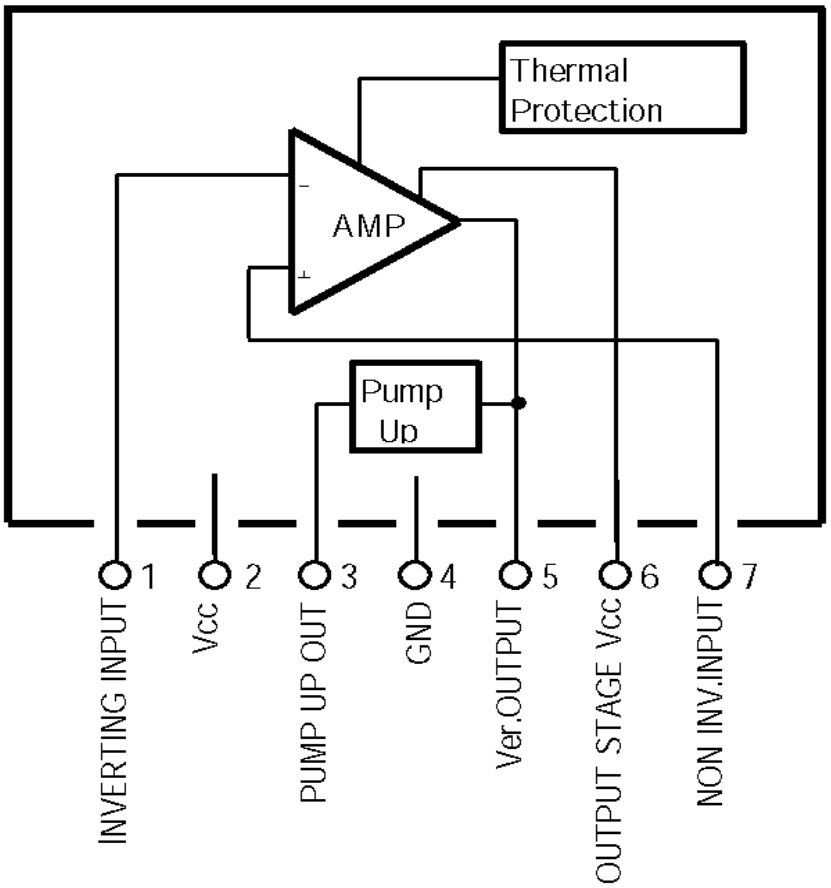


Fig.1 3 Block diagram

5．EEPROM AT24C04/08/16

1) Features

Low-voltage and Standard-voltage Operation

-2.7 (Vcc=2.7V to 5.5V)

-1.8 (Vcc=1.8V to 5.5V)

Internally Organized 128x8(1K), 256x8 (2K), 512x8 (4K),

1024x8 (8K) or 2048x8 (16K)

2-wire Serial Interface

Schmitt Trigger, Filtered Inputs for Noise Suppression

Bi-directional Data Transfer Protocol

100kHz (1.8V, 2.5V, 2.7V) and 400 kHz (5V) Compatibility

Write Protect Pin for Hardware Data Protection

8-byte Page (1K, 2K), 16-byte Page (4K, 8K, 16K) Write Modes

Partial Page Writes are Allowed

Self-timed Write Cycle (10 ms max)

High-reliability

-Endurance: 1 Million Write Cycles

- Data Retention: 100 Years

Automotive Grade and Extended Temperature Devices Available

8-lead PDIP, 8-lead JEDEC SOIC, 8-lead MAP and 8-lead TSSOP Package

2-wire

Serial EEPROM

AT24C01A 1K (128 x 8)

AT24C02 2K (256 x 8)

AT24C04 4K (512 x 8)

AT24C08 8K (1024 x 8)

AT24C16 6K (2048 x 8)

2) Description

The AT24C01A/02/04/08/16 provides 1024/2048/4096/8192/16384 bits of serial electrically erasable and programmable read-only memory (EEPROM) organized as 128/256/512/1024/2048 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operations are essential. The AT24C01A/02/04/08/16 is available in space-saving 8-pin PDIP, 8-lead JEDEC SOIC, 8-lead MAP and 8-lead TSSOP packages and is accessed via a 2-wire serial interface. In addition, the entire family is available in 2.7V (2.7V to 5.5V) and 1.8V (1.8V to 5.5V) versions.

3) Pin Configuration

Table 12

Pin Name	Function
A0-A2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
NC	No Connect

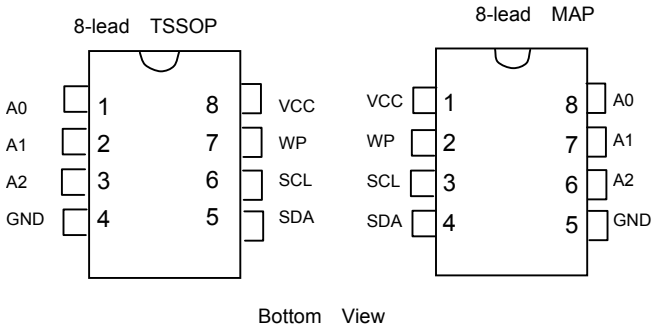


Fig. 14

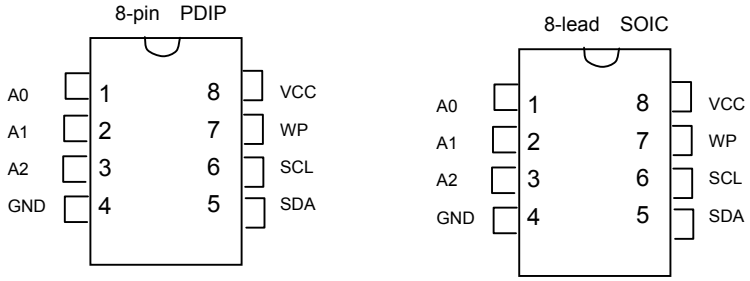


Fig. 15

4) Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bi-directional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open-collector devices.

DEVICE/PAGE ADDRESSES (A2, A1, A0): The A2, A1 and A0 pins are device address inputs that are hard wired for the AT24C01A and the AT24C02. As many as eight 1K/2K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section).

The AT24C04 uses the A2 and A1 inputs for hard wire addressing and a total of four 4K devices may be addressed on a single bus system. The A0 pin is a no connect.

The AT24C08 only uses the A2 input for hardwire addressing and a total of two 8K devices may be addressed on a single bus system. The A0 and A1 pins are no connects.

The AT24C16 does not use the device address pins, which limits the number of devices on a single bus to one. The A0, A1 and A2 pins are no connects.

WRITE PROTECT (WP): The AT24C01A/02/04/16 has a Write Protect pin that provides hardware data

protection. The Write Protect pin allows normal read/write operations when connected to ground (GND). When the Write Protect pin is connected to Vcc, the write protection feature is enabled and operates as shown in table 14.

Table 13

WP Pin Status	Part of the Array Protected				
	24C01A	24C02	24C04	24C08	24C16
At Vcc	Full (1K) Array	Full (2K) Array	Full (4K) Array	Normal Read/ Write Operation	Upper Half (8K) Array
At GND	Normal Read/Write Operations				

5) Memory Organization

AT24C01A, 1K SERIAL EEPROM: Internally organized with 16 pages of 8 bytes each, the 1K requires a 7-bit data word address for random word addressing.

AT24C02, 2K SERIAL EEPROM: Internally organized with 32 pages of 8 bytes each, the 2K requires an 8-bit data word address for random word addressing.

AT24C04, 4K SERIAL EEPROM: Internally organized with 32 pages of 16 bytes each, the 4K requires a 9-bit data word address for random word addressing.

AT24C08, 8K SERIAL EEPROM: Internally organized with 64 pages of 16 bytes each, the 8K requires a 10-bit data word address for random word addressing.

AT24C16, 16K SERIAL EEPROM: Internally organized with 128 pages of 16 bytes each, the 16K requires an 11-bit data word address for random word addressing.

6) Block Diagram

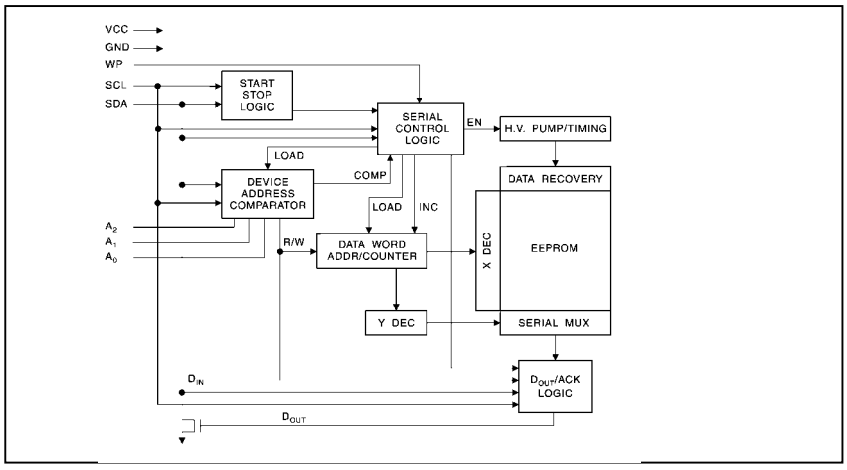


Fig.16

7) Refer to Table 21 about Functions and Data of the IC's Pins.

7. SWITCH-MODE POWER SUPPLY IC STRG5653/G8656

1). General Description

The STRG5653/G8656 are part of the STRG5600/G8600 series thick-film ICs for switch-mode power supply incorporating power MOSFET with a high-precise error amplifier. The ICs feature fewer external components, small-size and standard power supply.

The series STR-G8600 use Chip on Chip technology with the same operation principle as STR-G5600. Pin configuration, function and threshold of STR-G8600 are compatible with those of STR-G5600.

2) Block Diagram

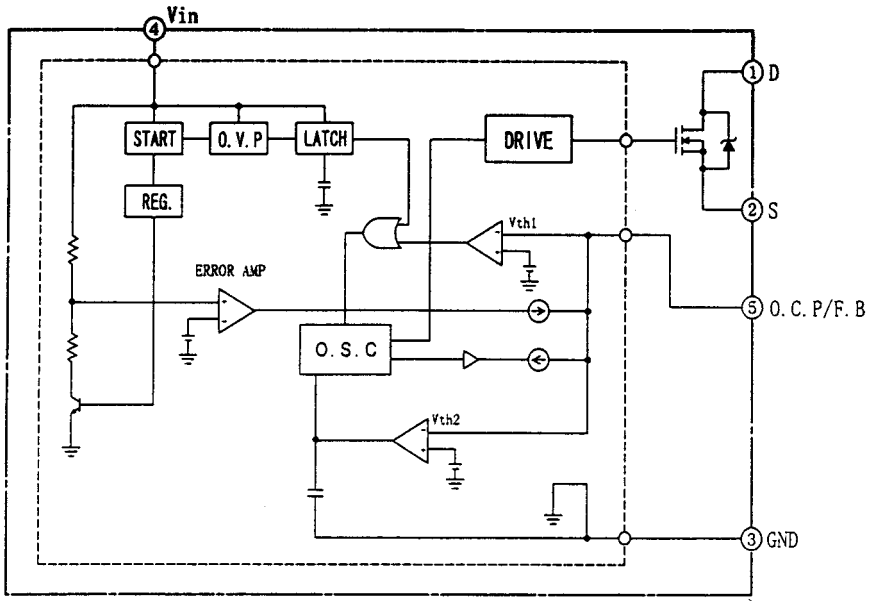


Fig.18

3) Function of Terminal

Table 15 Function of Terminal

Terminal No.	Symbols	Description	Functions
1	D	Drain Terminal	MOS FET drain
2	S	Source Terminal	MOS FET source
3	GND	Ground Terminal	Ground
4	VIN	Power supply Terminal	Input of power supply for control signals
5	O.C.P/F.B	Overcurrent/Feedback Terminal	Input of overcurrent detection signal and constant voltage signals

4) Refer to Table 22 about Functions and Data of the IC's Pins.

protection. The Write Protect pin allows normal read/write operations when connected to ground (GND). When the Write Protect pin is connected to Vcc, the write protection feature is enabled and operates as shown in table 14.

Table 13

WP Pin Status	Part of the Array Protected				
	24C01A	24C02	24C04	24C08	24C16
At Vcc	Full (1K) Array	Full (2K) Array	Full (4K) Array	Normal Read/ Write Operation	Upper Half (8K) Array
At GND	Normal Read/Write Operations				

5) Memory Organization

AT24C01A, 1K SERIAL EEPROM: Internally organized with 16 pages of 8 bytes each, the 1K requires a 7-bit data word address for random word addressing.

AT24C02, 2K SERIAL EEPROM: Internally organized with 32 pages of 8 bytes each, the 2K requires an 8-bit data word address for random word addressing.

AT24C04, 4K SERIAL EEPROM: Internally organized with 32 pages of 16 bytes each, the 4K requires a 9-bit data word address for random word addressing.

AT24C08, 8K SERIAL EEPROM: Internally organized with 64 pages of 16 bytes each, the 8K requires a 10-bit data word address for random word addressing.

AT24C16, 16K SERIAL EEPROM: Internally organized with 128 pages of 16 bytes each, the 16K requires an 11-bit data word address for random word addressing.

6) Block Diagram

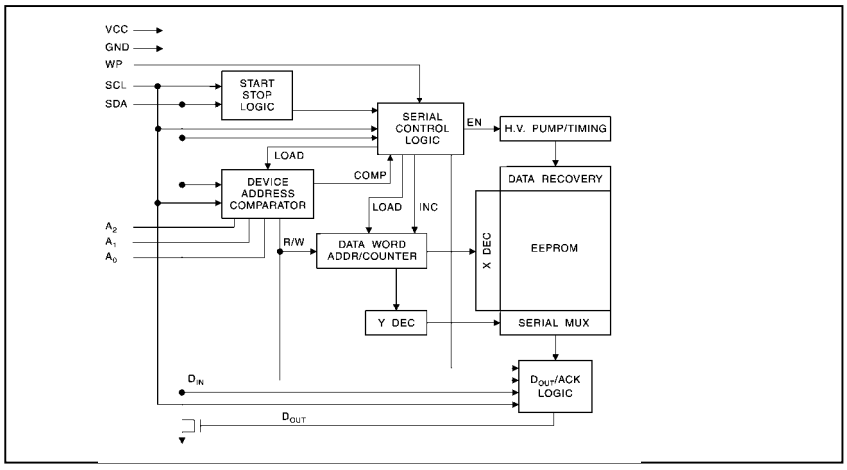


Fig.16

7) Refer to Table 21 about Functions and Data of the IC's Pins.

SERVICE DATA OF KEY ICS

Table 16 Ground Resistance of TMPA8873 Pins

Pin No	1	2	3	4	5	6
Resistance	>2000 KΩ	>2000 KΩ	-	0	5.6 KΩ	>2000 KΩ
Pin No	7	8	9	10	11	12
Resistance	>2000 KΩ	0	>2000 KΩ	0	0	>2000 KΩ
Pin No	13	14	15	16	17	18
Resistance	-	>2000 KΩ	>2000 KΩ	18.6 KΩ	10.6 KΩ	0
Pin No	19	20	21	22	23	24
Resistance	>2000 KΩ	>2000 KΩ	>2000 KΩ	107 KΩ	93.2 KΩ	3.2 KΩ
Pin No	25	26	27	28	29	30
Resistance	0.56 KΩ	24.70 KΩ	16.65 KΩ	22.04 KΩ	0.3 KΩ	3.27 KΩ
Pin No	31	32	33	34	35	36
Resistance	3.2 KΩ	107 KΩ	>2000 KΩ	>2000 KΩ	1500 KΩ	1.9 KΩ
Pin No	37	38	39	40	41	42
Resistance	>2000 KΩ	100 KΩ	>2000 KΩ	0	56 KΩ	56 KΩ
Pin No	43	44	45	46	47	48
Resistance	14.5 KΩ	220 KΩ	3.2 KΩ	>2000 KΩ	1.9 KΩ	-
Pin No	49	50	51	52	53	54
Resistance	0.7 KΩ	69 KΩ	120 KΩ	69 KΩ	0	-
Pin No	55	56	57	58	59	60
Resistance	-	-	-	-	-	>2000 KΩ
Pin No	61	62	63	64		
Resistance	>2000 KΩ	-	>2000 KΩ	-		

Note: Measured when Power-off

Table 17 Operating Voltage of TMPA8873(N202)'s Pins

Pin No	1	2	3	4	5	6
Voltage (V)	0V	0V	5V	GND	5V	2.3V
Pin No	7	8	9	10	11	12
Voltage (V)	2.1V	GND	5V	GND	GND	1.1V
Pin No	13	14	15	16	17	18
Voltage (V)	2.2V	5.9V	4.1V	4.7V	8.3V	0V
Pin No	19	20	21	22	23	24
Voltage (V)	3.2V	2.4V	3.2V	3.8V	2.5V	2.5V
Pin No	25	26	27	28	29	30
Voltage (V)	0V	2.7V	4.5V	3.2V	3.2V	3.0V
Pin No	31	32	33	34	35	36
Voltage (V)	1.5V	3.9V	3.0V	3.1V	2.4V	5V
Pin No	37	38	39	40	41	42
Voltage (V)	2.0V	3.9V	3.0V	GND	0V	2.0V
Pin No	43	44	45	46	47	48
Voltage (V)	1.4V	2.6V	2.8V	2.3V	5.0V	4.5V
Pin No	49	50	51	52	53	54
Voltage (V)	3.4V	2.5V	2.5V	2.5V	GND	GND
Pin No	55	56	57	58	59	60
Voltage (V)	5V	0V	5V	5V	0V	5.0V
Pin No	61	62	63	64		
Voltage (V)	0V	4.5V	0.9V	0V		

Table 18 Functions and Service Data of TFA9842AJ's Pins

Pin No.	Symbol	Functions Description	Digital Multimeter	
			Reference Voltage(V)	Positive Resistance(20KΩ)
1	IN2	Input 2	4.7	18.2MΩ
2	OUT2	Loudspeaker terminal 2	9.0	28KΩ
3	CIV	Common input voltage decoupling	4.7	280KΩ
4	IN1	Input 2	4.7	18.2MΩ
5	GND	ground	0	0
6	SVR	Half supply voltage decoupling(ripple rejection)	10.4	-
7	VC	Volume control input(standby，mute and volume control)	20	11KΩ
8	OUT1	Loudspeaker terminal 1	9	-
9	VCC	supply voltage	20	1KΩ

Table 20 Functions and Service Data of LA78040's Pins

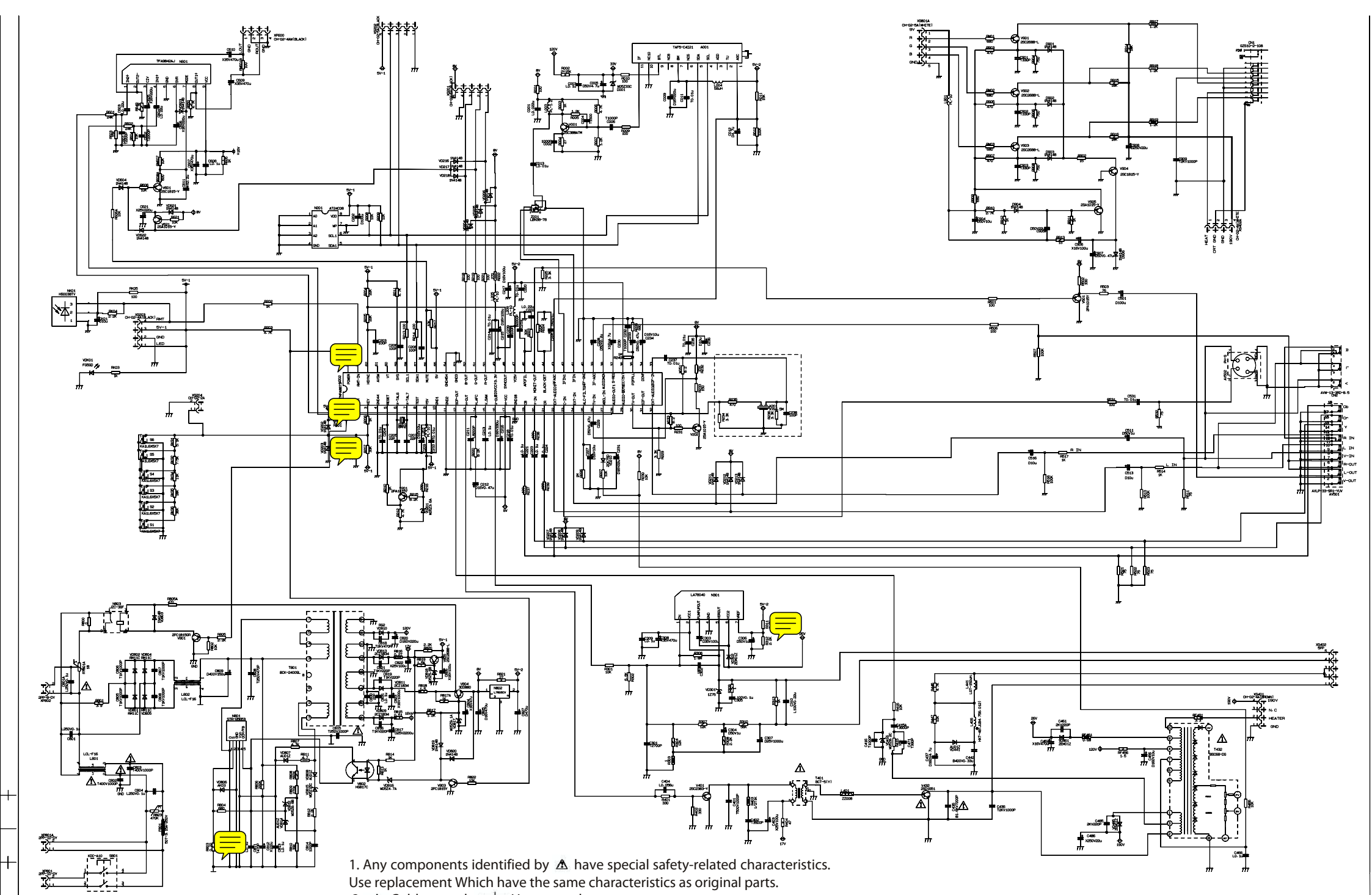
Pin No.	Function Description	GDM8145 Multimeter		
		Voltage of Pin (V)	Ground Resistance (KΩ)	
			Measure with red probe while grounding black probe.	Measure with black probe while grounding red probe.
1	INVERTING INPUT	2.04	-	2.62
2	VCC	25.02	-	1.87
3	Pump UP OUT	1.76	-	2.68
4	GND	0	0	0
5	Ver. OUTPUT	15.32	-	2.26
6	OUTPUT STAGE Vcc	25.20	∞	2.35
7	NON INV. INPUT	2.04	3.25	2.5

Table 21 Functions and Service Data of AT24C08/16 Pins

Pin No.	Function Description	Digital Multimeter		
		Reference Voltage (V)	Positive Resistance (20KΩ)	Negative Resistance (20KΩ)
1	Address input	0	0	0
2	Address input	0	0	0
3	Address input	0	0	0
4	Common ground	0	0	0
5	Clock line	5	13.79	11.22
6	Data line	5	13.70	13.13
7	PW write protect	0	0	0
8	Supply voltage	5	3.79	3.78

Table 22 Functions and Service Data of STR-G5653's Pins

Pin No.	Functions Description	Digital Multimeter		
		Reference Voltage (V)	Positive Resistance (20KΩ)	Negative Resistance (20KΩ)
1	Drain terminal	288	∞	∞
2	Source terminal	0.028	0	0
3	Ground terminal	0	0	0
4	Power supply terminal	32.24	∞	1.838
5	Overcurrent/Freedback terminal	1.85	0.68	0.68



1. Any components identified by ⚠ have special safety-related characteristics.
Use replacement Which have the same characteristics as original parts.
2. ⊥ Cold ground ⏚ Hot ground

This circuit diagram is only for reference, specifications are subject to change without reference.

Circuit Diagram FOR SF21GA63